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Architecting Chiplet-Based Systems

Natalie Enright Jerger
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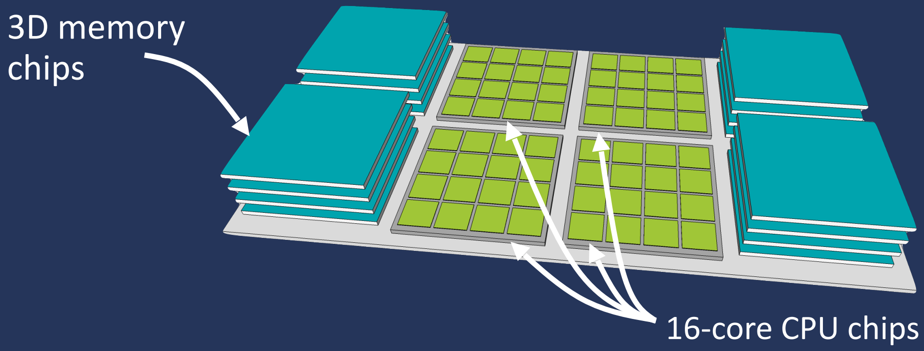

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Executive Summary

Why build chiplet-based systems?

How to build chiplet-based systems?

Where do we go from here?

Executive Summary

Why build chiplet-based systems?

- End of technology scaling
- Rise of heterogeneity
- Demands of big data

How to build chiplet-based systems?

Where do we go from here?

Executive Summary

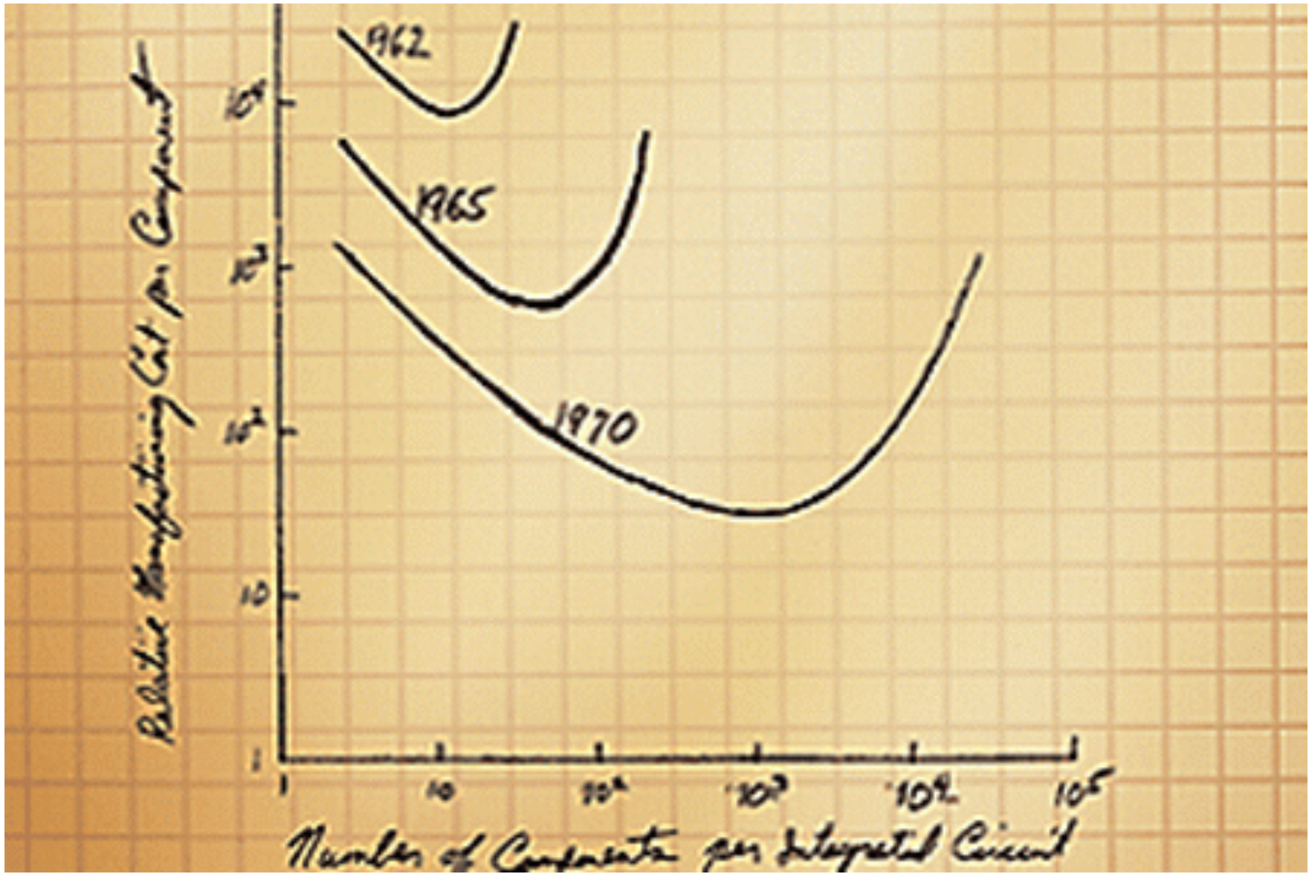
Why build chiplet-based systems?

How to build chiplet-based systems?

- Reintegrate with hybrid topologies
- Deadlock-free routing for independent, modular design

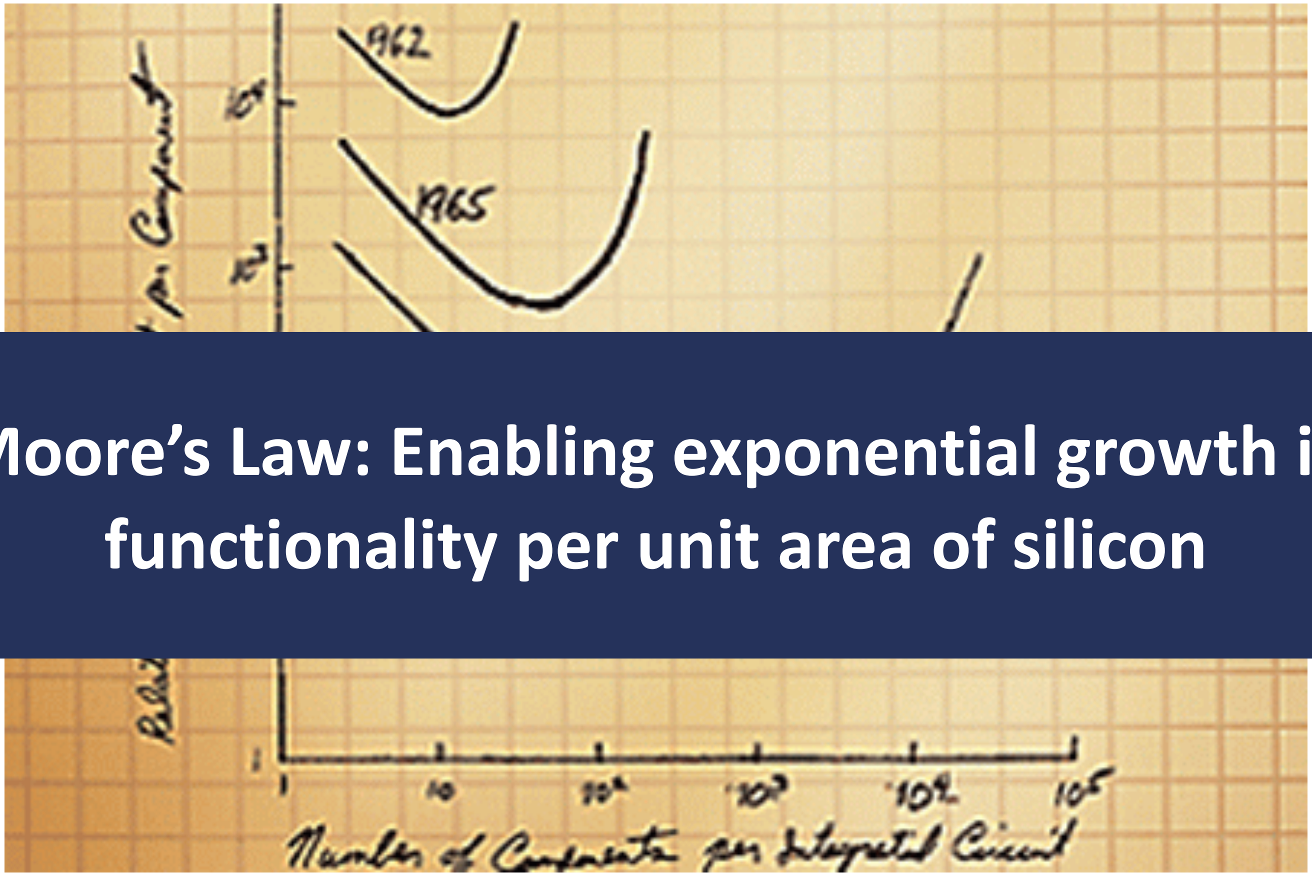
Where do we go from here?

Challenges: End of Scaling



Source: G.E. Moore, Electronics 1965

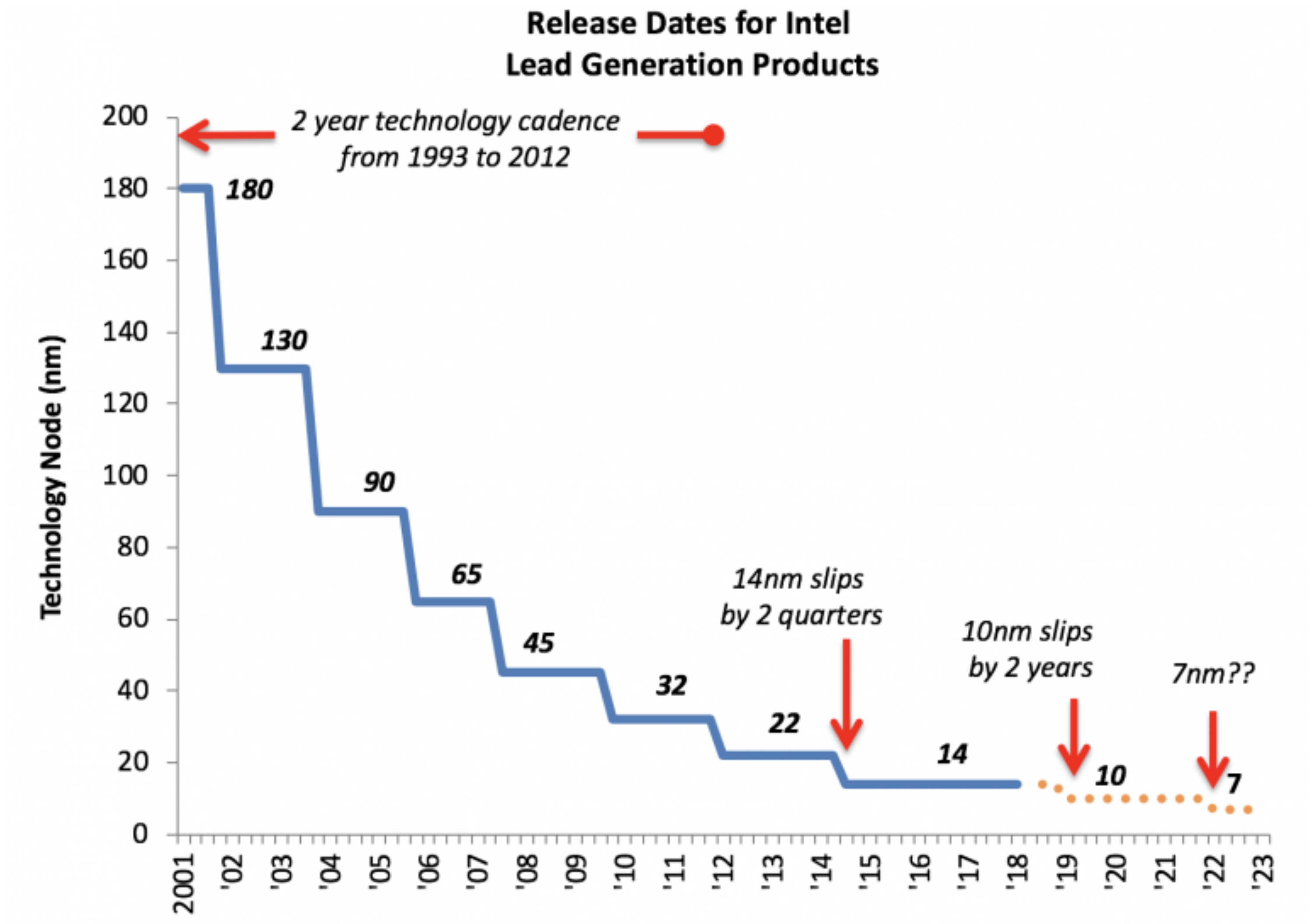
Challenges: End of Scaling



Moore's Law: Enabling exponential growth in functionality per unit area of silicon

Source: G.E. Moore, Electronics 1965

Challenges: End of Scaling



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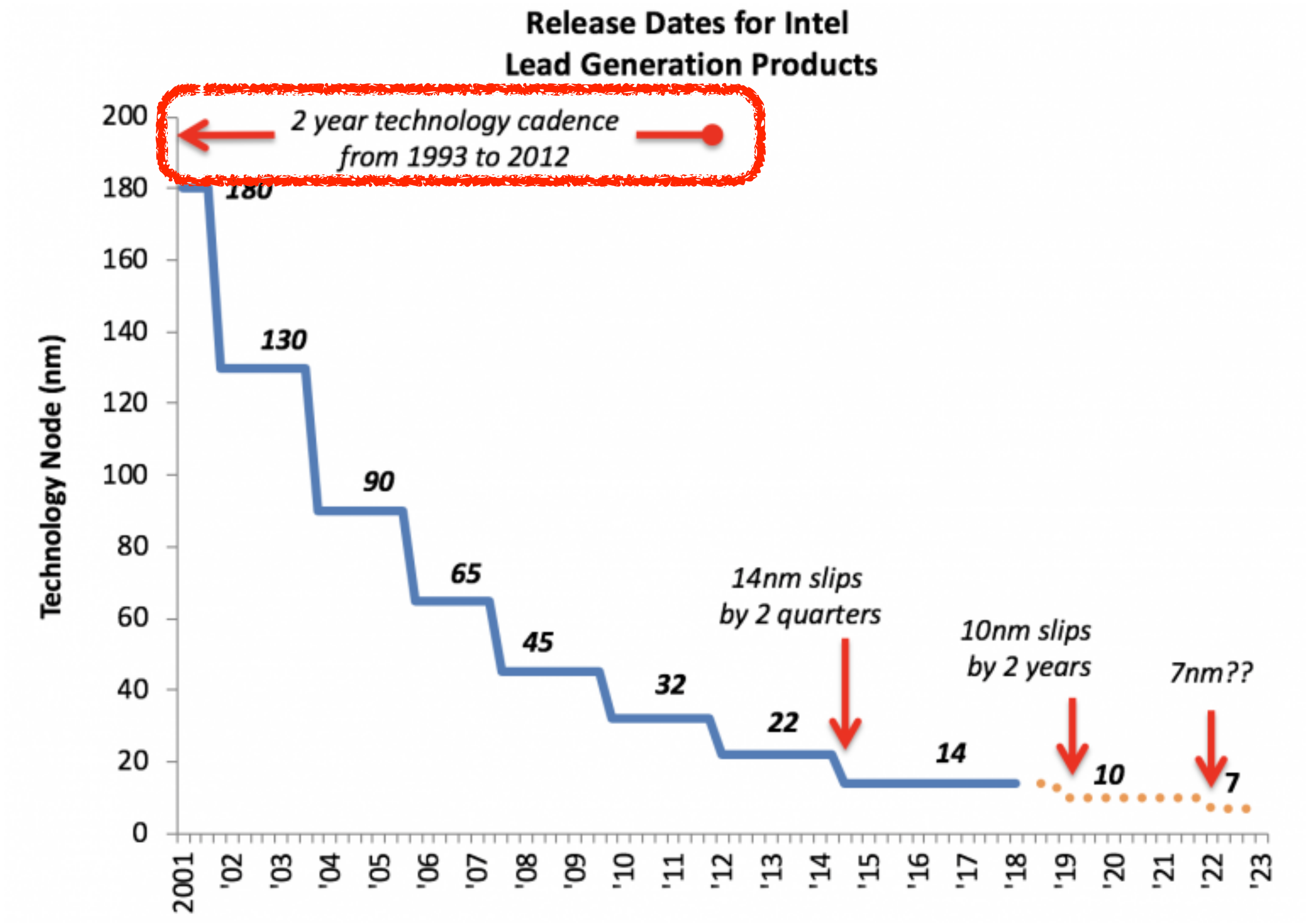

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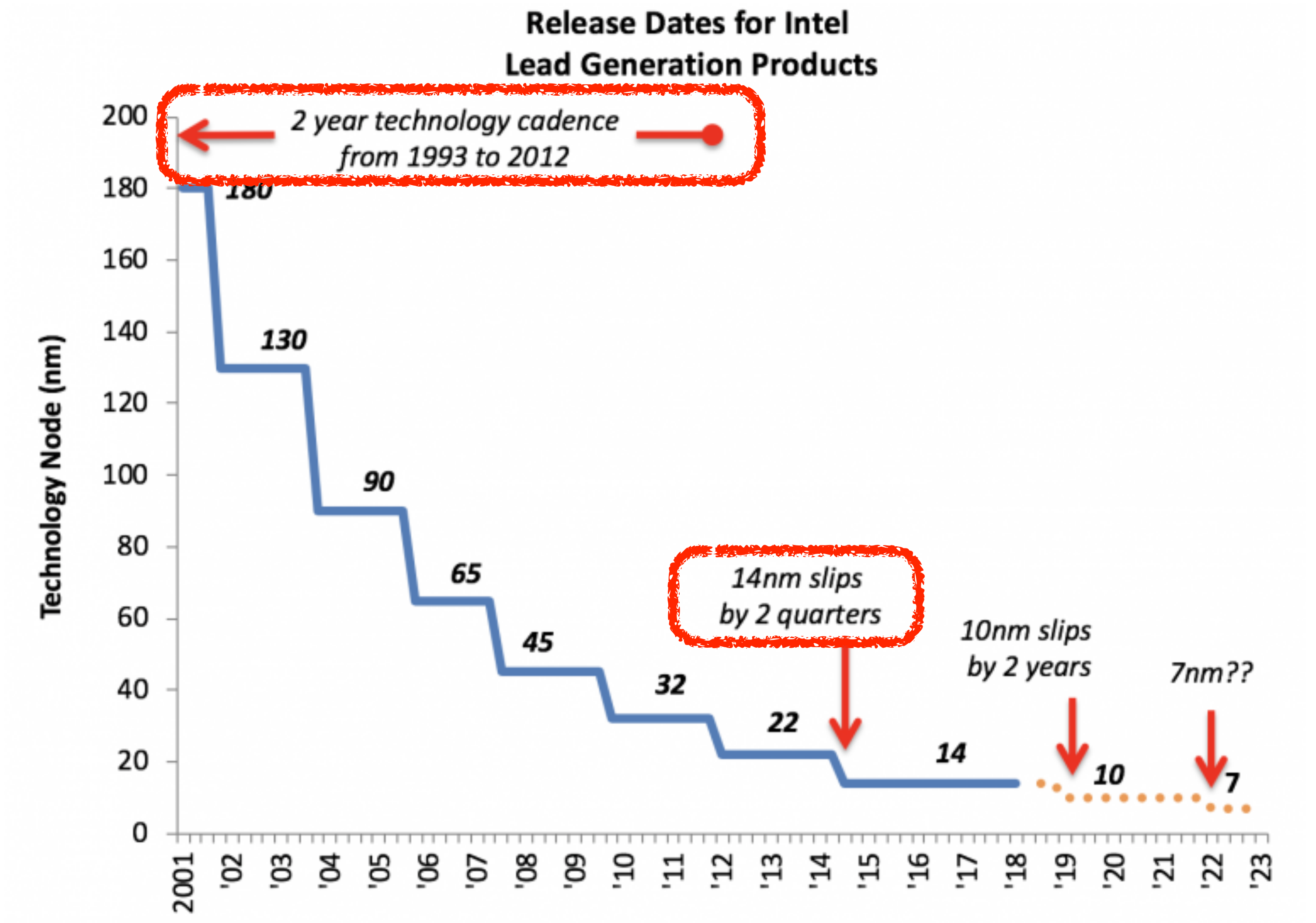

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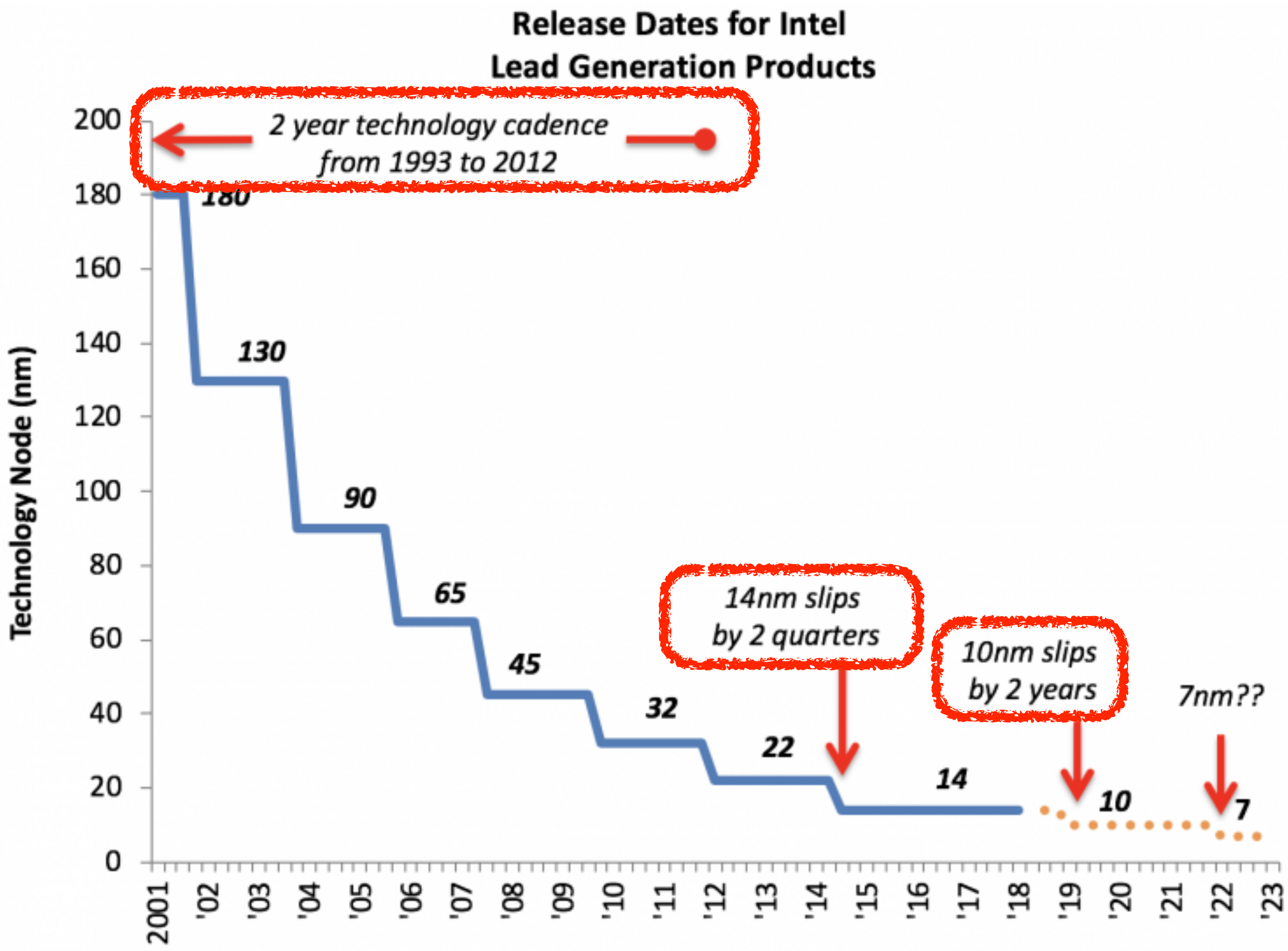

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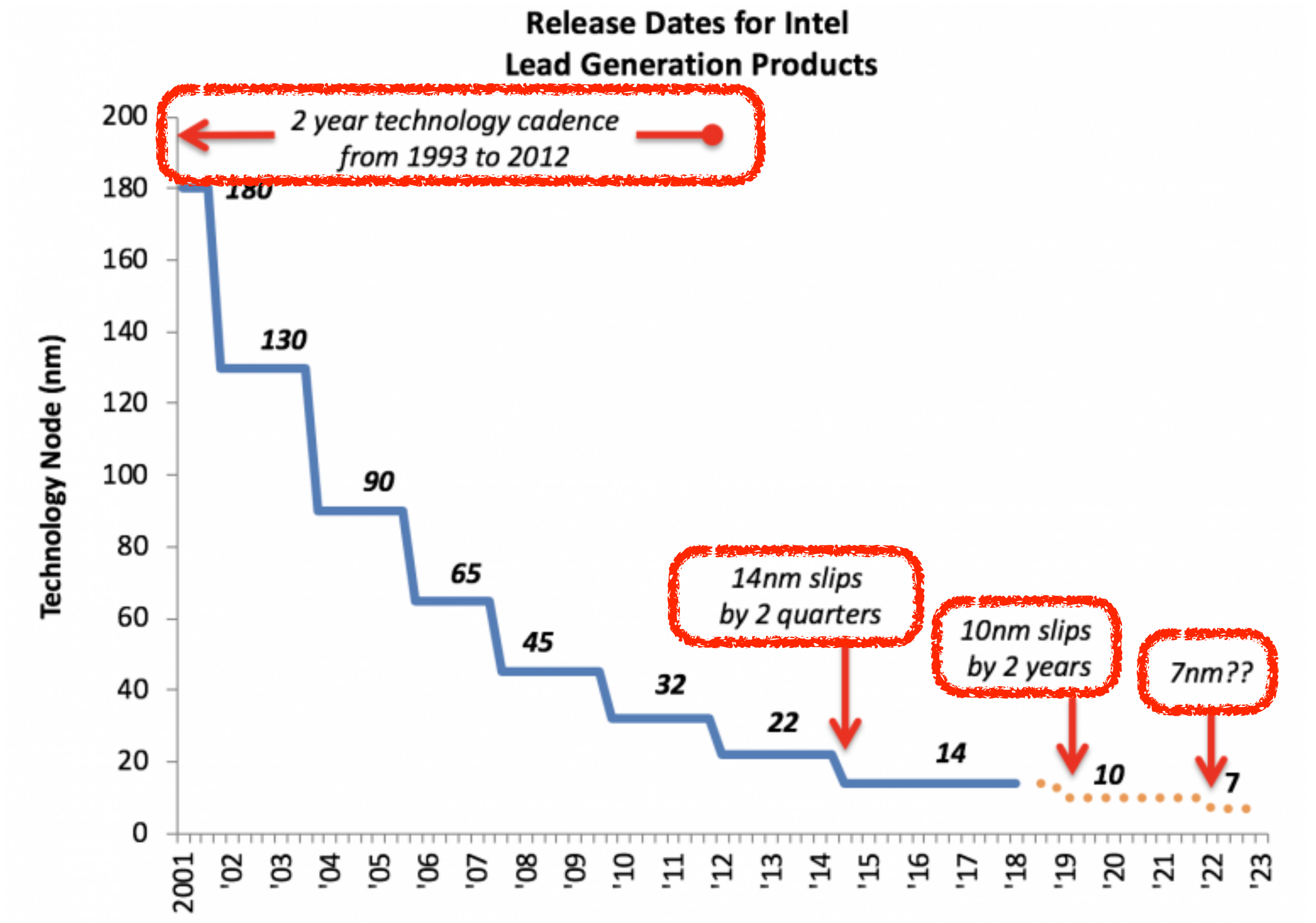

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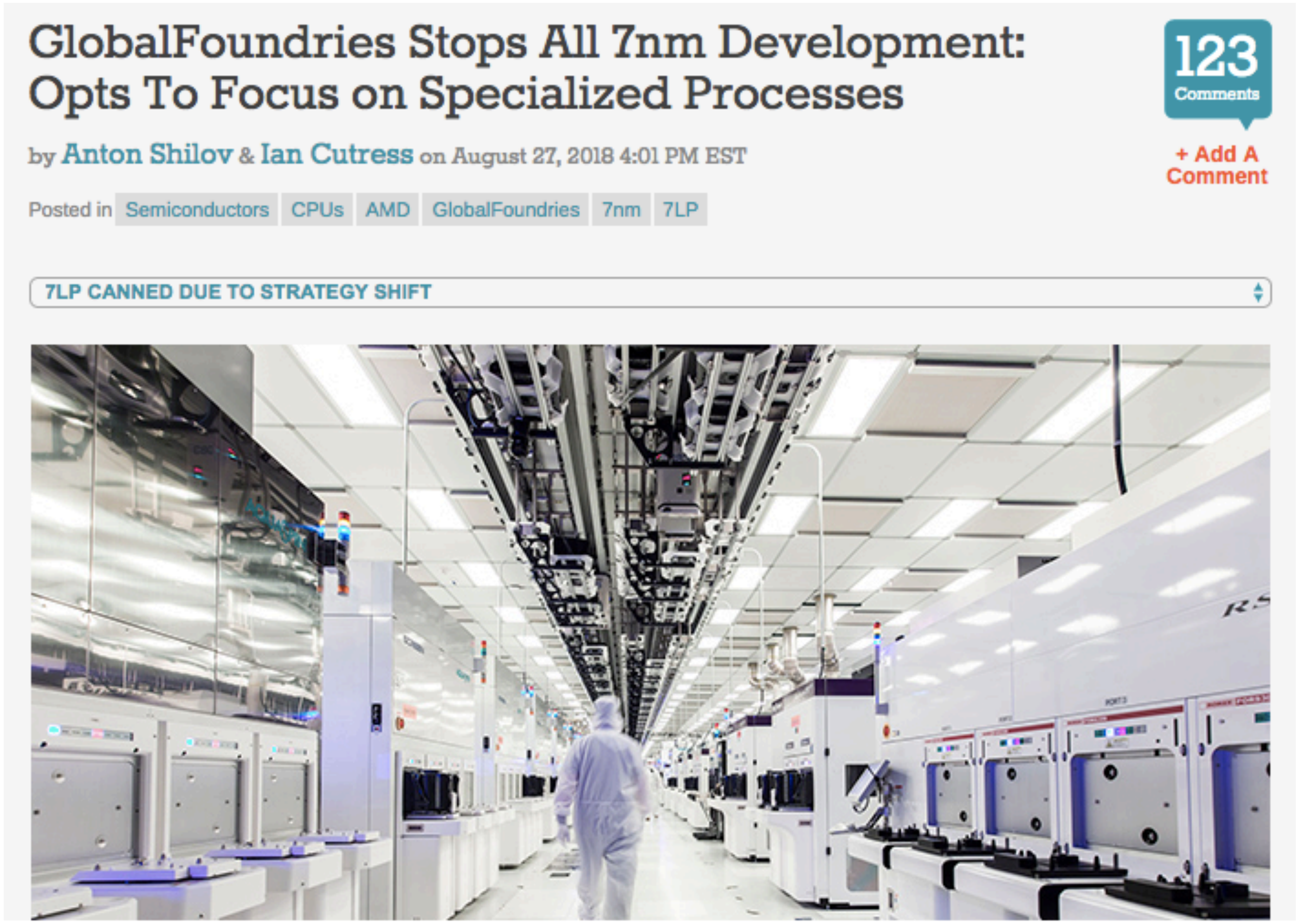
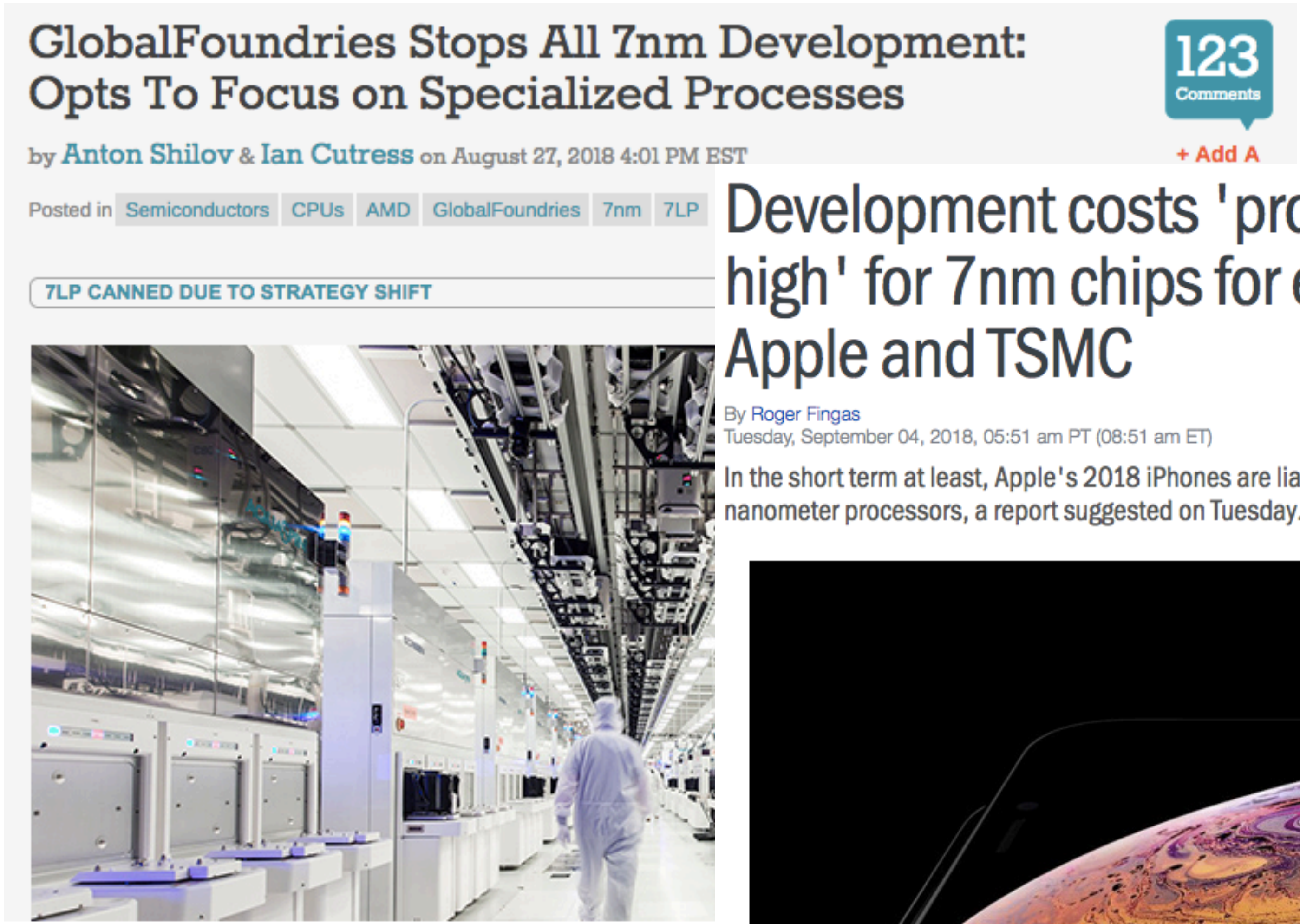


GlobalFoundries Stops All 7nm Development: Opts To Focus on Specialized Processes

by Anton Shilov & Ian Cutress on August 27, 2018 4:01 PM EST

Posted in Semiconductors CPUs AMD GlobalFoundries 7nm 7LP

Challenges: End of Scaling



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123 Comments

by Anton Shilov & Ian Cutress on August 27, 2018 4:01 PM EST

+ Add A

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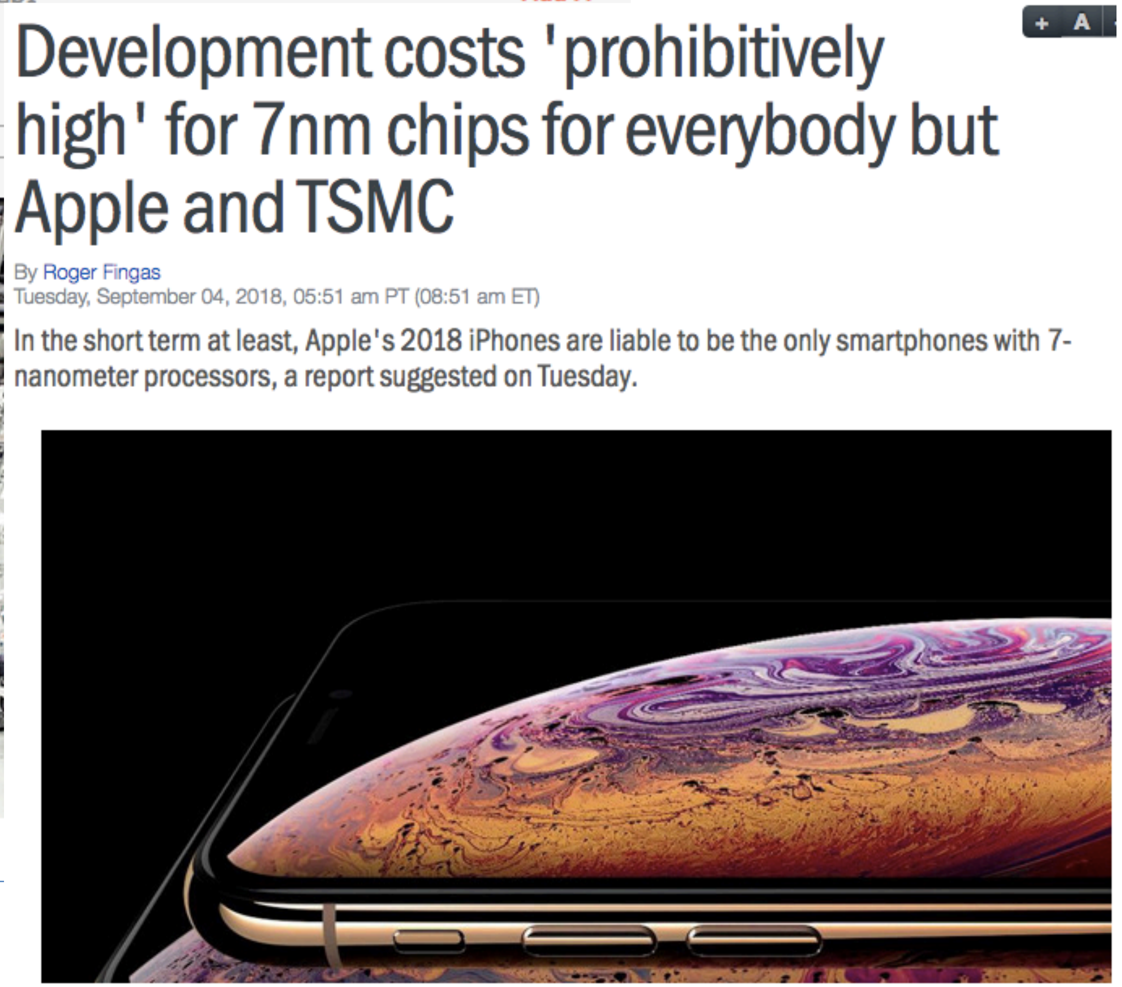
7LP CANNED DUE TO STRATEGY SHIFT



Development costs 'prohibitively high' for 7nm chips for everybody but Apple and TSMC

By Roger Fingas
Tuesday, September 04, 2018, 05:51 am PT (08:51 am ET)

In the short term at least, Apple's 2018 iPhones are liable to be the only smartphones with 7-nanometer processors, a report suggested on Tuesday.

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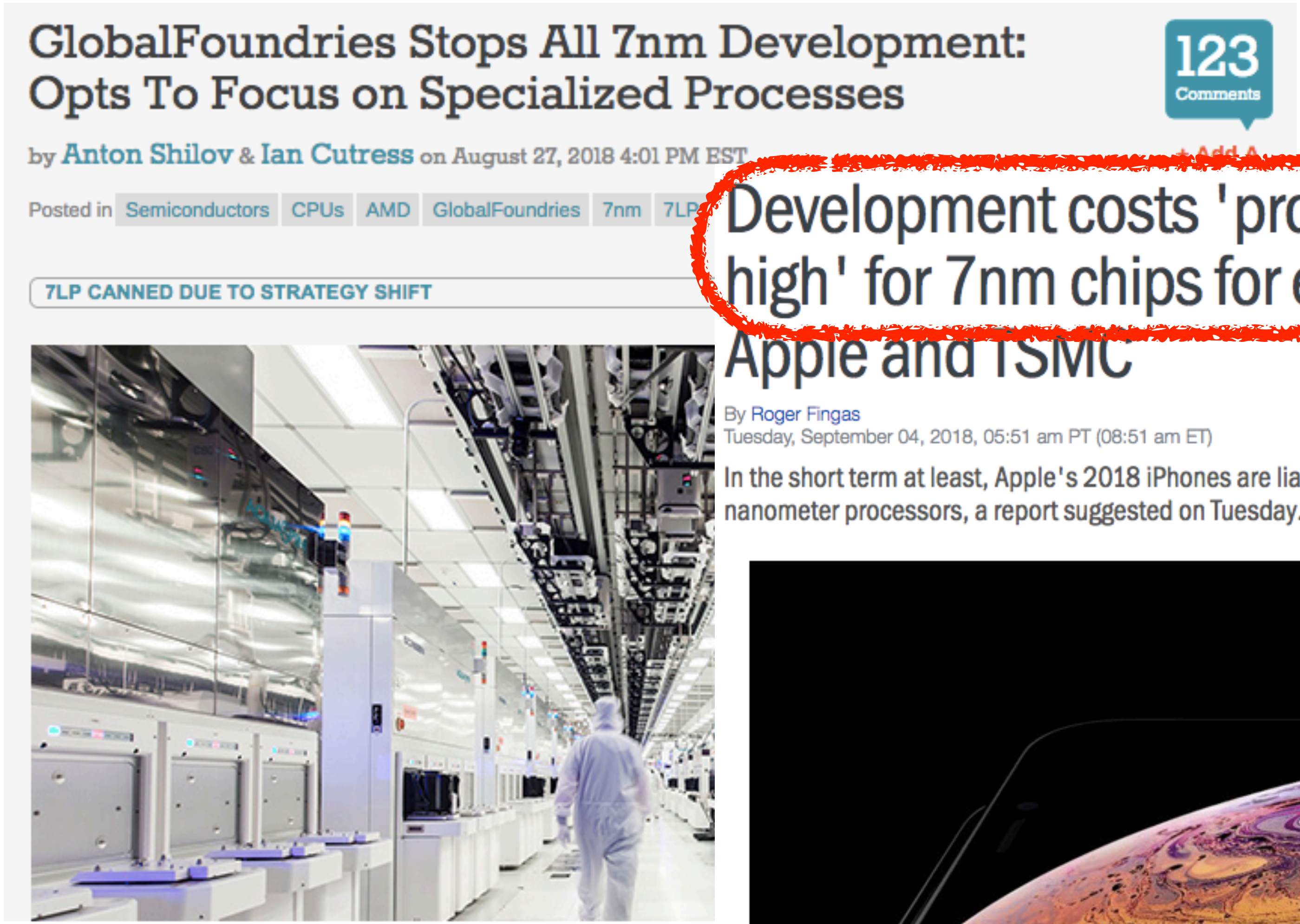

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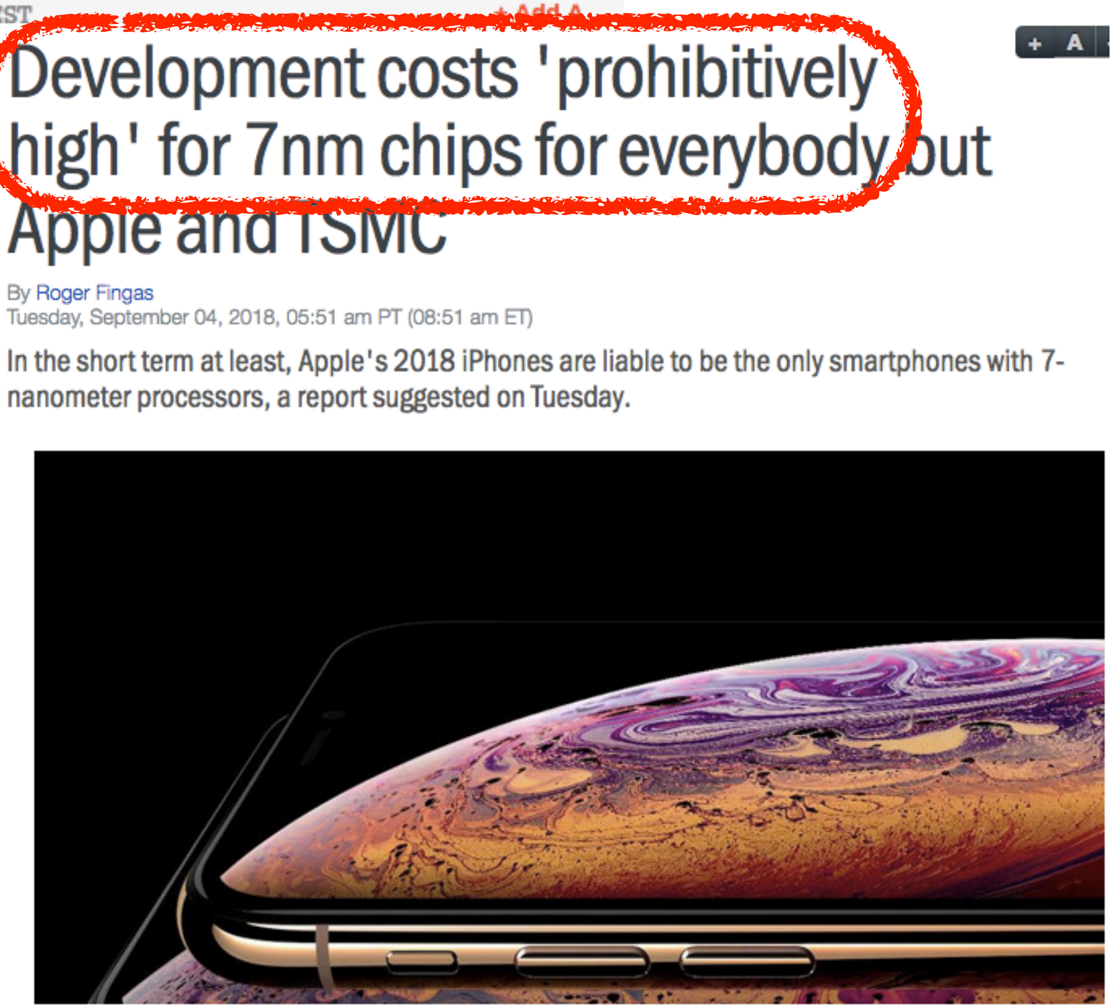

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7LP CANNED DUE TO STRATEGY SHIFT

Development costs 'prohibitively high' for 7nm chips for everybody but

Moving forward, limited ability to integrate more transistors on a chip

Need: Novel approaches to increase integration *affordably*

Challenges: The Rise of Heterogeneity

End of Dennard scaling

- Need power efficient alternatives to general purpose computing

Challenges: The Rise of Heterogeneity

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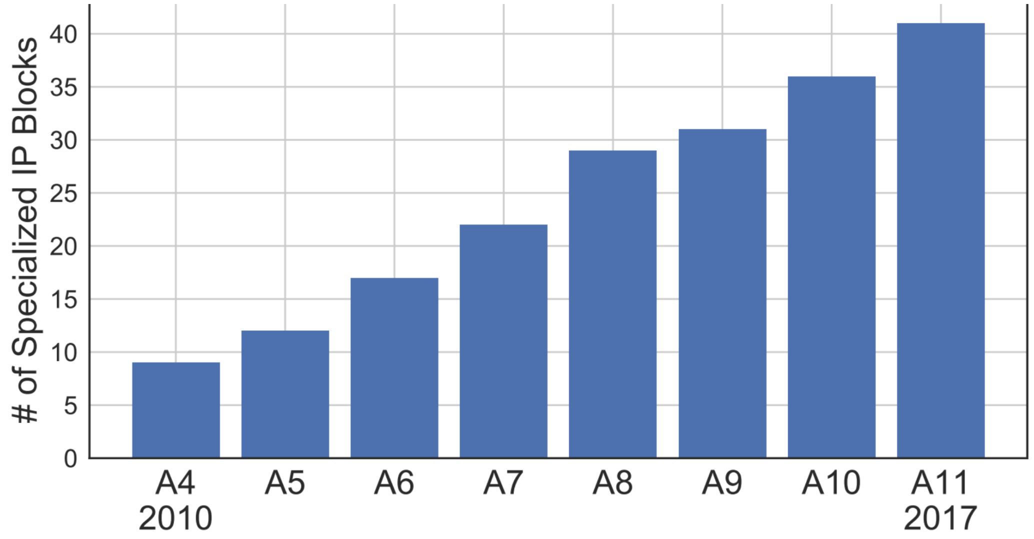
Need power efficient alternatives to general purpose computing



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Challenges: The Rise of Heterogeneity

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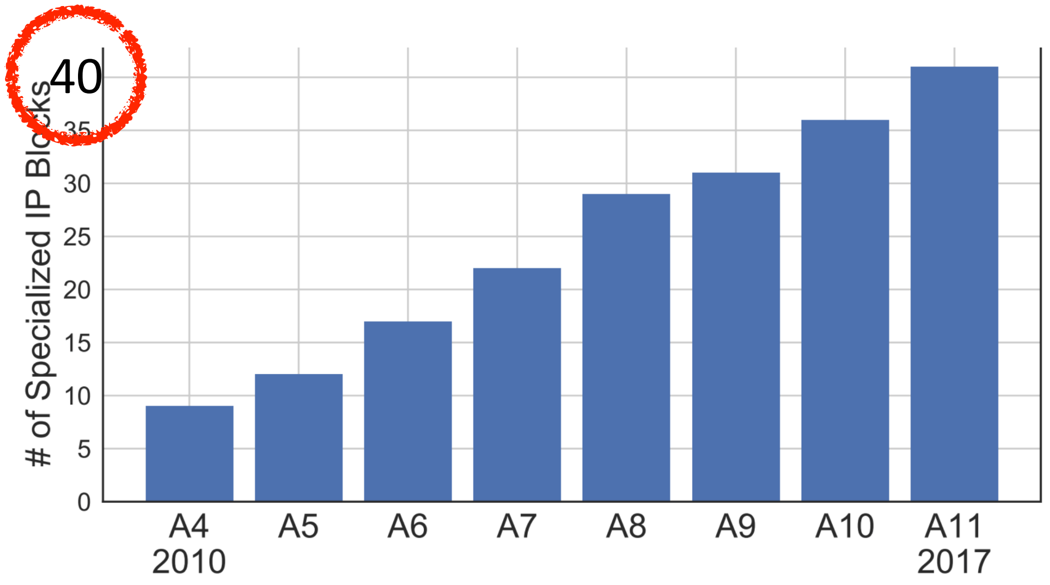
Need power efficient alternatives to general purpose computing



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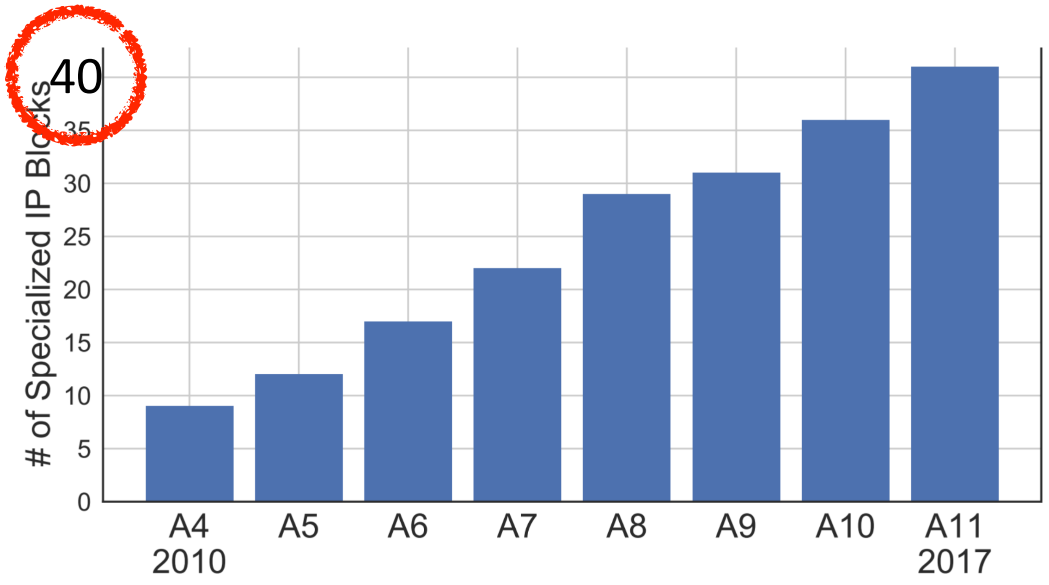

Source: David Brooks

Not just Machine Learning

Challenges: The Rise of Heterogeneity

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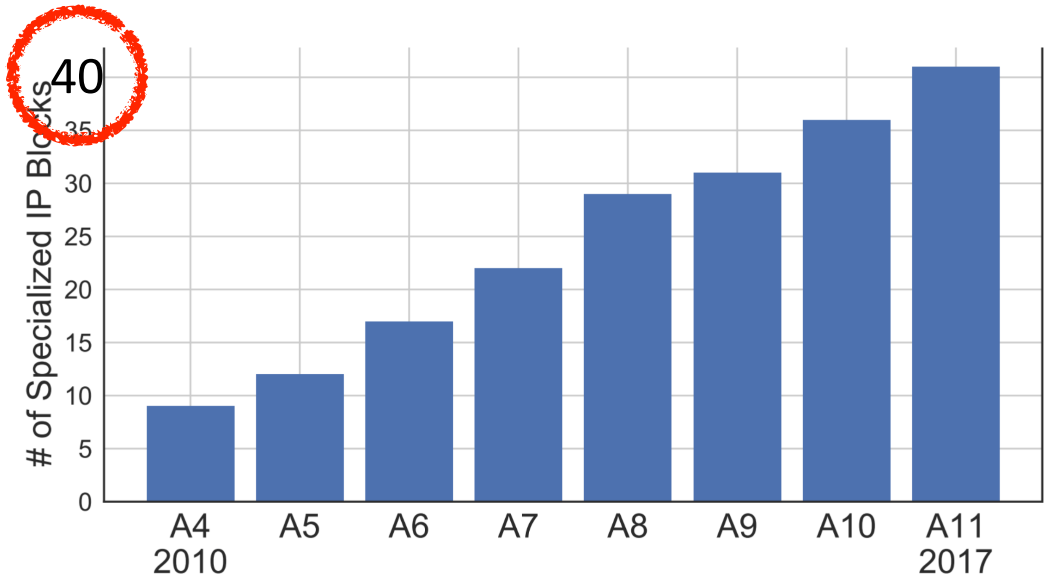
Need power efficient alternatives to general purpose computing

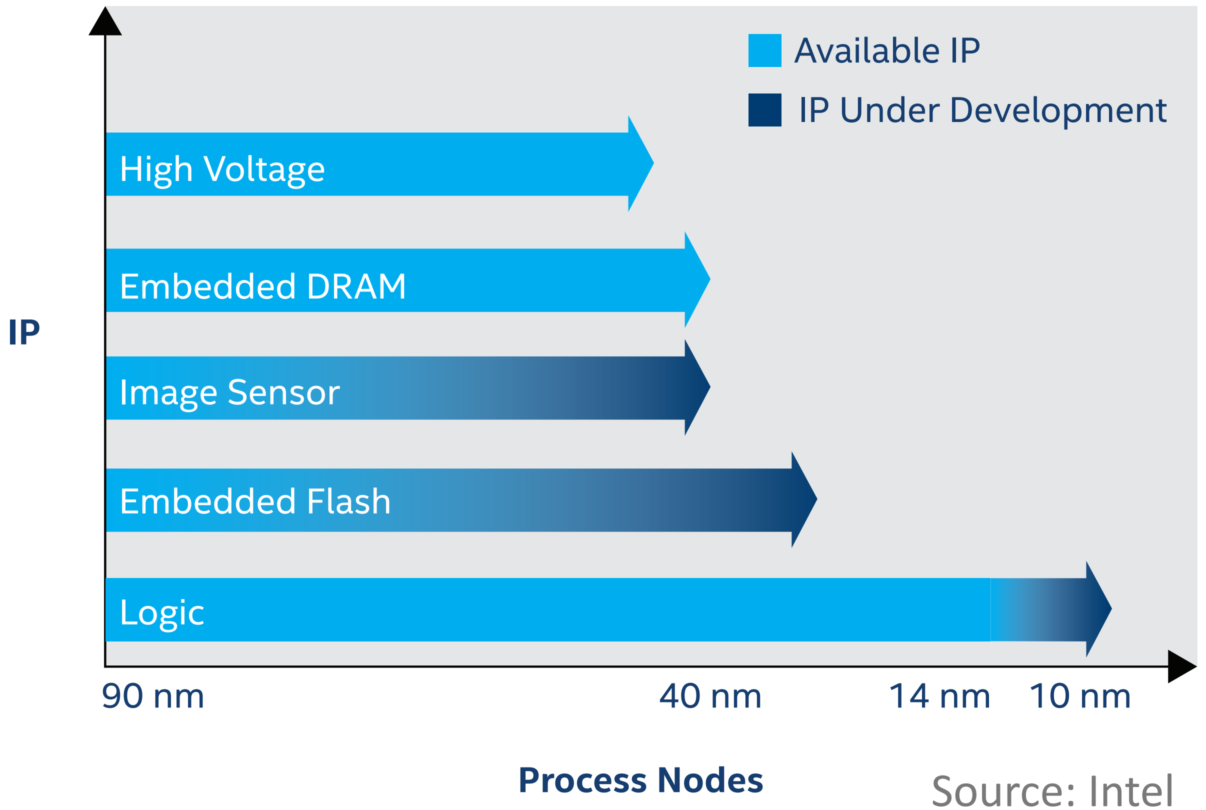


Source: David Brooks

Not just Machine Learning

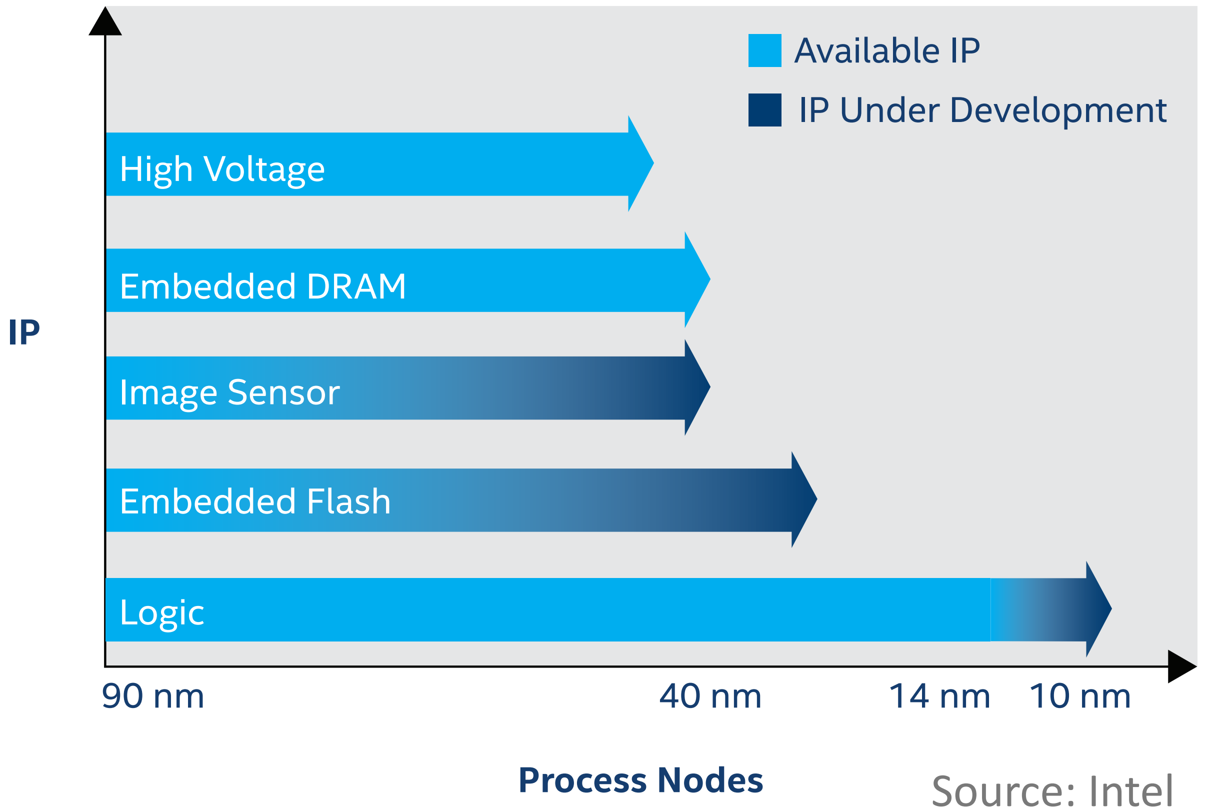
SoC integration challenges for datacentres, cellphones

Challenges: Rise of Heterogeneity



Source: Intel

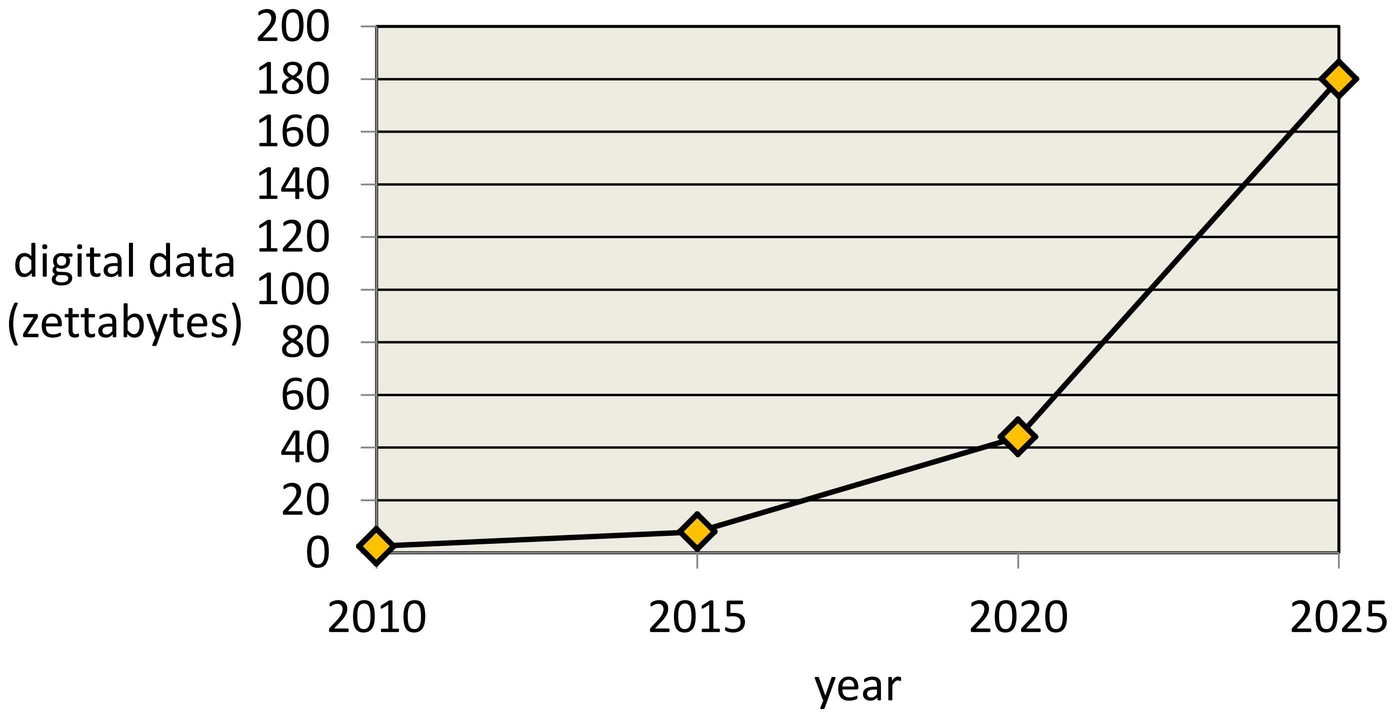
Challenges: Rise of Heterogeneity



Source: Intel

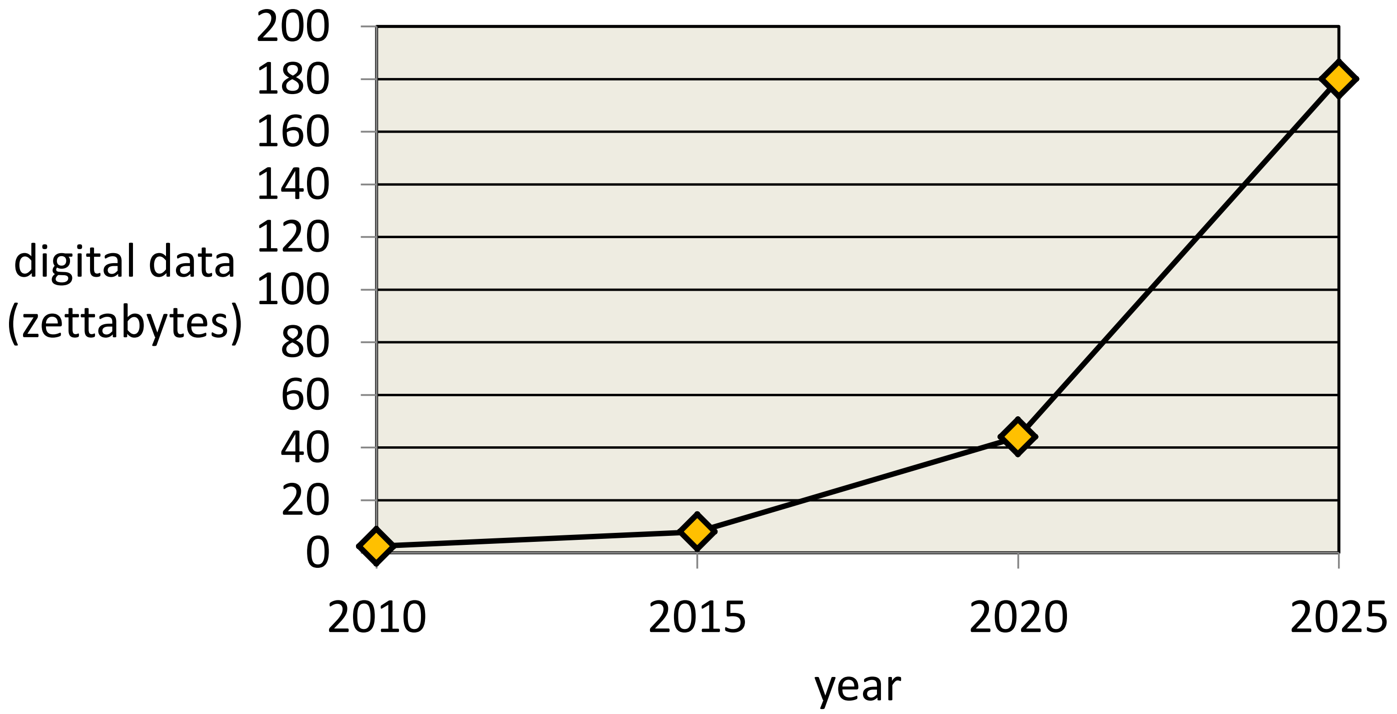
Heterogeneous manufacturing processes for different IP

Challenges: Big Data



Source: International Data Corporation, 2016

Challenges: Big Data



Workloads increasingly memory and communication bound
Need to integrate lots of memory!

What do we need?

What do we need?

A means to continue integrating more functionality

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A means to deal with IP and manufacturing heterogeneity

What do we need?

A means to continue integrating more functionality

A means to deal with IP and manufacturing heterogeneity

A means to enable greater memory integration and efficient communication

What do we need?

A means to continue integrating more functionality

A means to deal with IP and manufacturing heterogeneity

A means to enable greater memory integration and efficient communication

All while combating skyrocketing manufacturing costs

What do we need?

A means to continue integrating more functionality

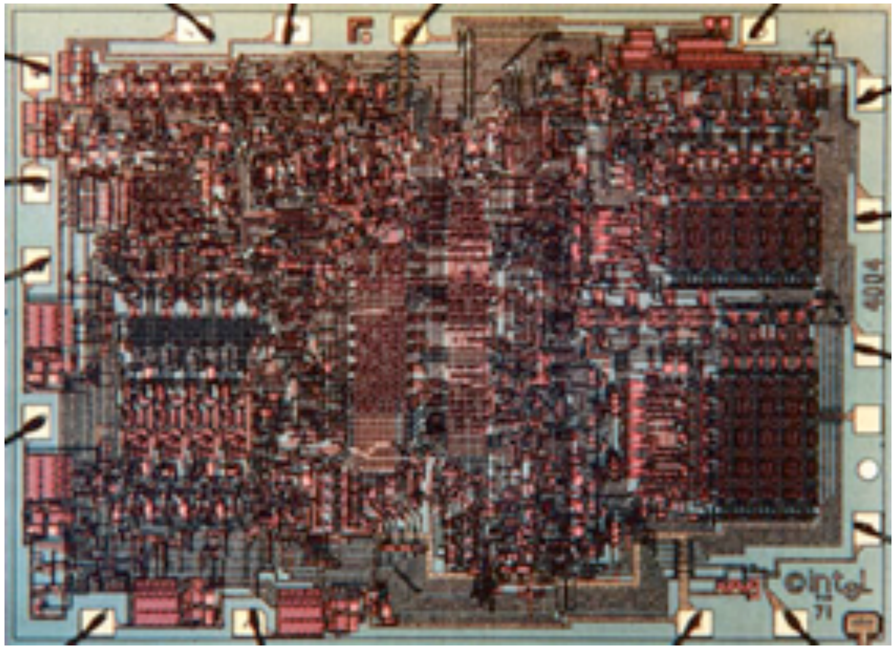
A means to deal with IP and manufacturing hetero

But first…

A mea and efficient communication

All while combating skyrocketing manufacturing costs

Walk down memory lane (1971)



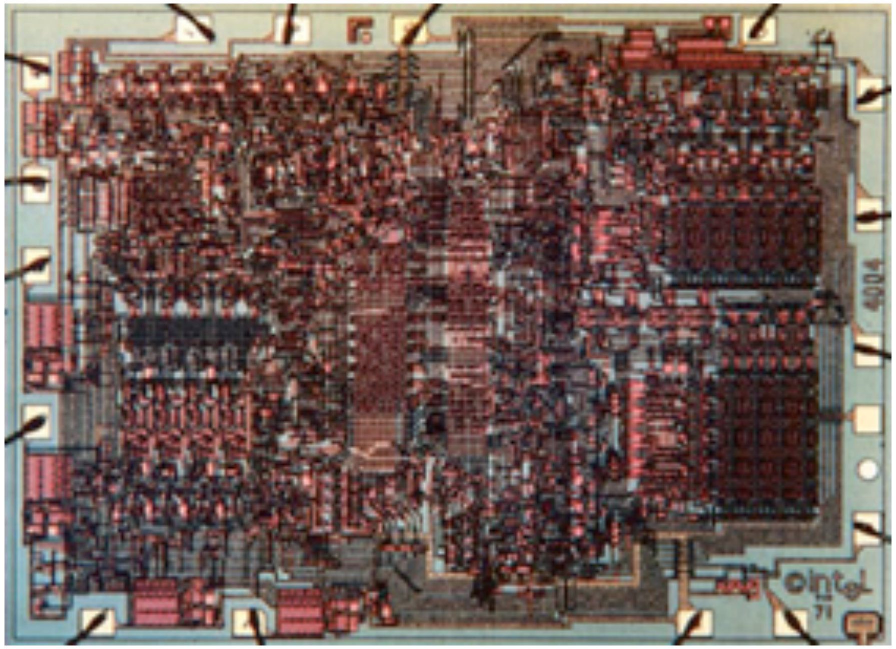
Intel introduces 4004

1st commercial microprocessor

2300 transistors

13mm^2

Walk down memory lane (1971)



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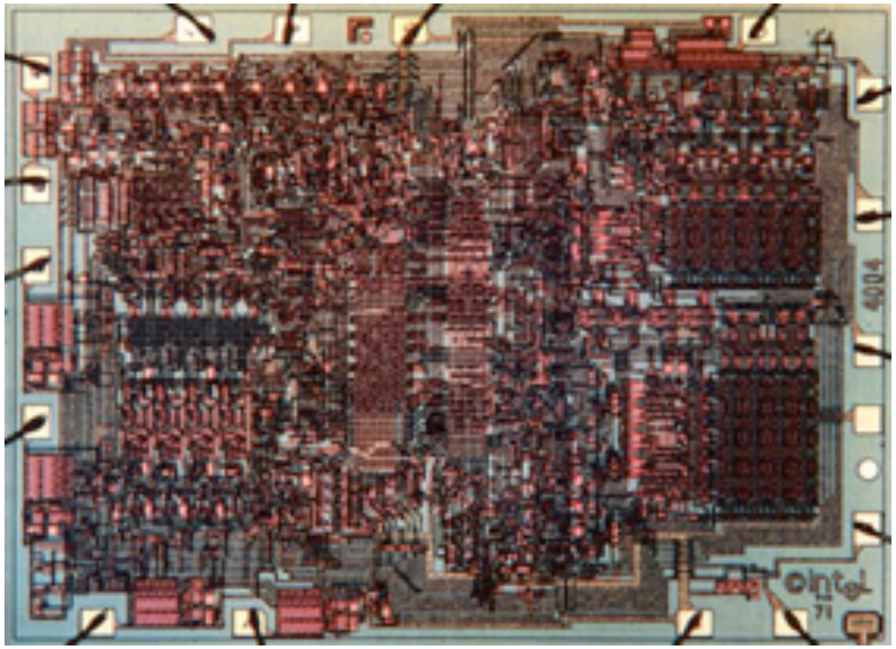
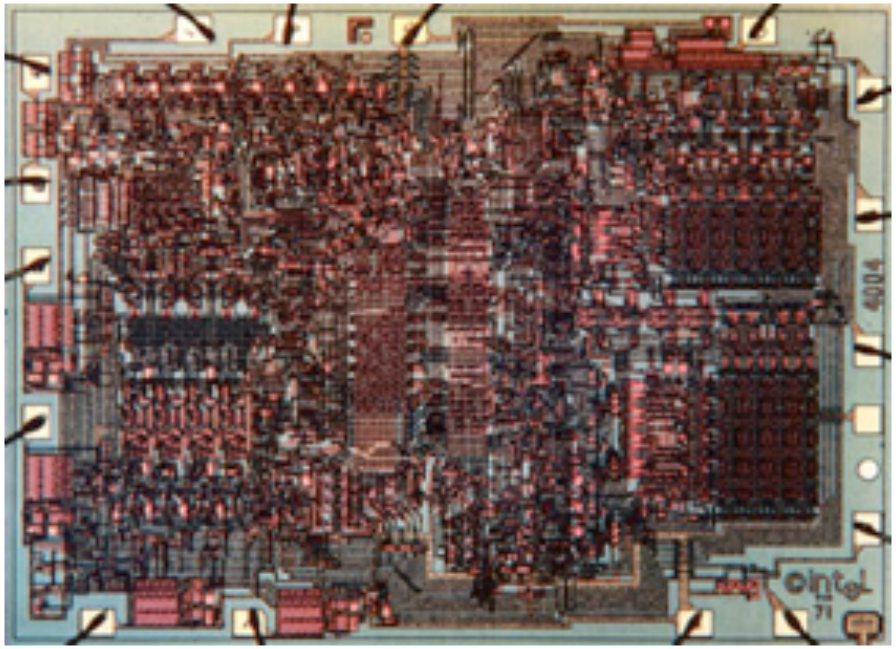


😁 Everything on one chip

Walk down memory lane (1971)



- 😁Everything on one chip
- 😁No more slow chip crossings

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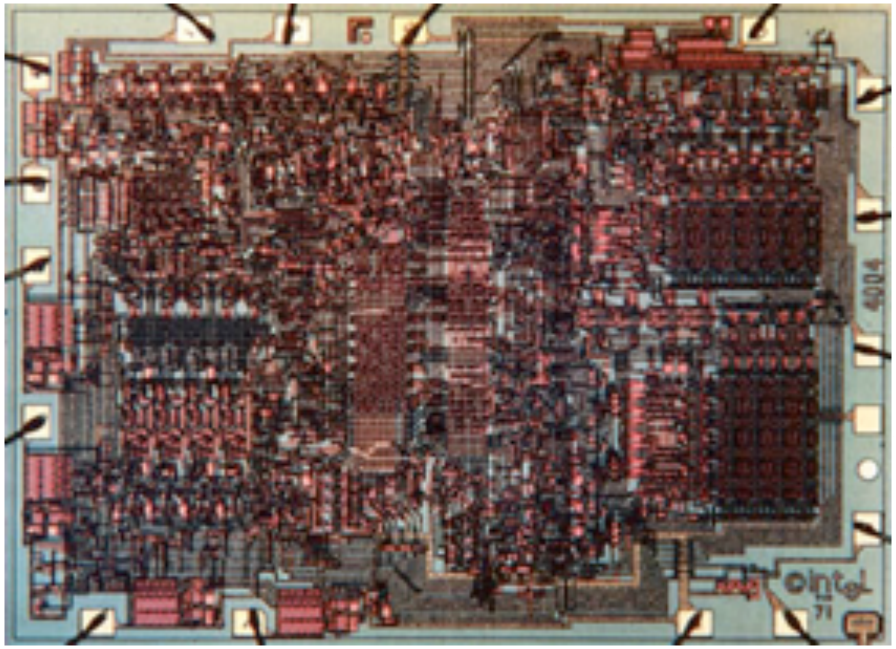

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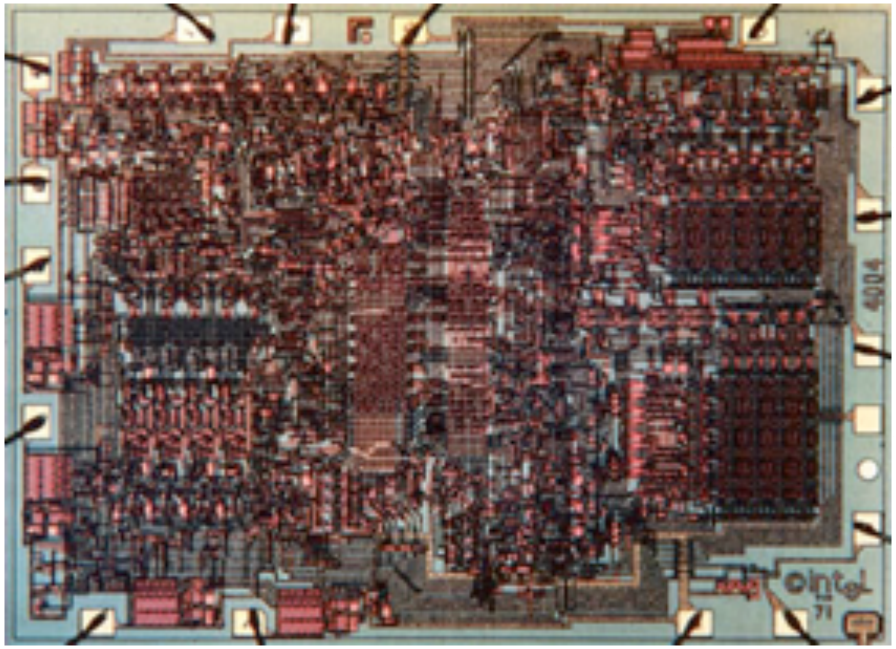

- 😁Everything on one chip
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A sea change for the computer industry

Disintegrate chips into chiplets (2020)

Large *Cost-Effective* SoCs through Disintegration

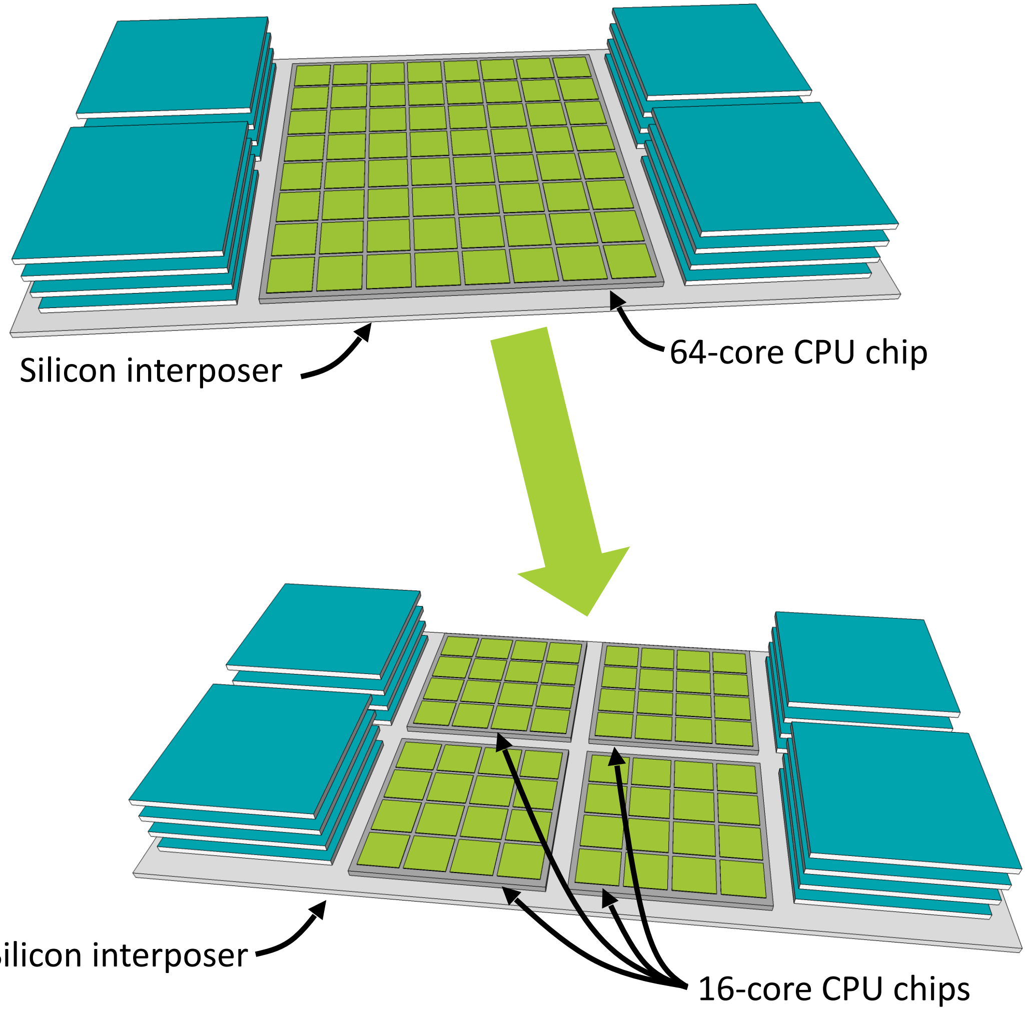
Why disintegrate?

Want more functionality, but…

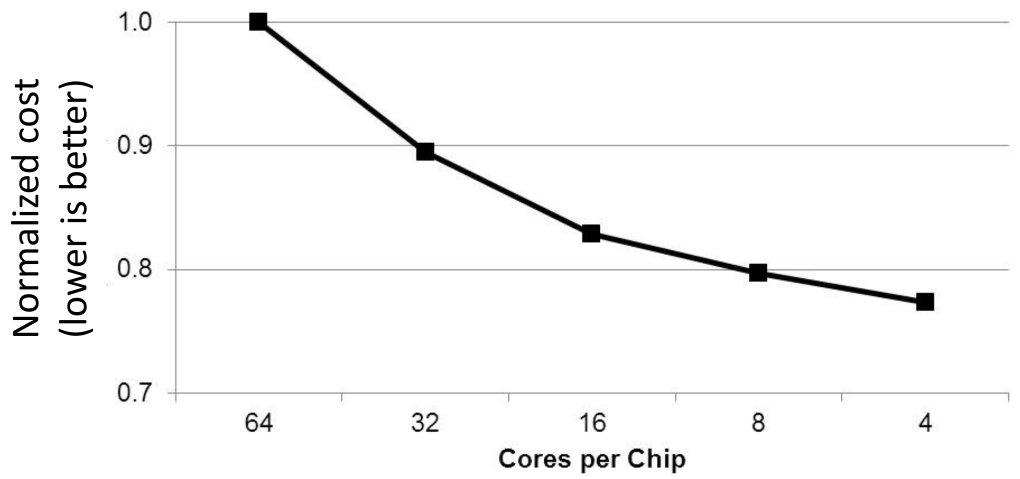
Big chips are expensive

Break (disintegrate) into several smaller pieces

Cheaper to manufacture



Disintegration → Cheaper SoCs



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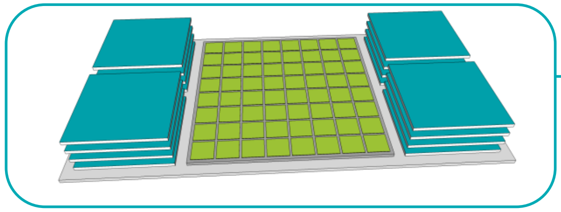

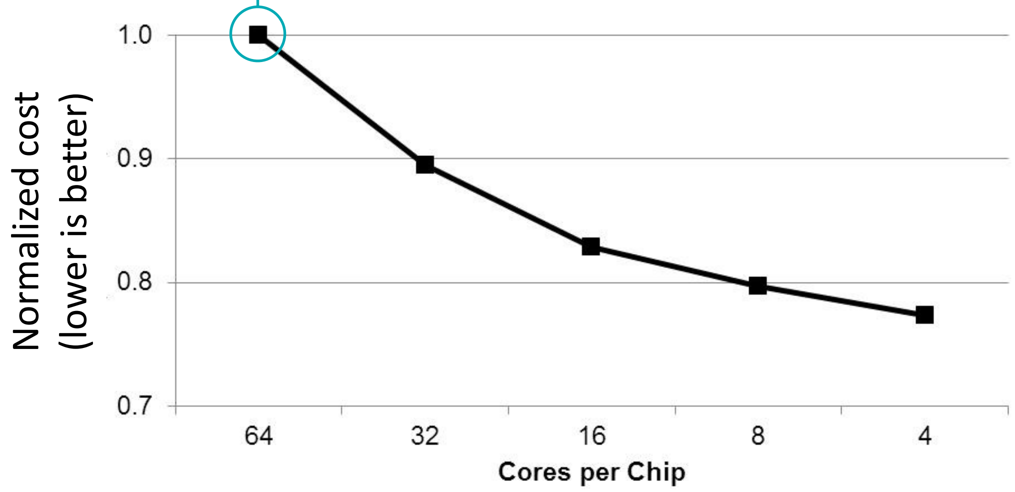

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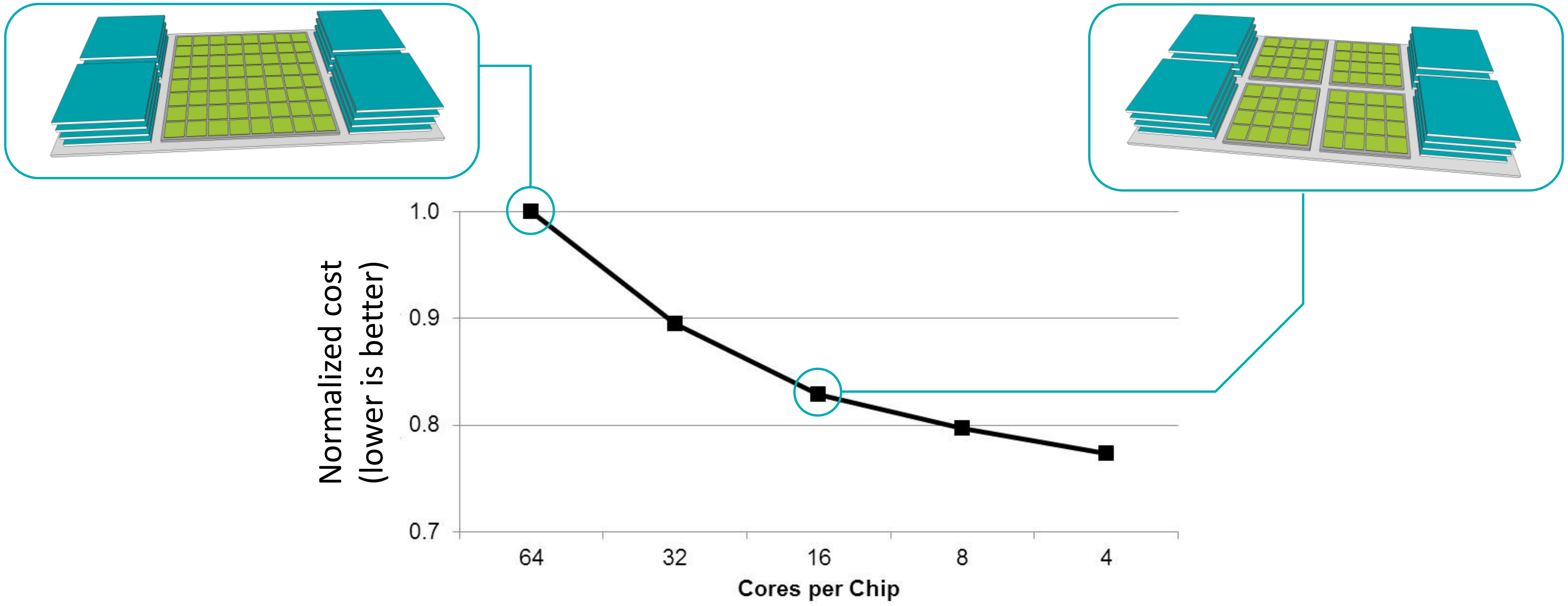

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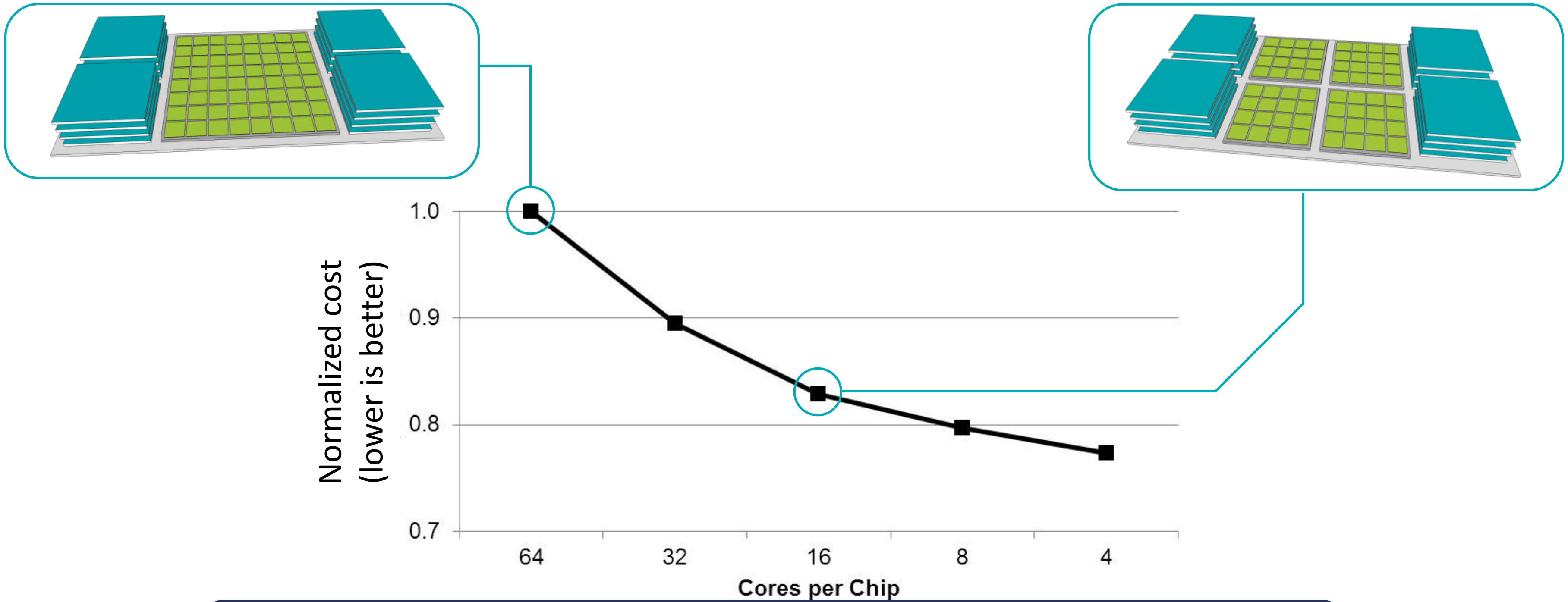
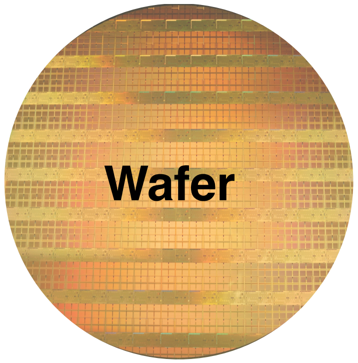


Disintegrated SoCs have potential for reducing costs of large chips while maintaining functionality

Cost Argument: High-Level Idea



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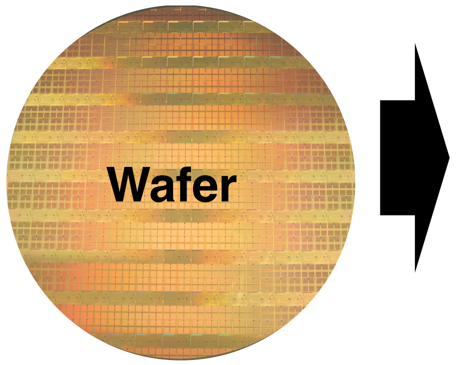

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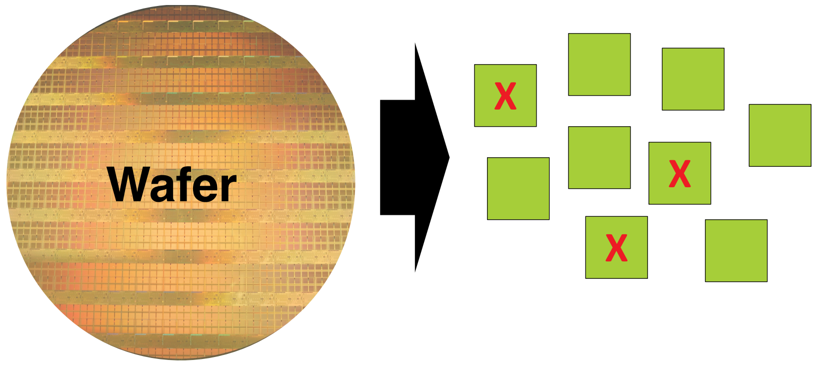

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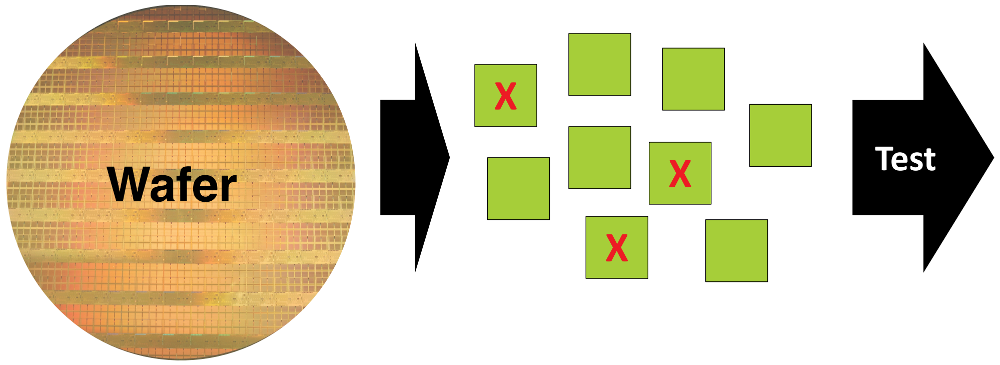

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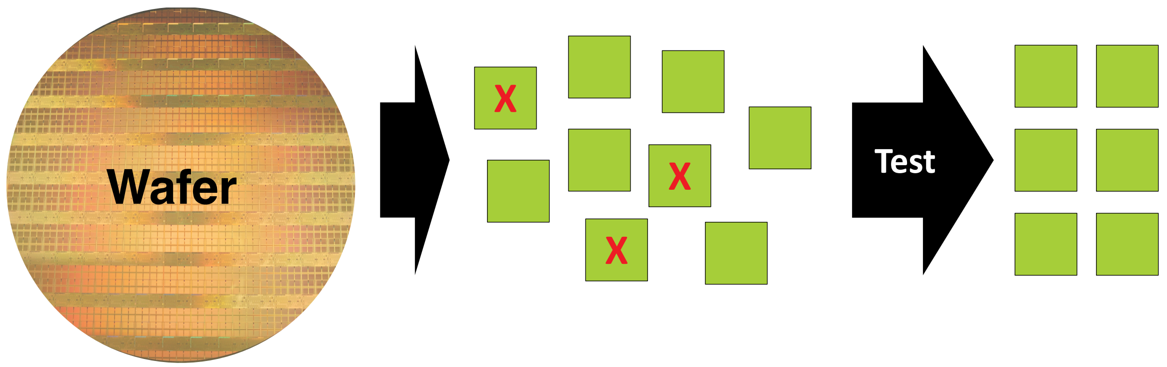

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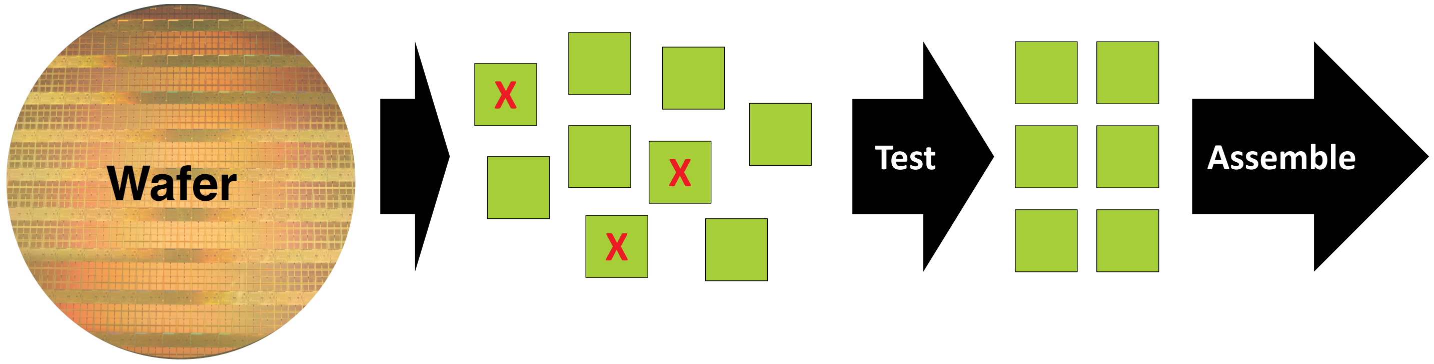

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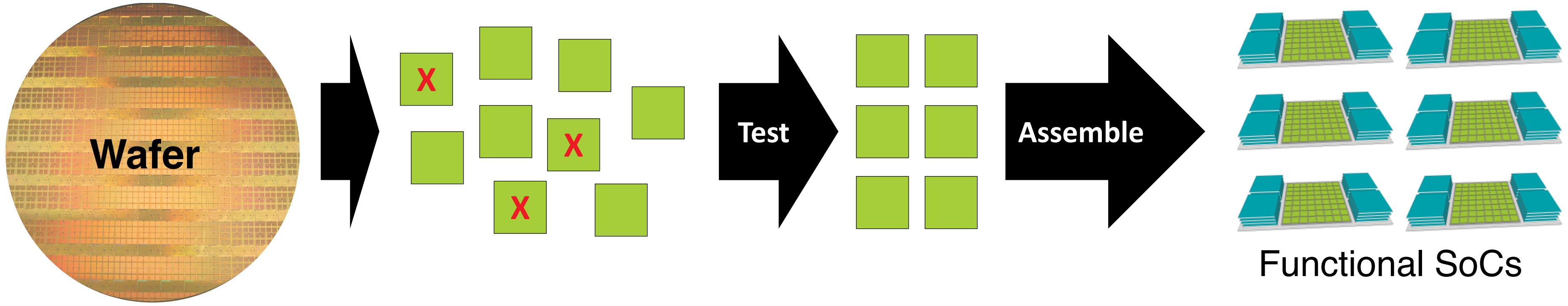

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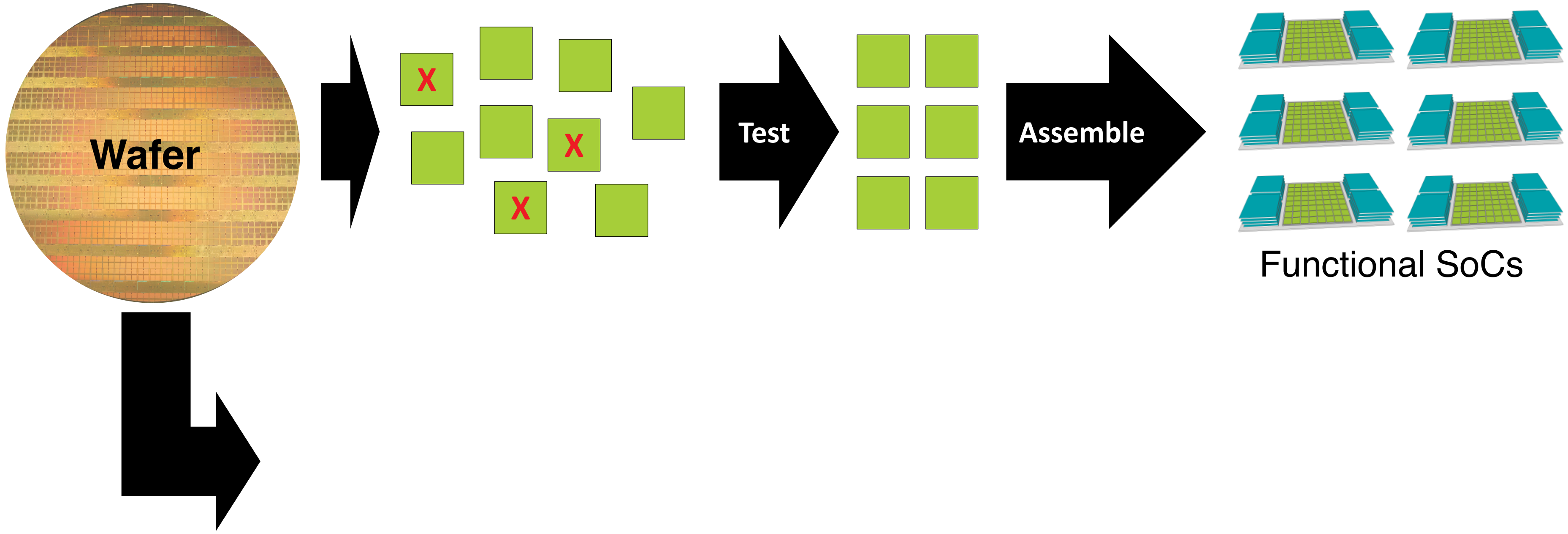

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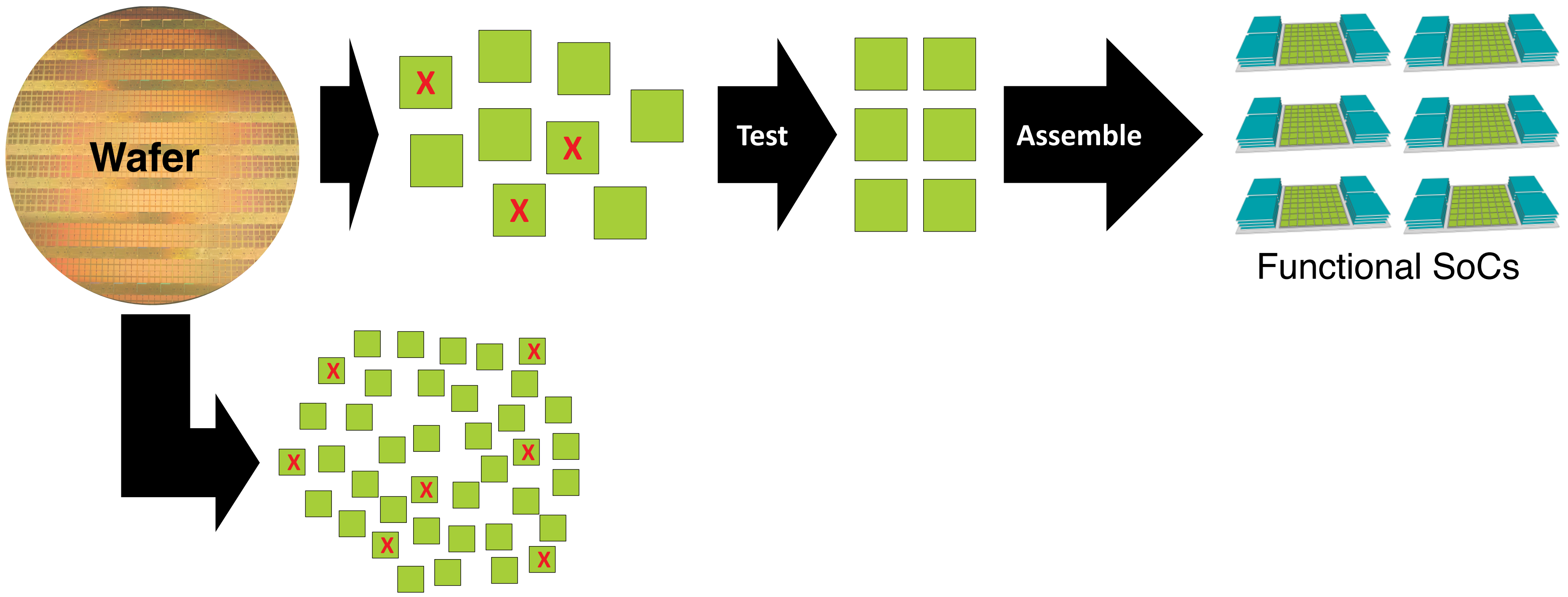

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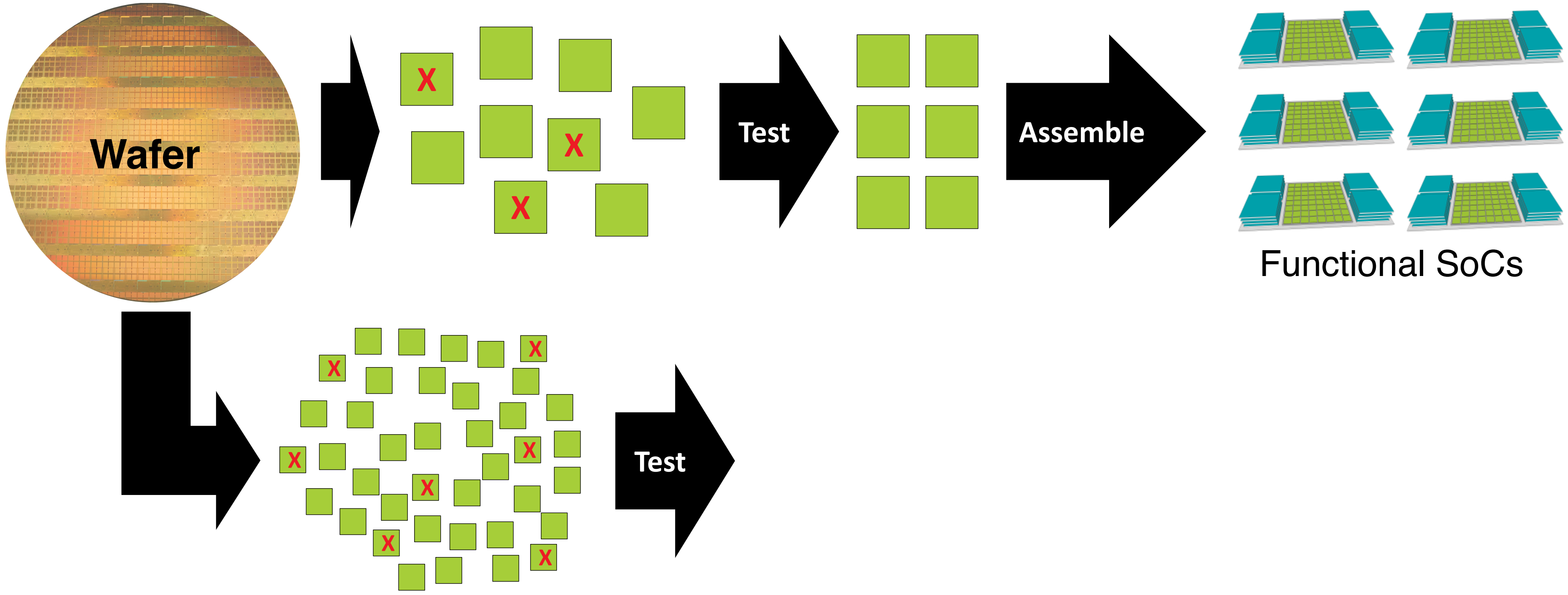

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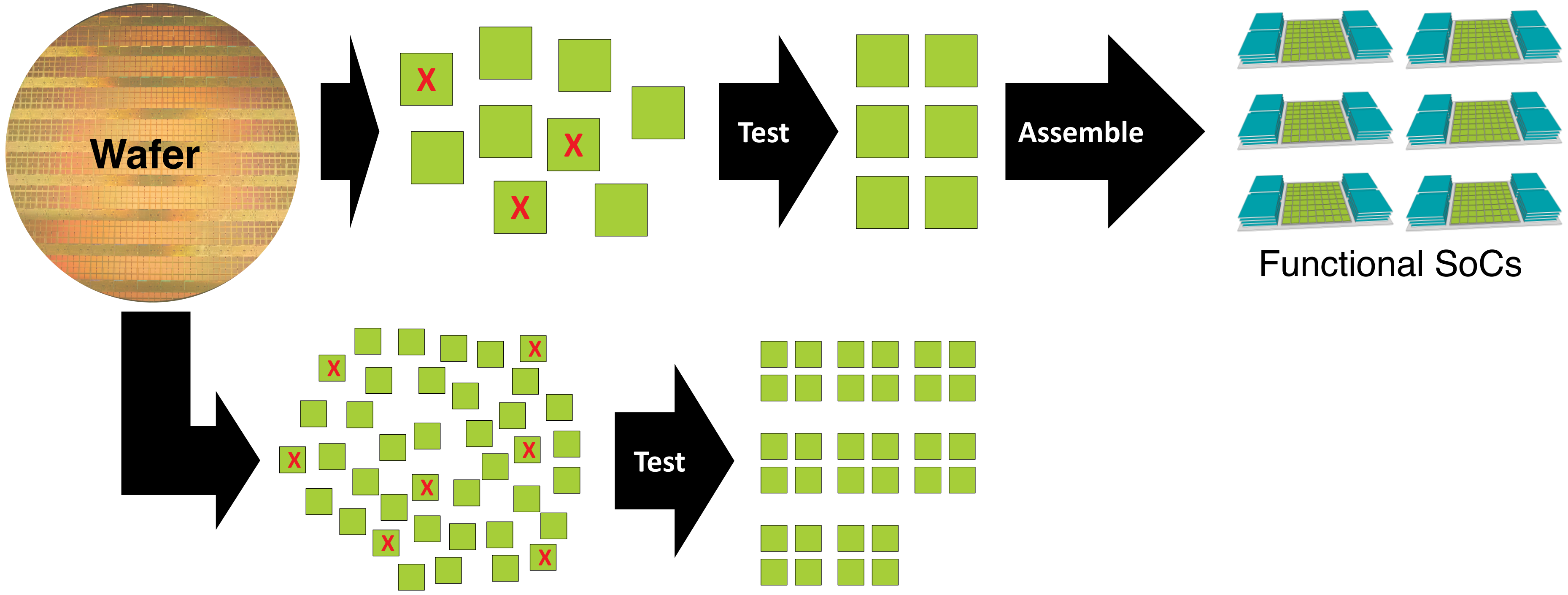

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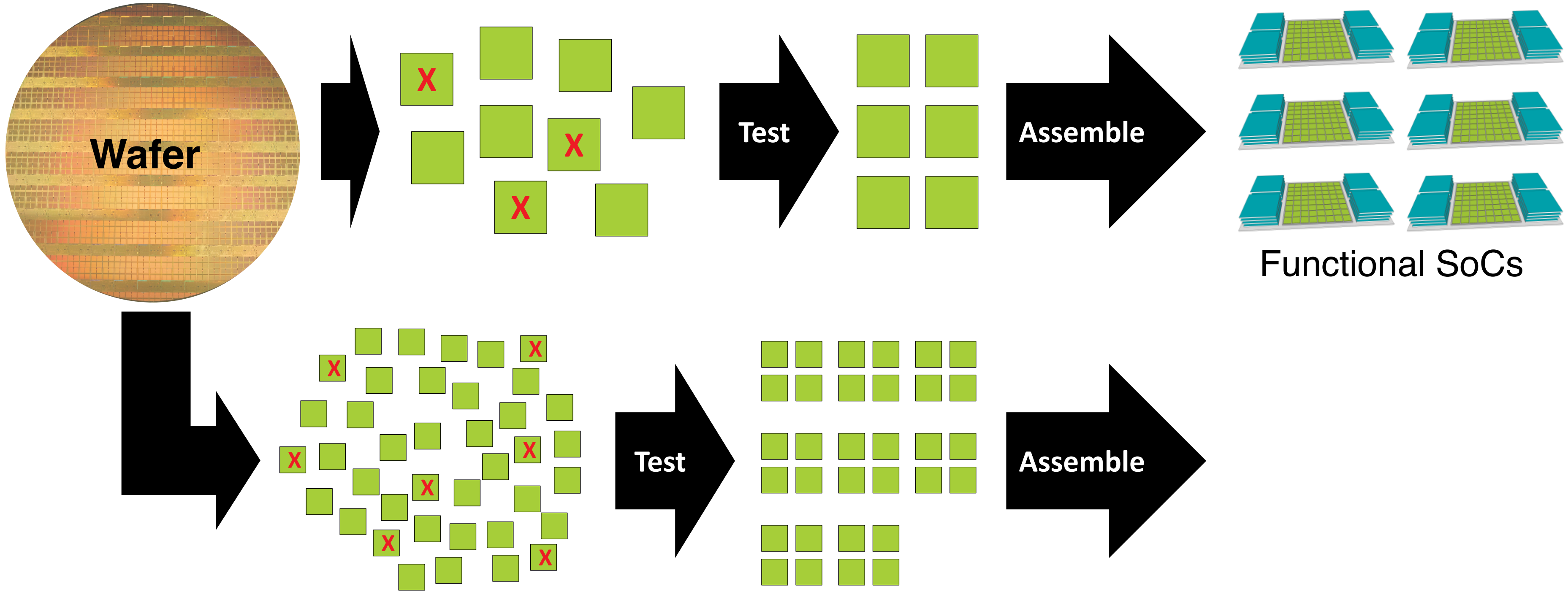

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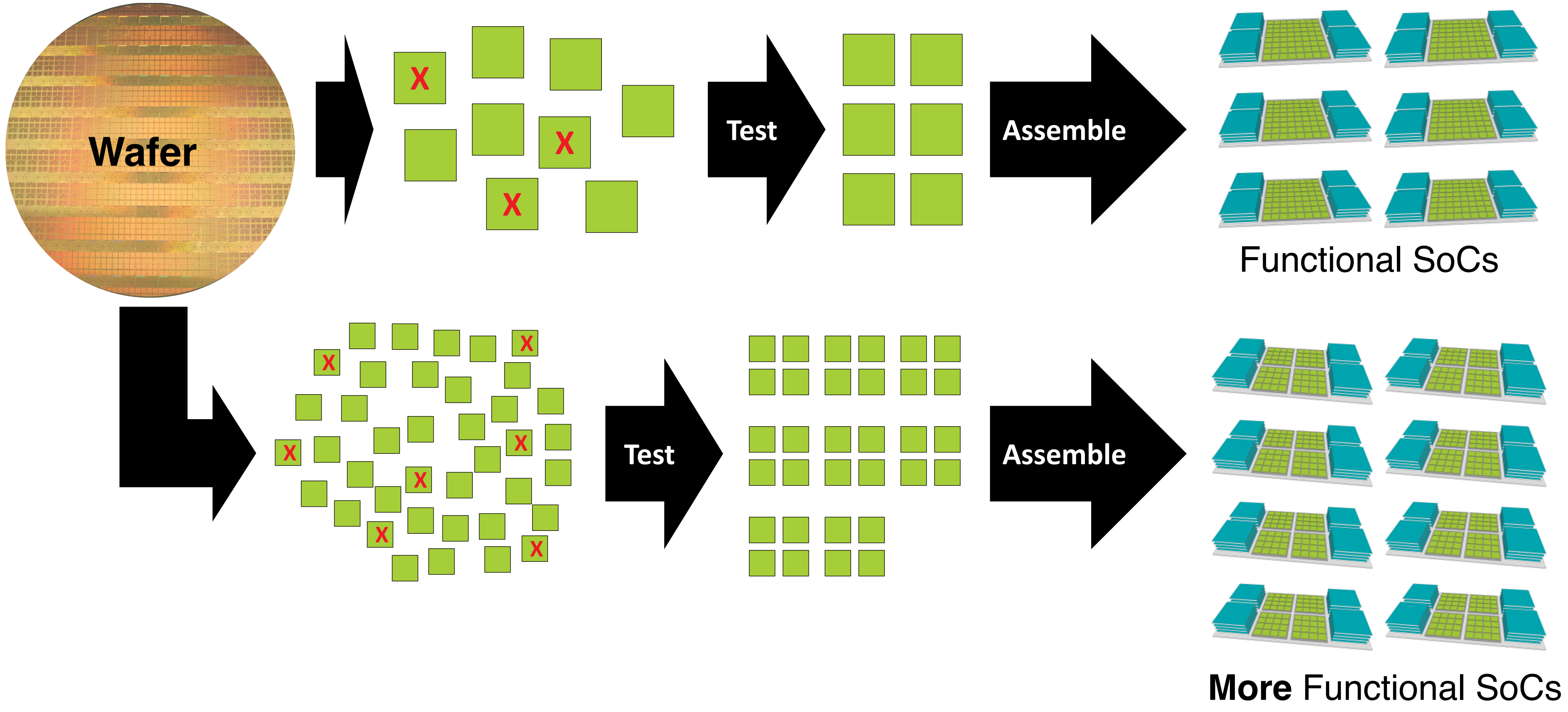

Cheaper Chips + Larger Profit Margins

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Process variations lead to different maximum operating frequencies

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Sort chips before assembly to improve speed binning

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Within die variations hurt performance of large monolithic chips

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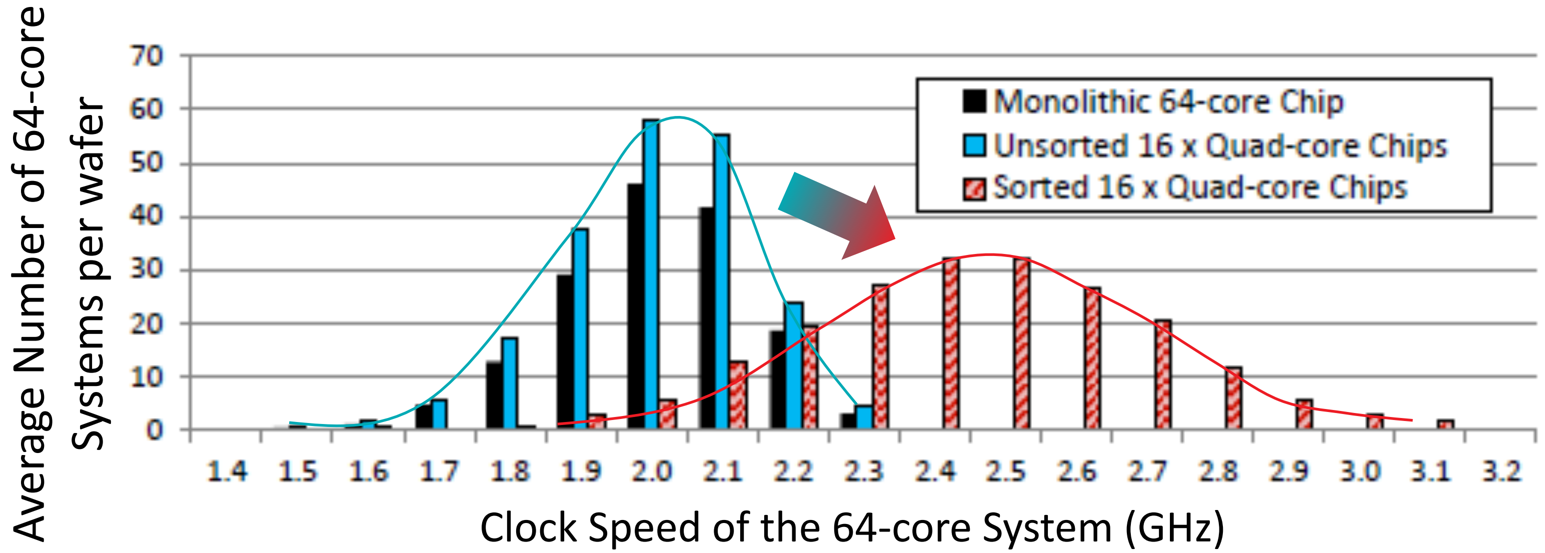
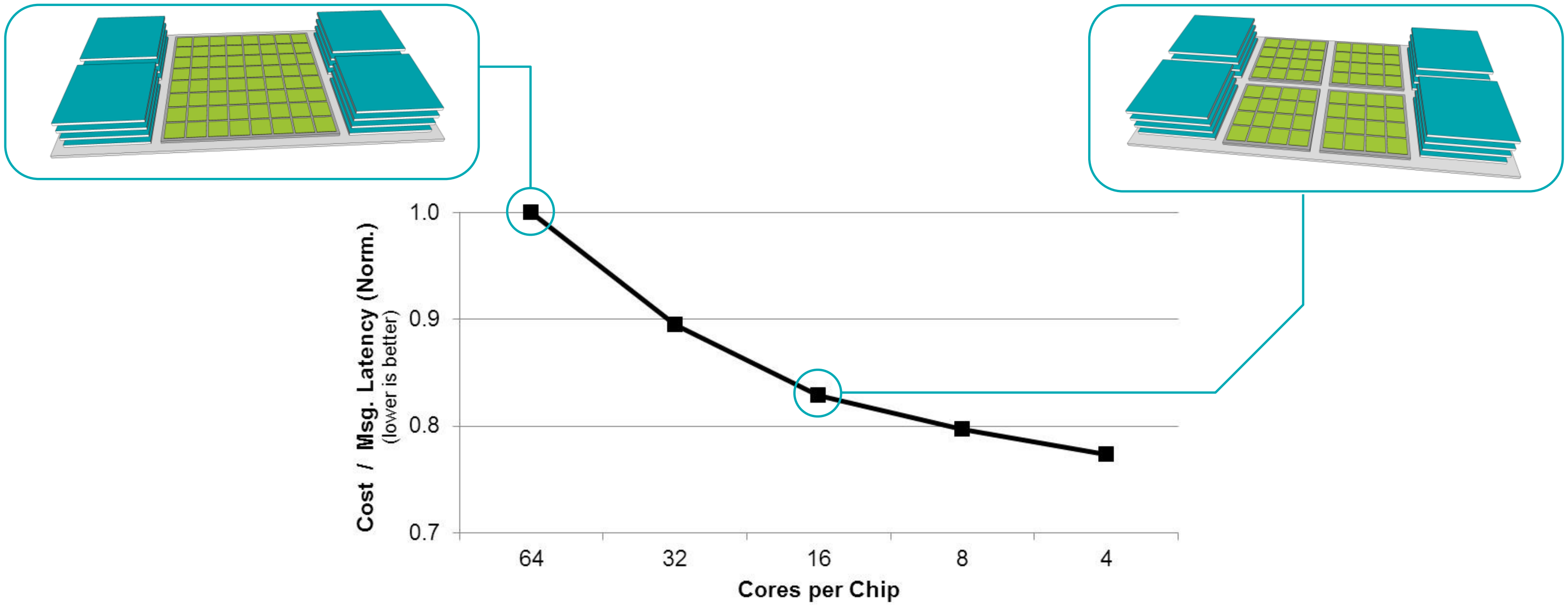
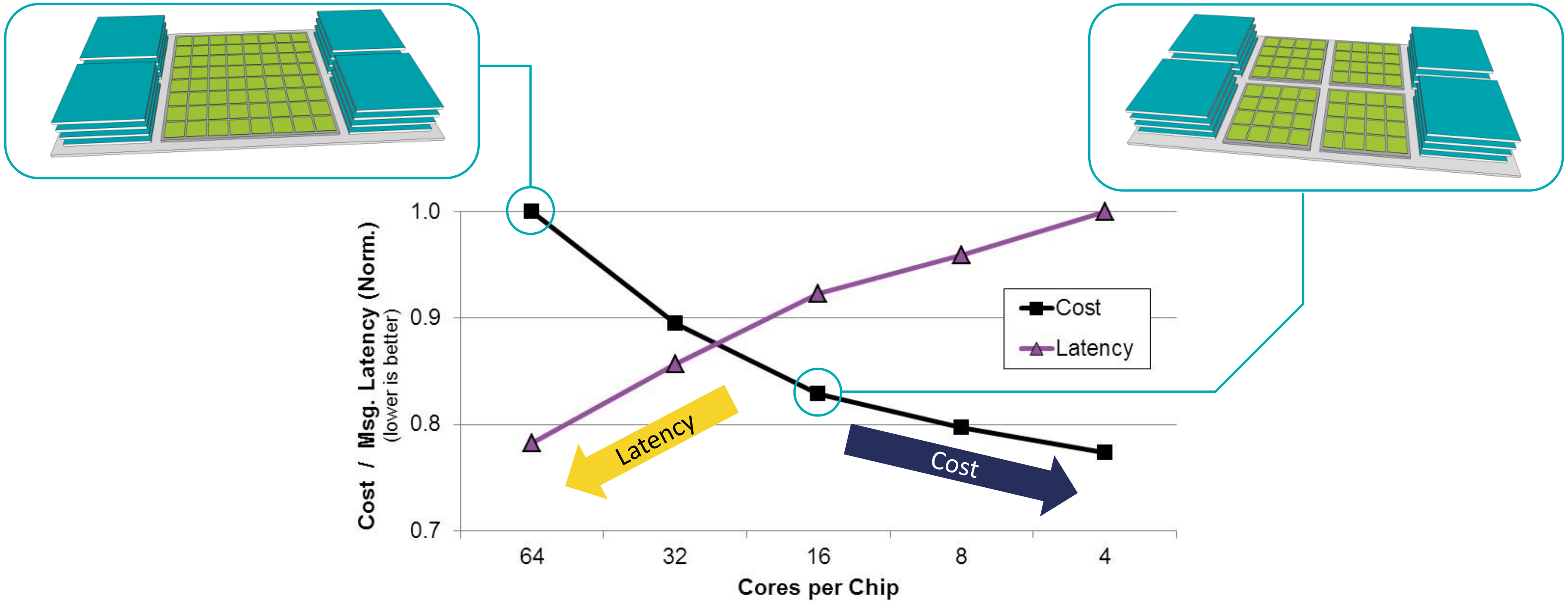


Fragmented Architecture



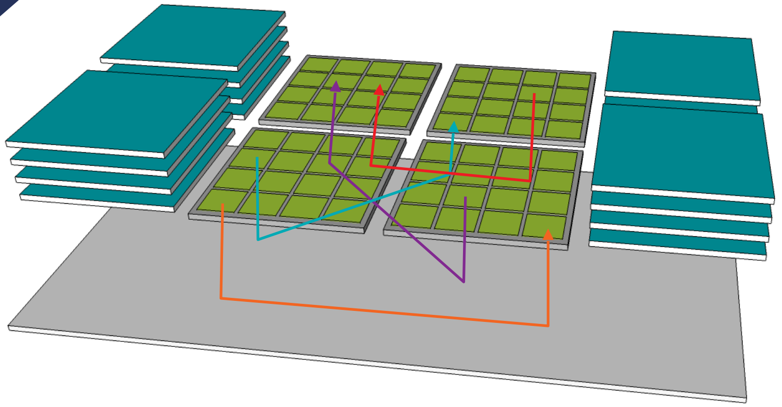
Disintegrated SoCs have potential for reducing costs of large chips

Fragmented Architecture



Disintegrated SoCs have potential for reducing costs of large chips

But performance degrades with disintegration granularity



How to integrate chiplets?

What are we looking for when reintegrating?

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Enable small/simple chiplets

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Enable small/simple chiplets

High bandwidth/low latency connections between chiplets

What are we looking for when reintegrating?

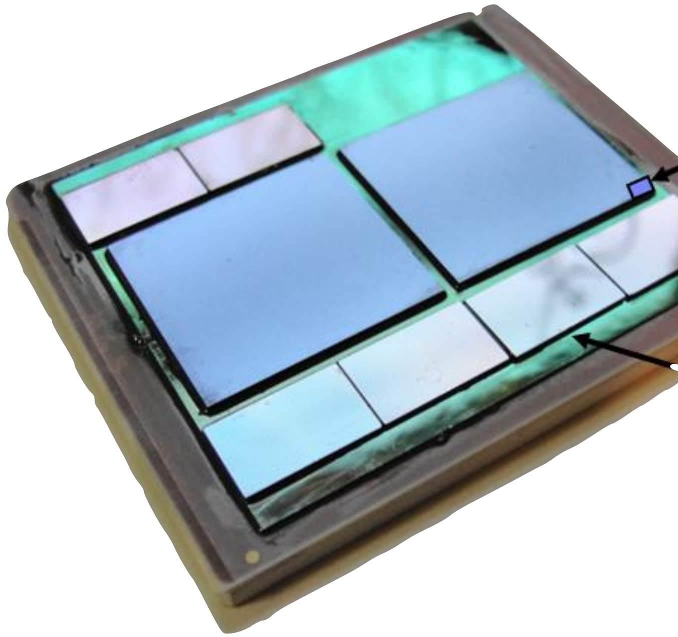
Enable small/simple chiplets

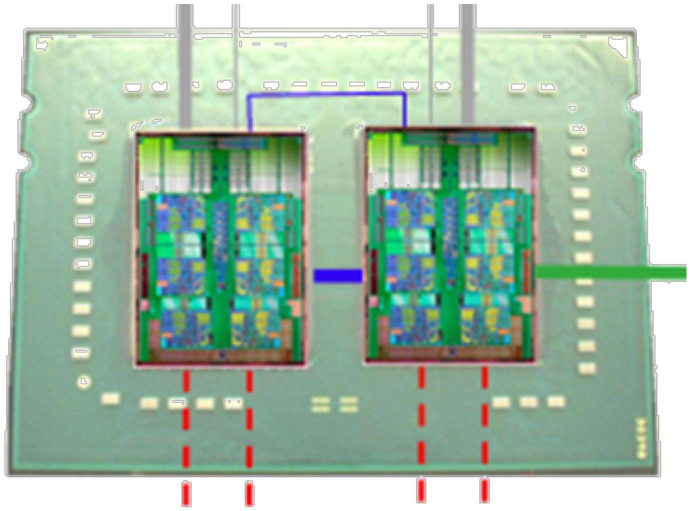
High bandwidth/low latency connections between chiplets

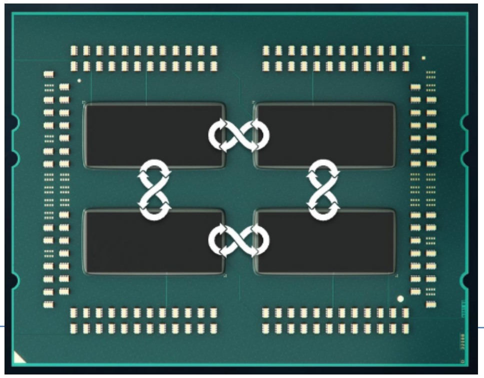
Ease of manufacturing

How to integrate?

Multi-chip modules (MCM)



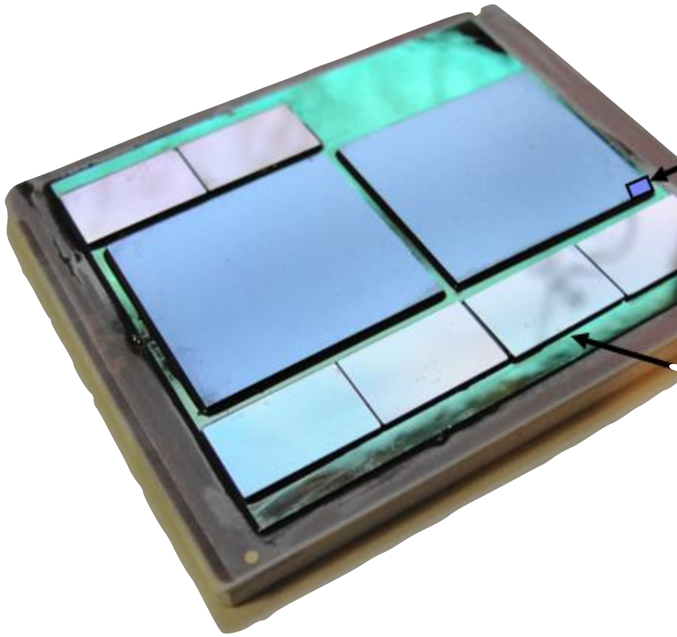


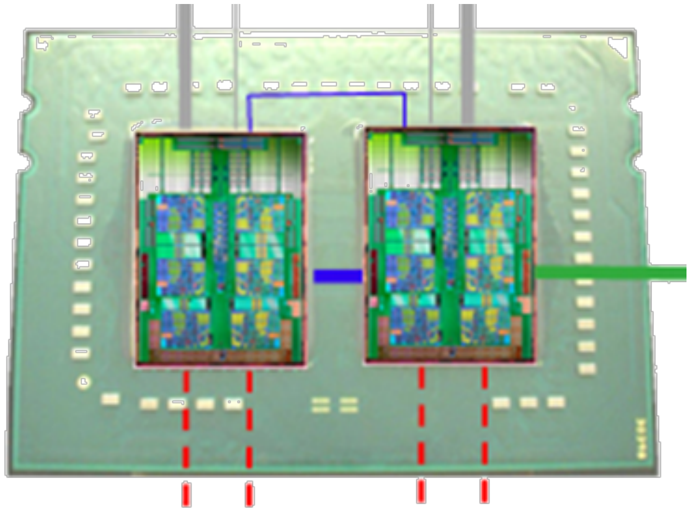


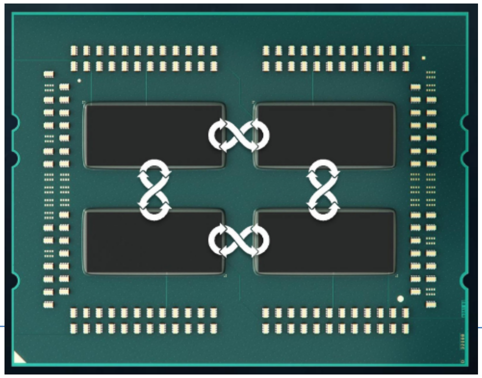
How to integrate?

Multi-chip modules (MCM)

😁 Avoids pin limitations of multi-package solutions



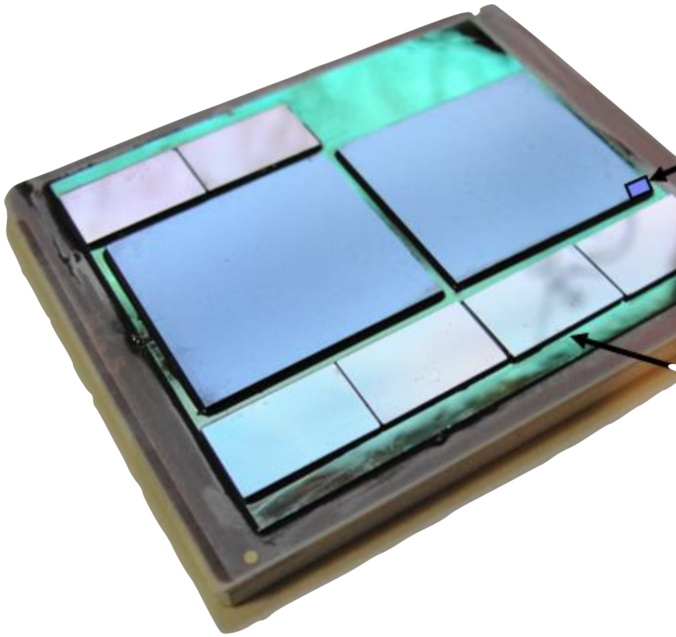


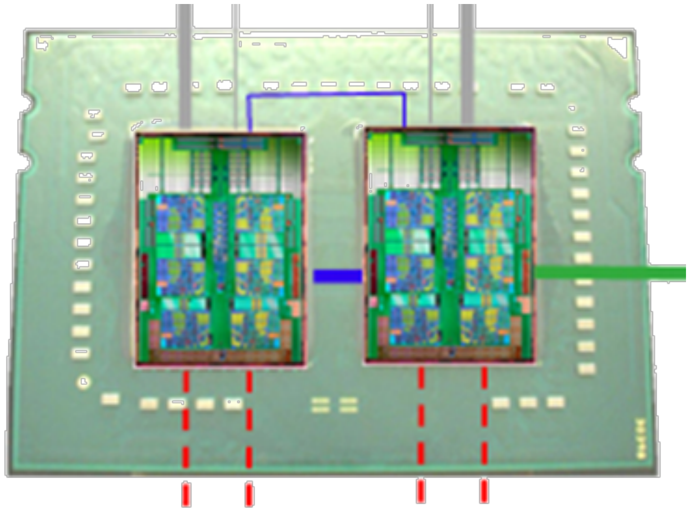


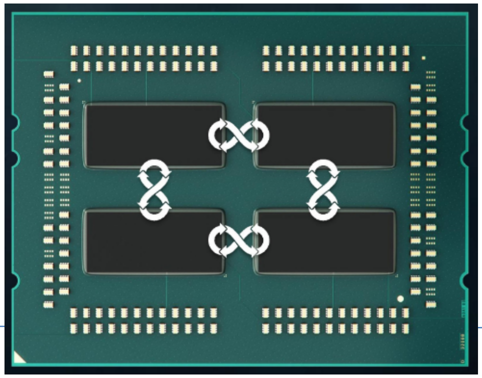
How to integrate?

Multi-chip modules (MCM)

- 😁 Avoids pin limitations of multi-package solutions
- 😢 Bandwidth/Latency constraints of C4 bumps and substrate



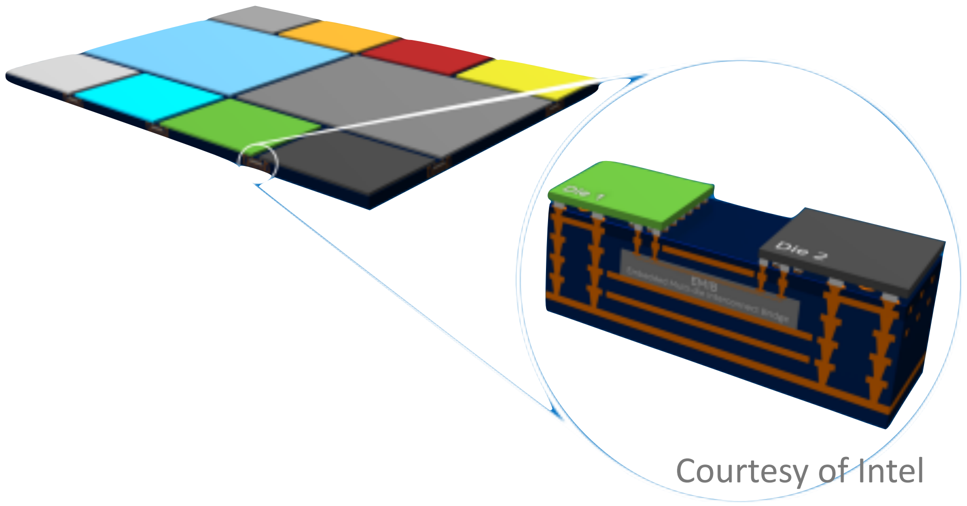




How to integrate?

Multi-chip modules (MCM)

Embedded Multi-Chip Interconnect Bridge (EMIB)



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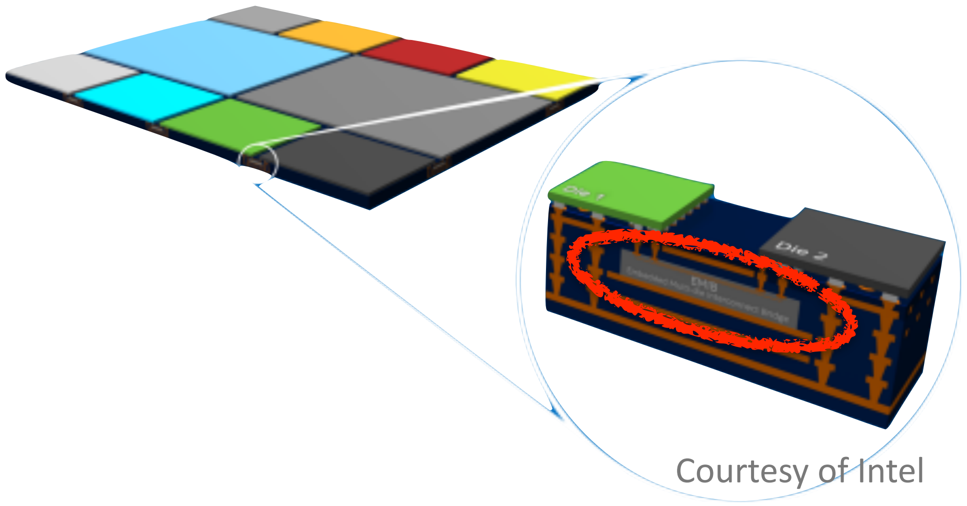

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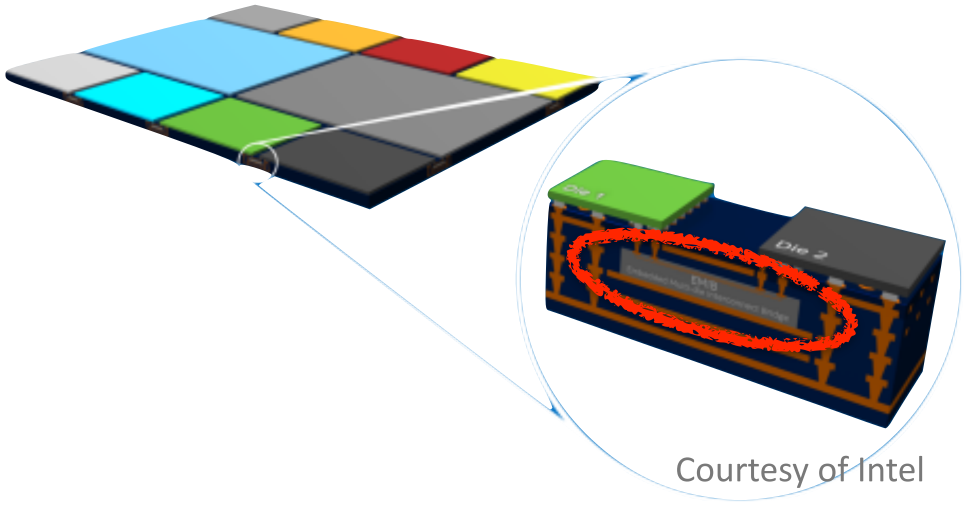
- 😁 Small/simple chiplets



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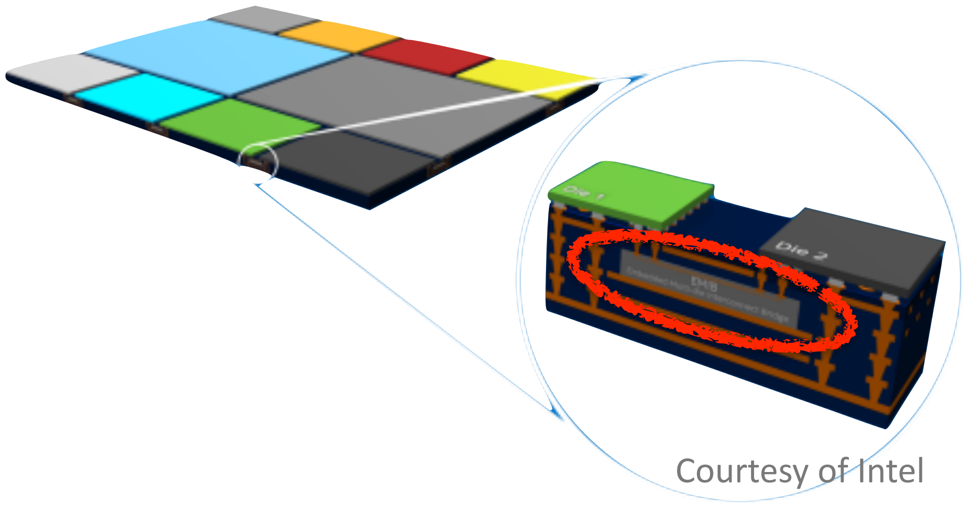
- 😁 Small/simple chiplets
- 😁 Small bridge die



Courtesy of Intel

How to integrate?

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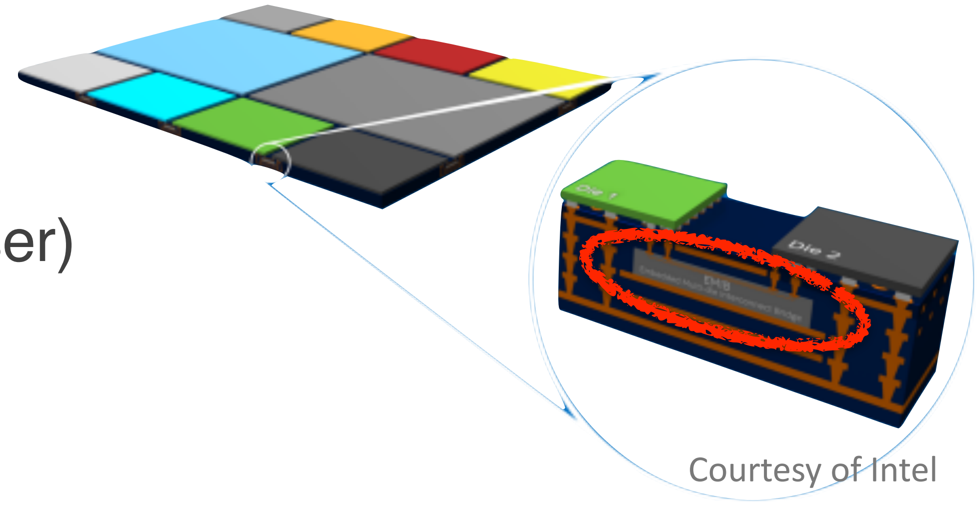
- 😁 Avoids large die (interposer)



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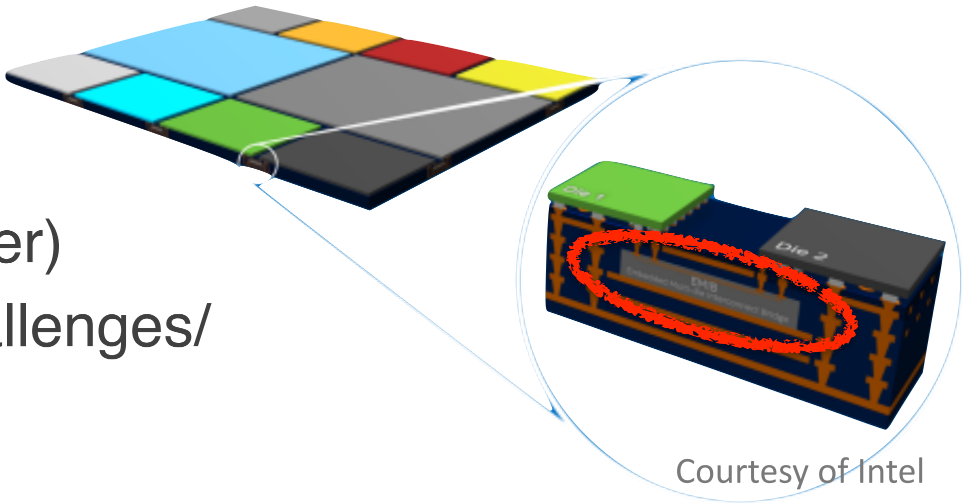

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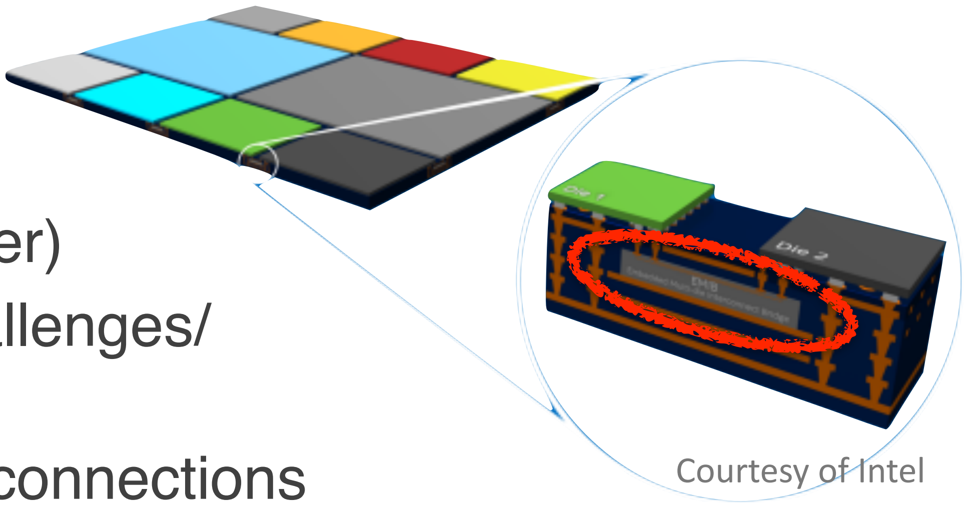


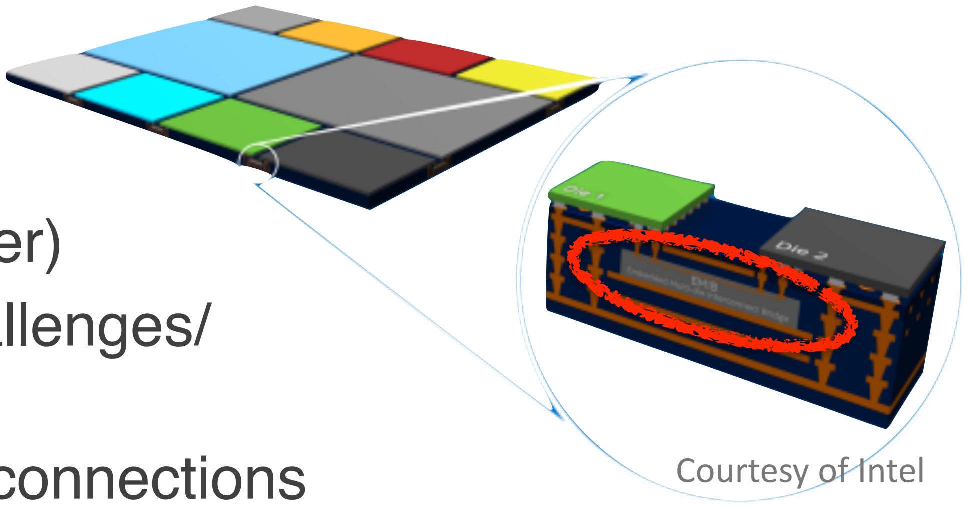
Courtesy of Intel

How to integrate?

Multi-chip modules (MCM)

Embedded Multi-Chip Interconnect Bridge (EMIB)

- 😁 Small/simple chiplets
- 😁 Small bridge die
- 😁 Avoids large die (interposer)
- 😁 Avoids manufacturing challenges/ costs
- 😢 Only offers point-to-point connections
- 😢 Misses opportunity to offload some functionality to interposer



Courtesy of Intel

How to integrate?

Multi-chip modules (MCM)

Embedded Multi-Chip Interconnect Bridge (EMIB)

Silicon Interposer (2.5D)

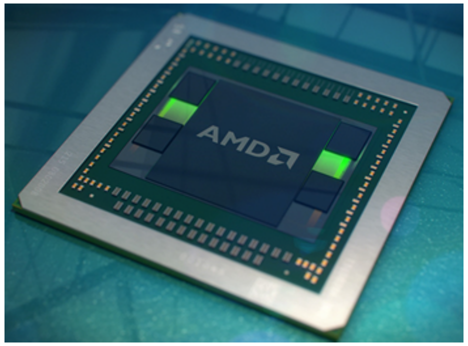
How to integrate?

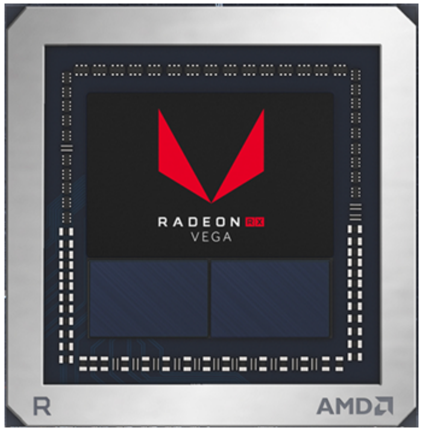
Multi-chip modules (MCM)

Embedded Multi-Chip Interconnect Bridge (EMIB)

Silicon Interposer (2.5D)

- 😁 Technology maturation (high volume passive interposer production — 3 years)





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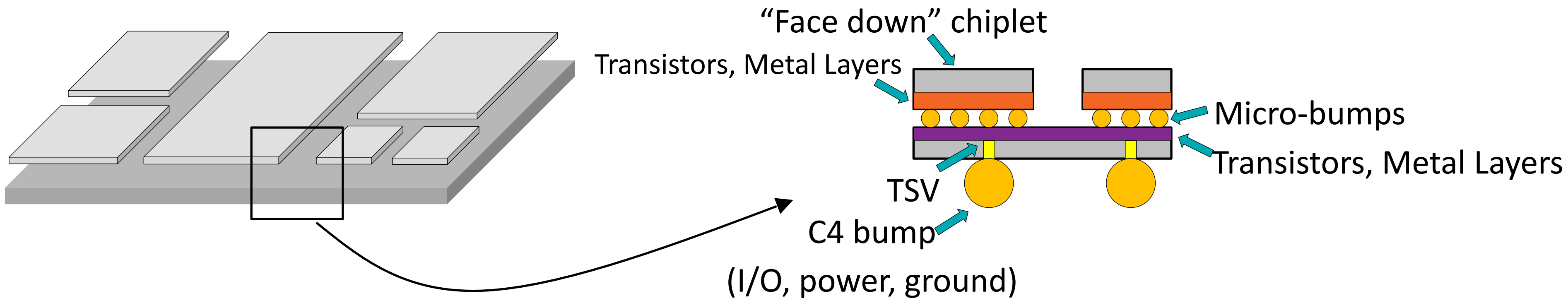

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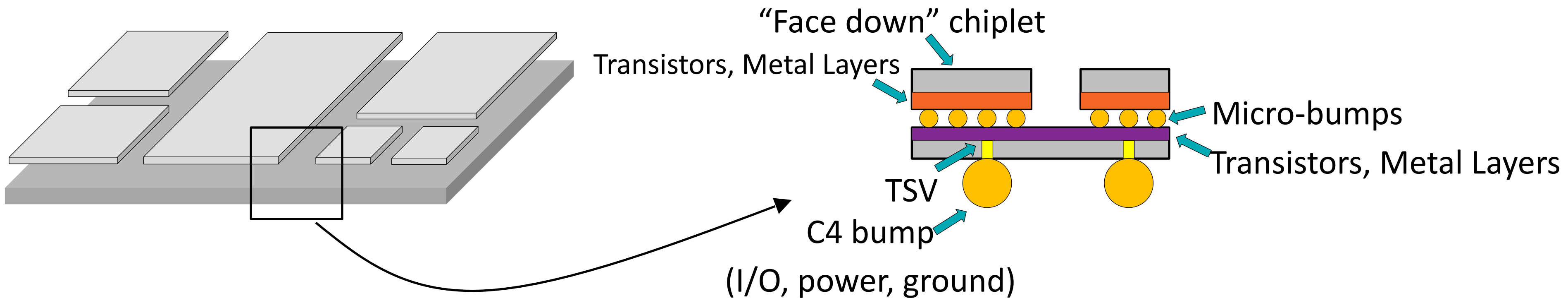
- 😁 Simple, small chiplets



How to integrate?

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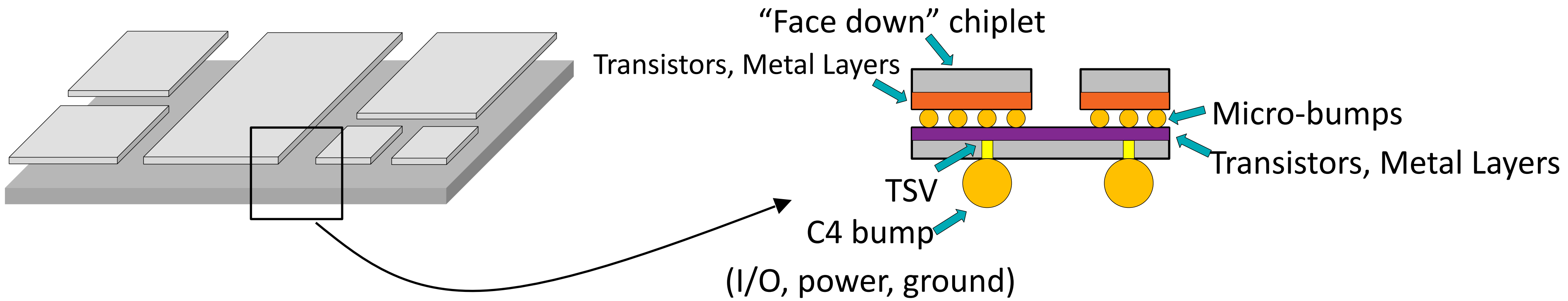
Active Silicon Interposer (2.5D)

- 😁 Simple, small chiplets
- 😁 Move SoC functionality into interposer



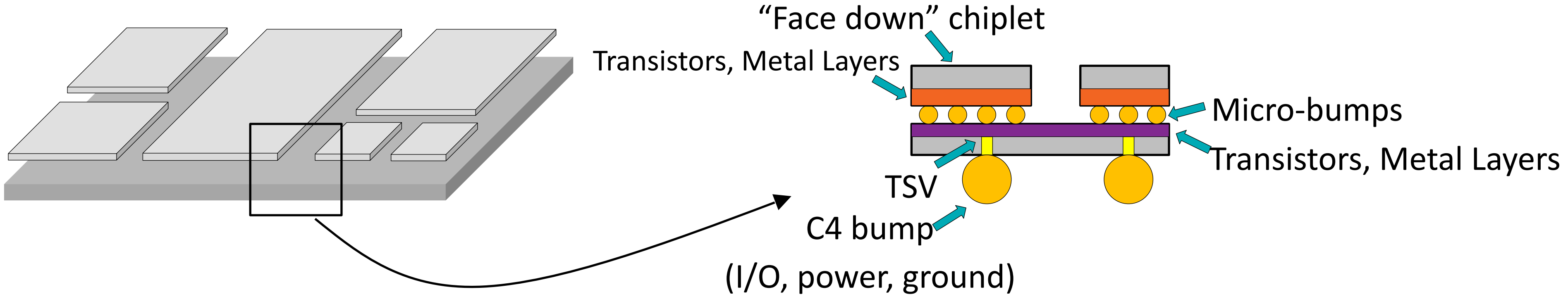
How to integrate?

Multi-chip modules (MCM)

Embedded Multi-Chip Interconnect Bridge (EMIB)

Active Silicon Interposer (2.5D)

- 😁 Simple, small chiplets
- 😁 Move SoC functionality into interposer
- 😁 Implement in older technology node



Interposers: An enabling integration technology

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Facilitates modular SoC design

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But what about…

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Facilitates modular SoC design

But what about…

- Cost — Aren't interposers expensive?

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But what about…

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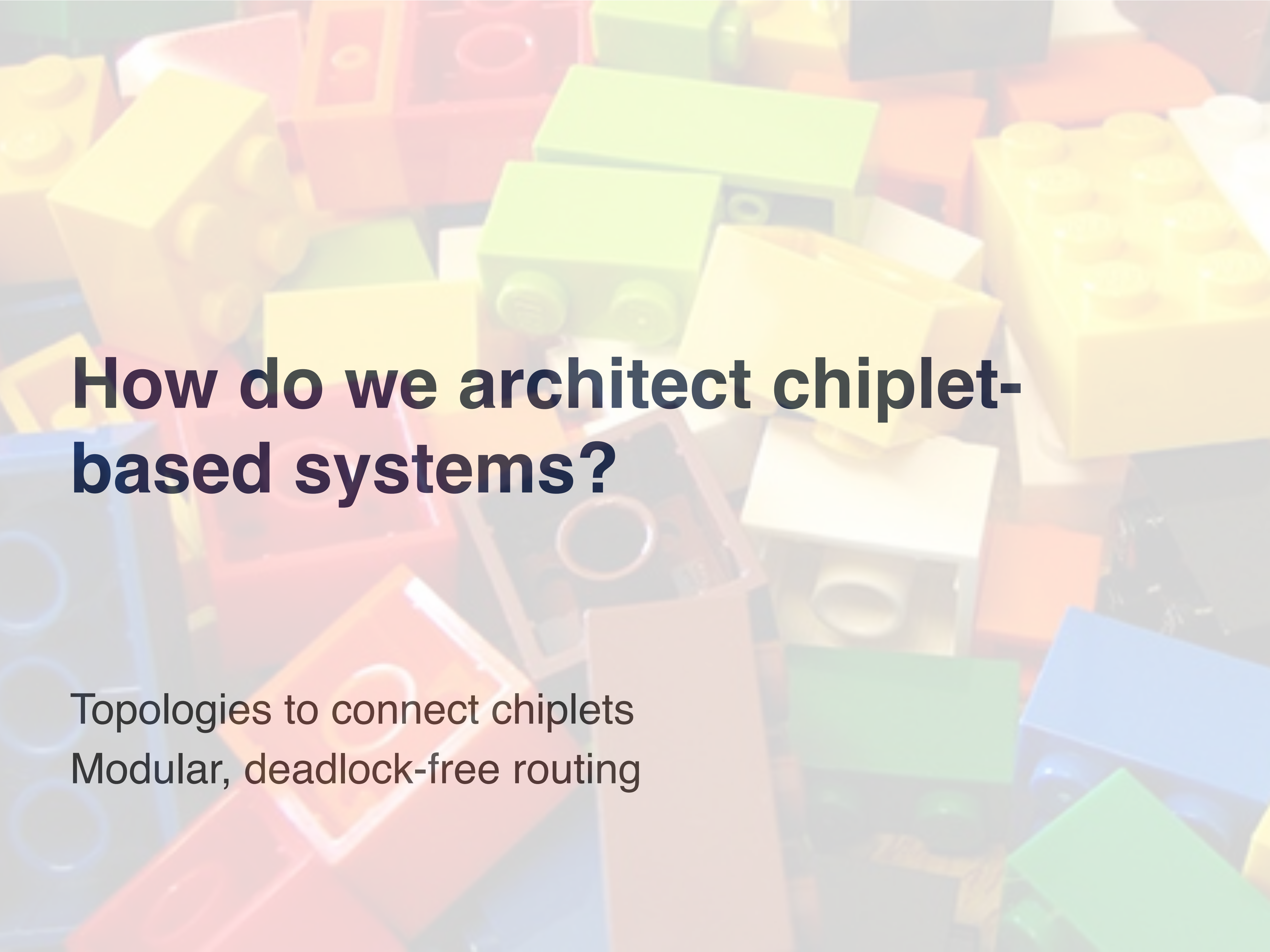
- Communication — How do we reintegrate?

Interposers: An enabling integration technology

Facilitates modular SoC design

But what about…

- Cost — Aren’t interposers expensive?
- Communication — How do we reintegrate?
- How to maximize modularity while reintegrating?

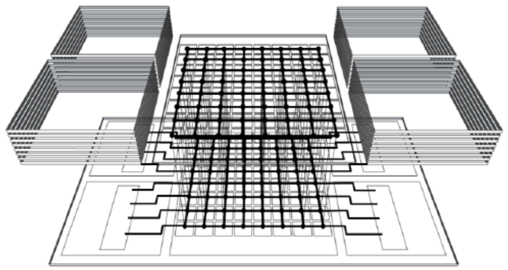


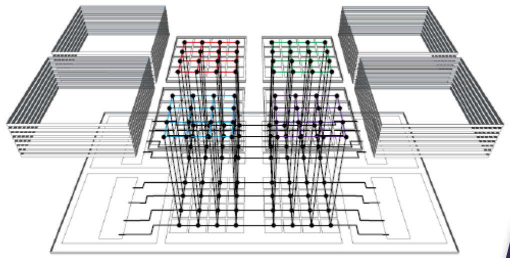
How do we architect chiplet-based systems?

Topologies to connect chiplets

Modular, deadlock-free routing

Network-on-Chip on Interposer to Reintegrate

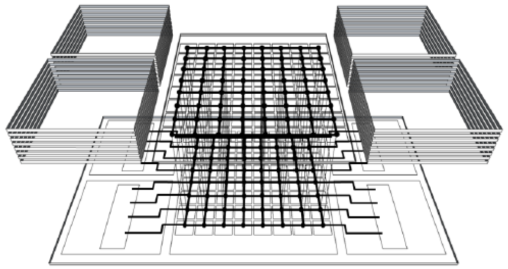


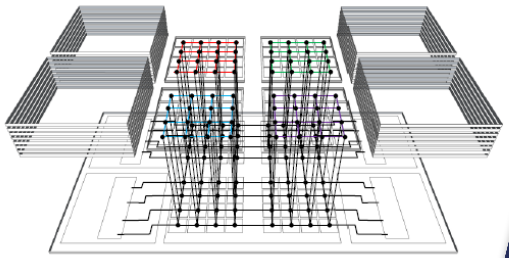


Q1: How do you build a NoC on the interposer?

Q2: What type of NoC should you build?

Network-on-Chip on Interposer to Reintegrate

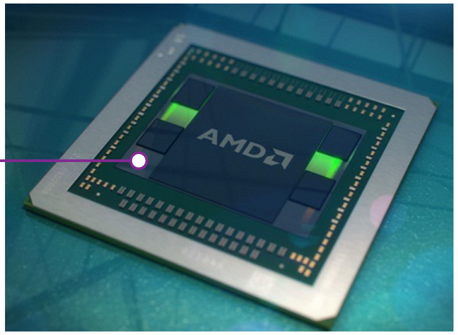




Q1: How do you build a NoC on the interposer?

Q2: What type of NoC should you build?

Q1: … current interposers are passive!



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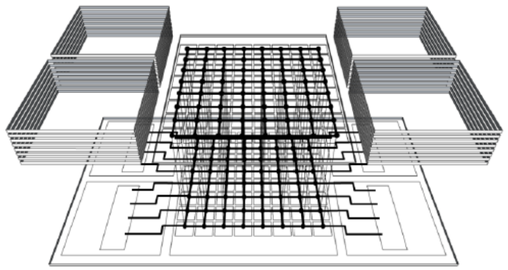

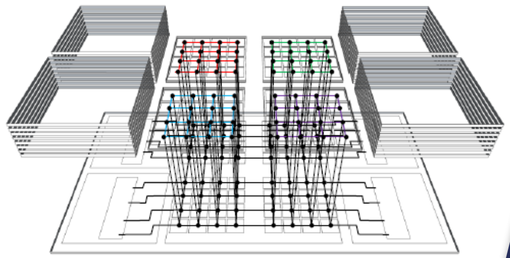

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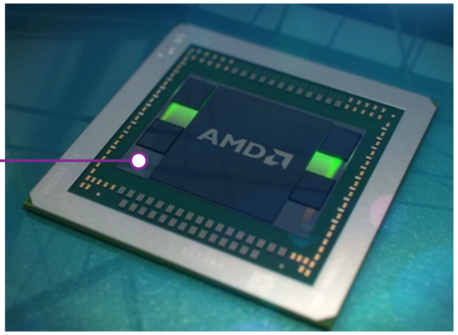
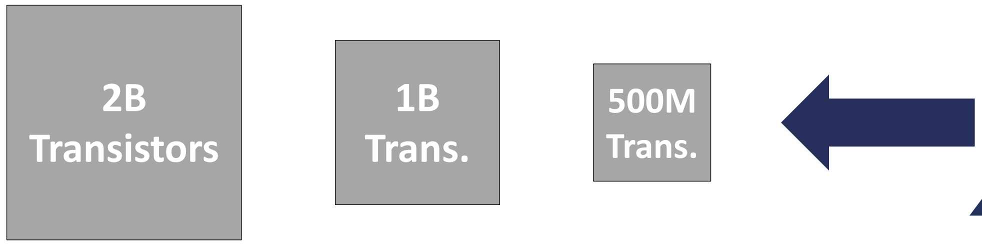


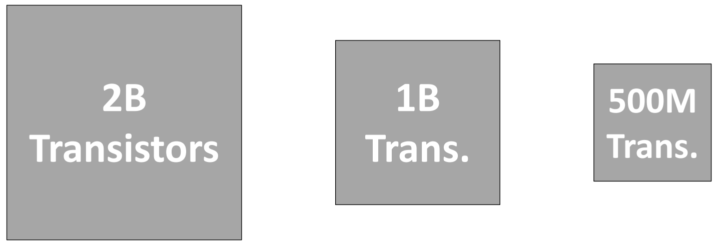
An active interposer is a huge chip, which should have horrible yield, no?!?

Minimally Active Interposers



Conventional chips:
Fewer transistors → smaller chip

Minimally Active Interposers



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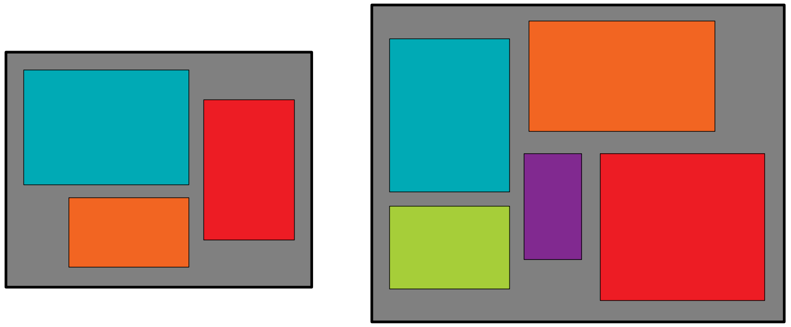
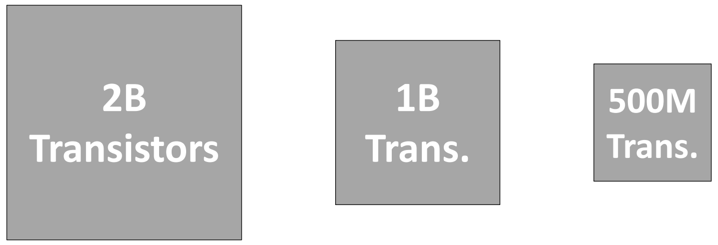


Interposer size depends on chips stacked on top of it

Minimally Active Interposers



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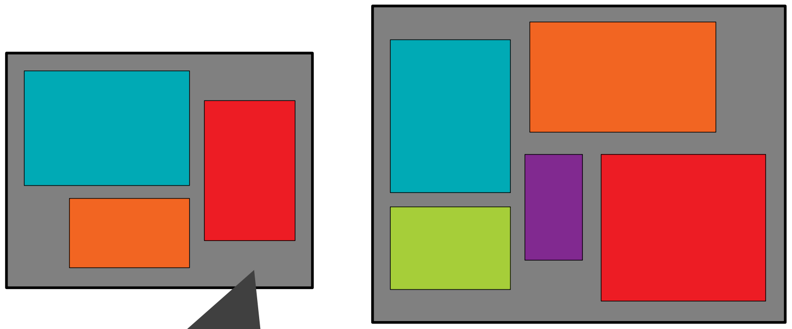
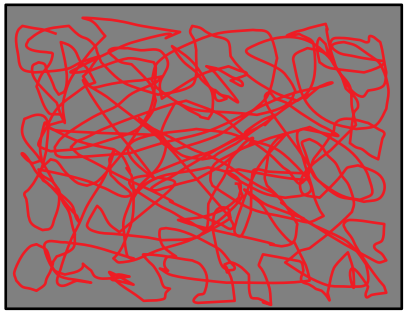
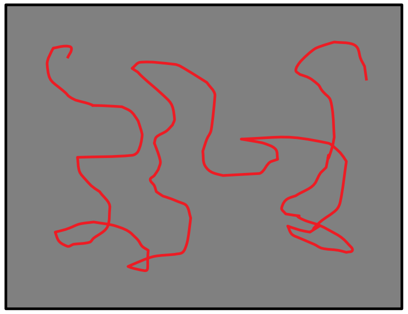


Interposer size depends on chips stacked on top of it

Zero or billion transistors, interposer size is the same

Minimally Active Interposers





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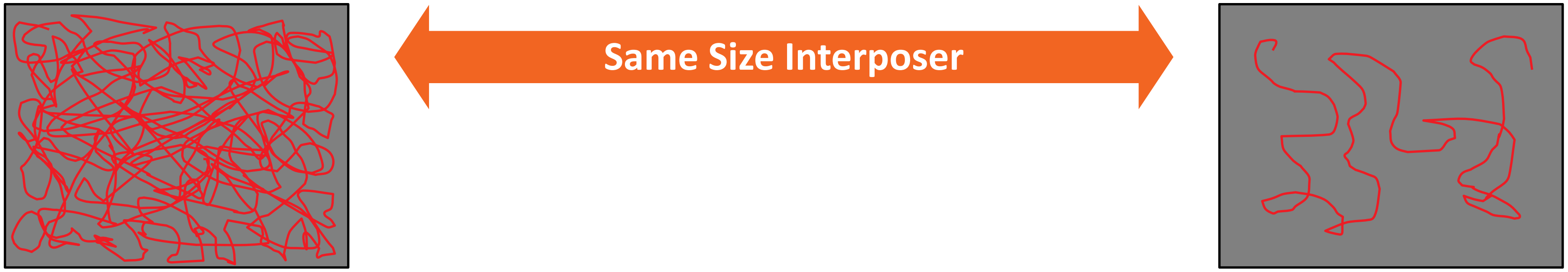

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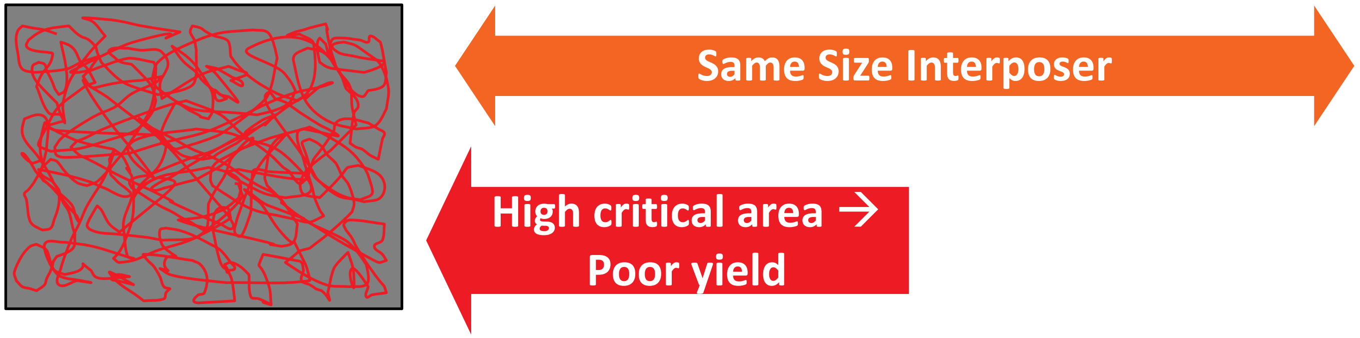

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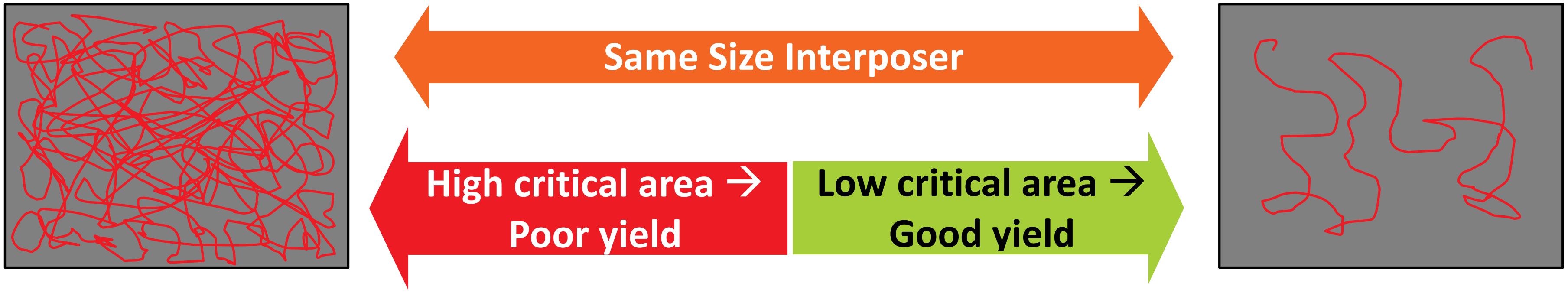
Same Size Interposer
High critical area → Poor yield
Low critical area → Good yield

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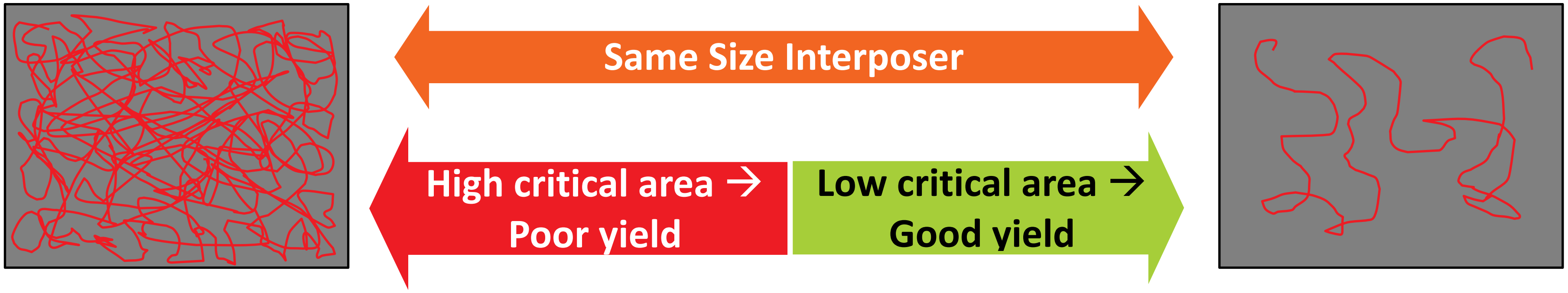
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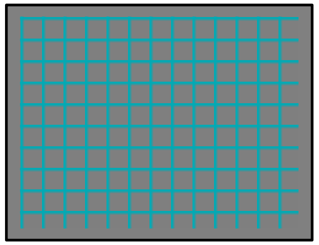
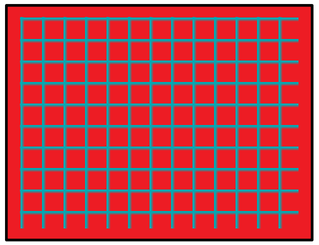
Chip yield impacted by defects in ***critical areas*** (e.g., contaminant in white space is fine)

Minimally Active Interposers for Large SoCs

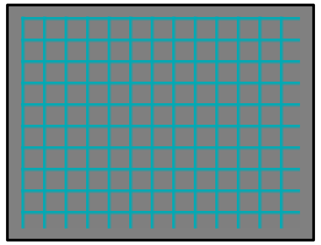


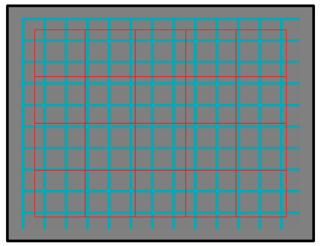


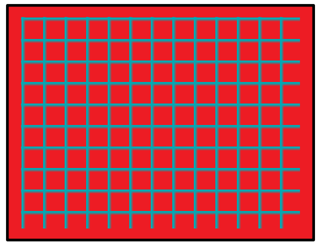
	24mm x 36mm interposer		
Defect Density	**Low**	**Medium**	**High**
Passive Interposer	98.5%	95.5%	92.7%
Active Interposer 1%	98.4%	95.4%	92.5%
Active Interposer 10%	98.0%	94.2%	90.7%
Fully-Active Interposer	87.2%	68.5%	55.6%

*Modelled, not real yield rates

Minimally Active Interposers for Large SoCs







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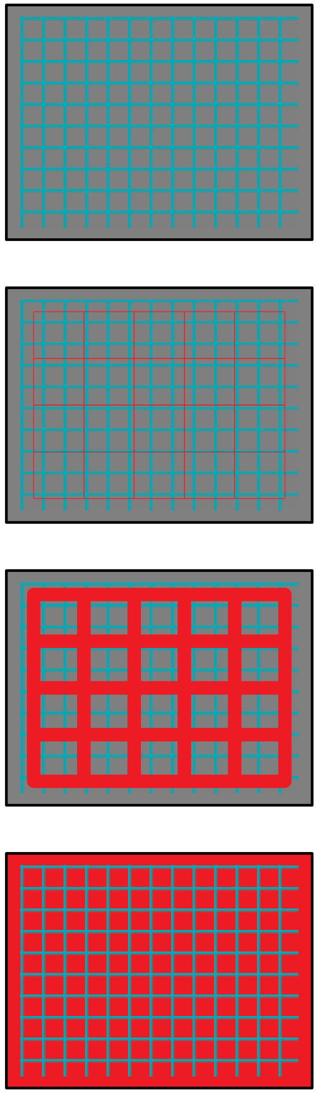

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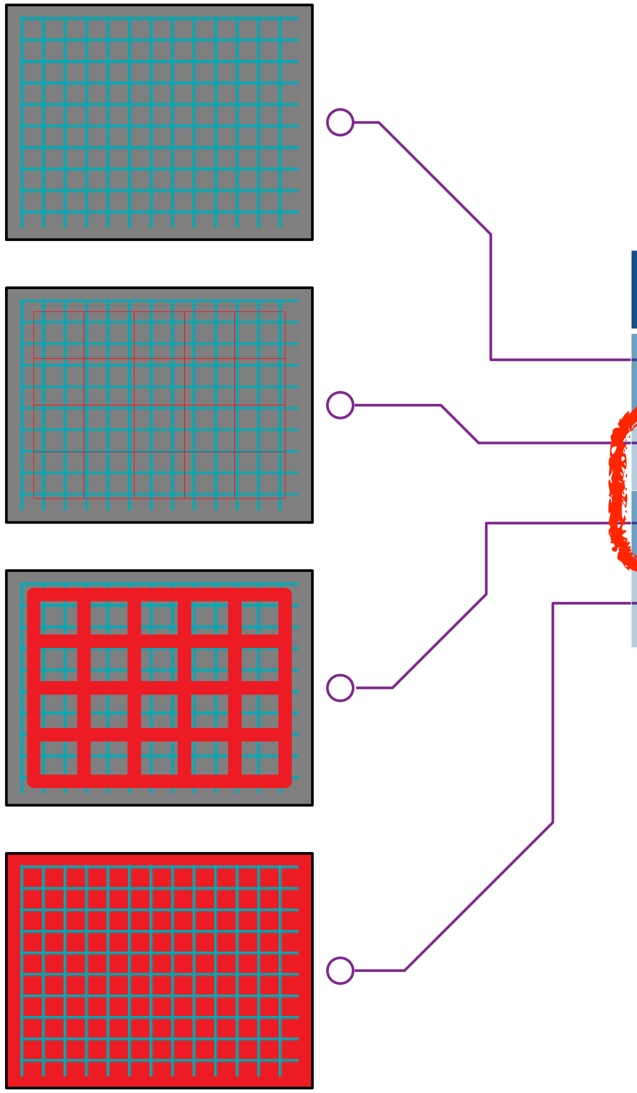

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Minimally Active Interposers for Large SoCs

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Active interposer is not free…

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Active interposer is not free…

… But appears practical if used judiciously

Minimally Active Interposers for Large SoCs

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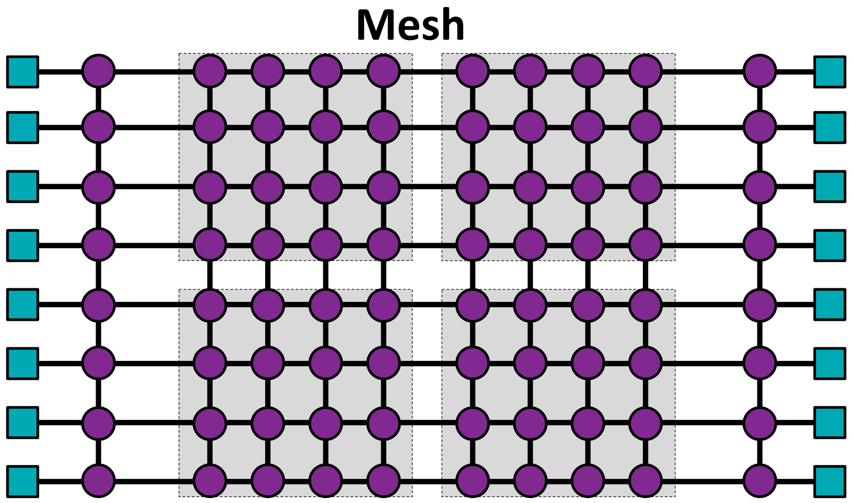
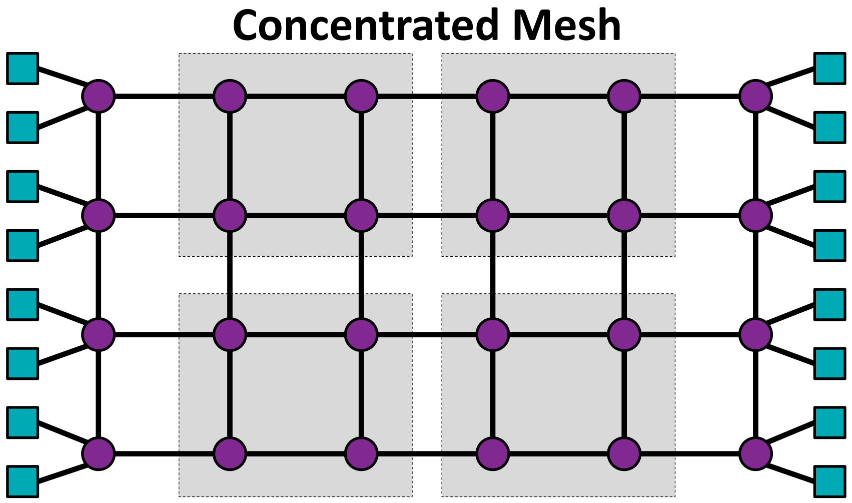
So how should we design our NoC on interposer?

NoC Goals: Diameter vs Bisection Bandwidth





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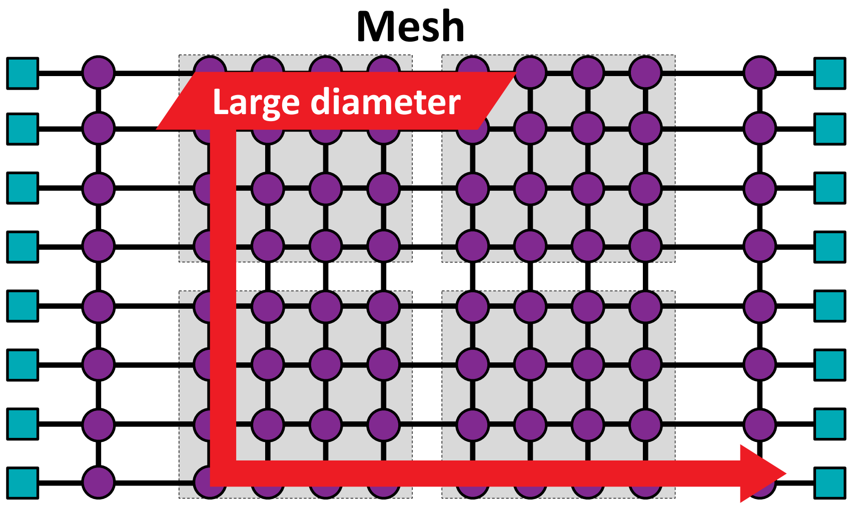

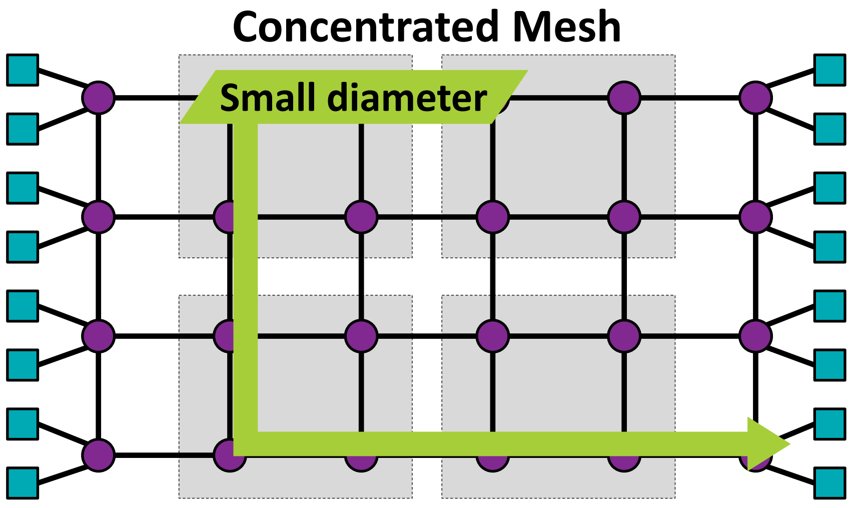

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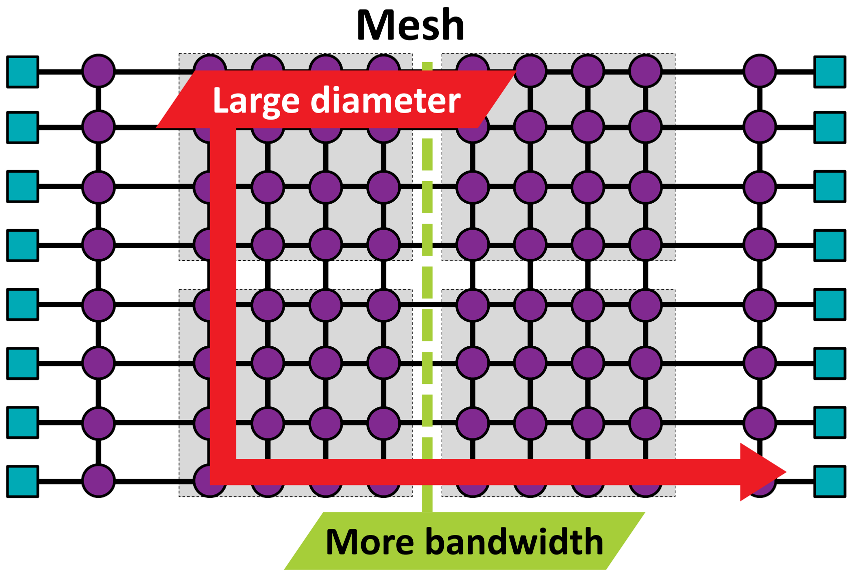

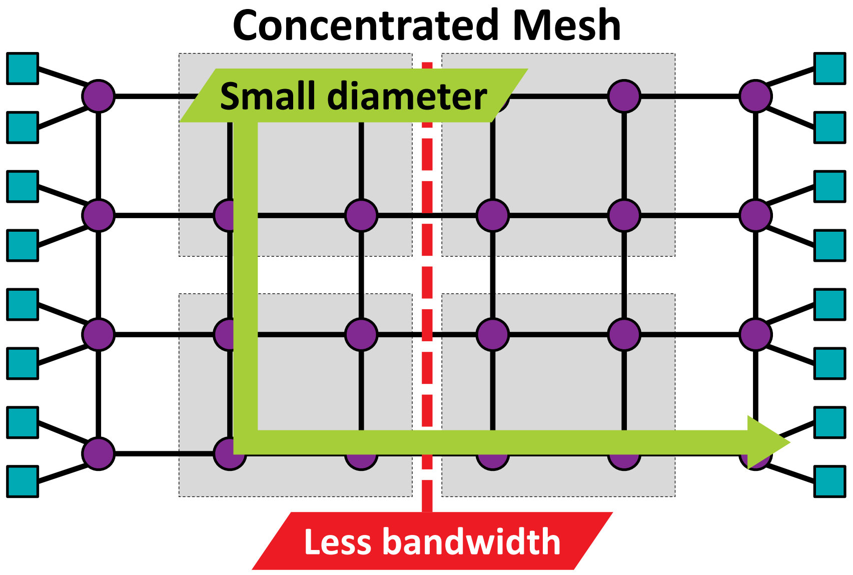

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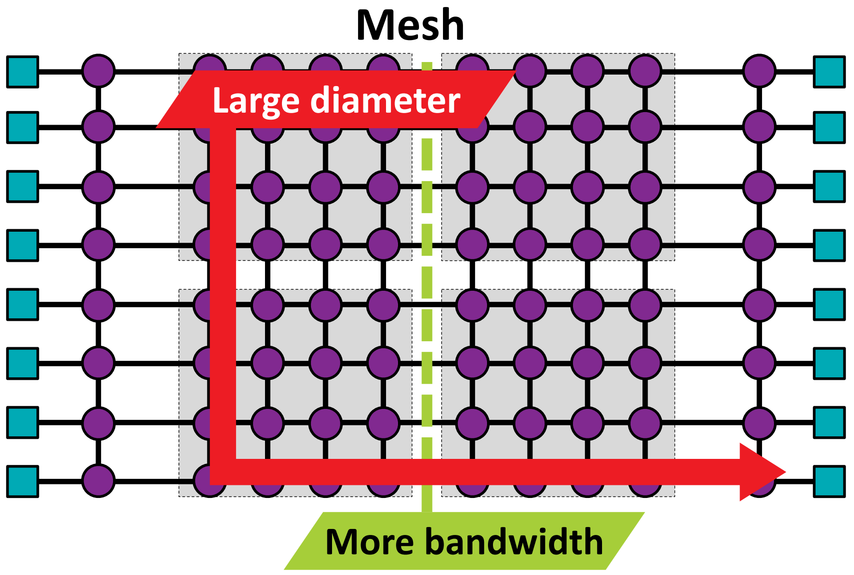
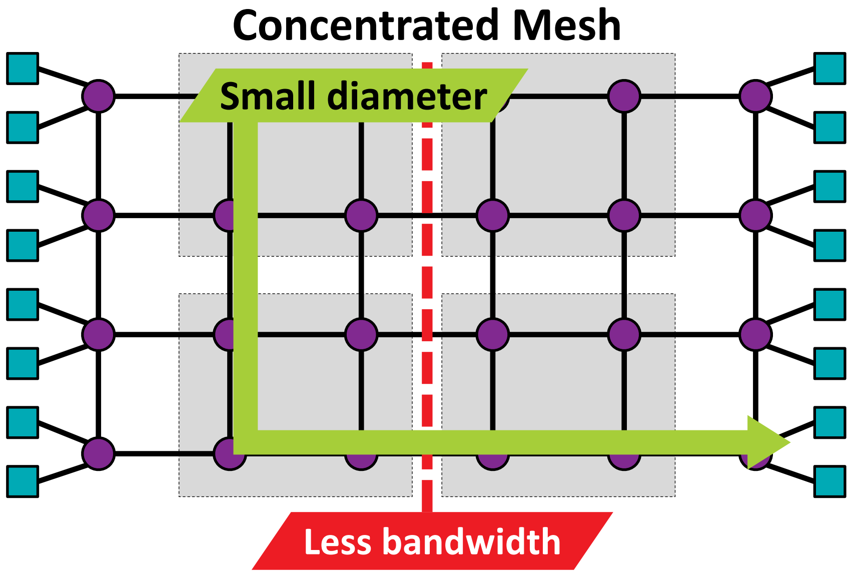
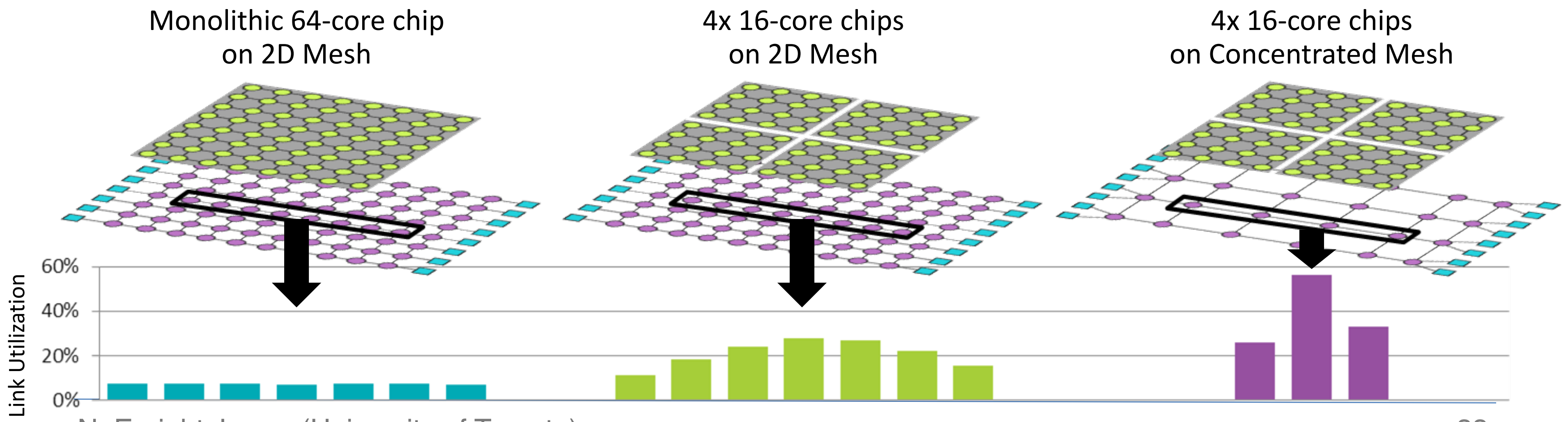


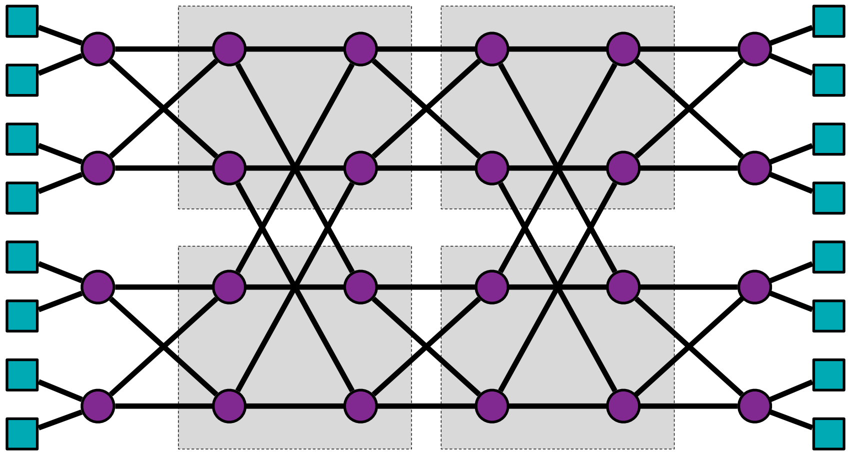




The ButterDonut

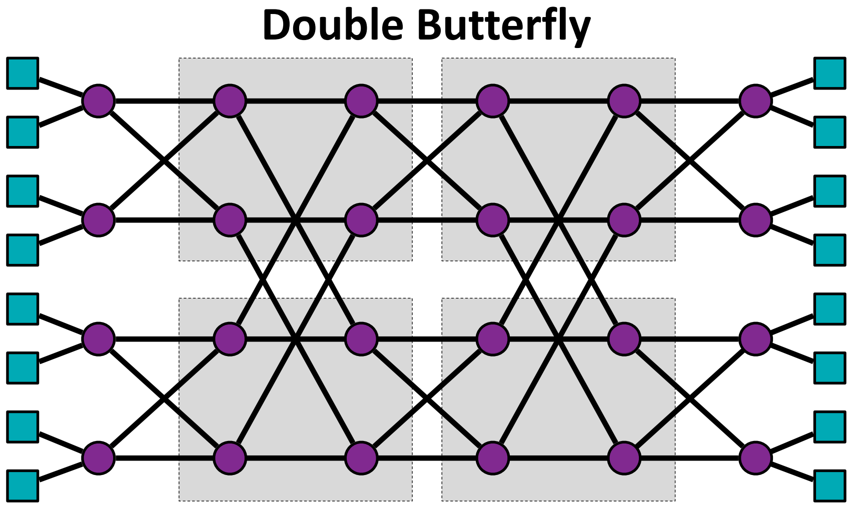
The ButterDonut

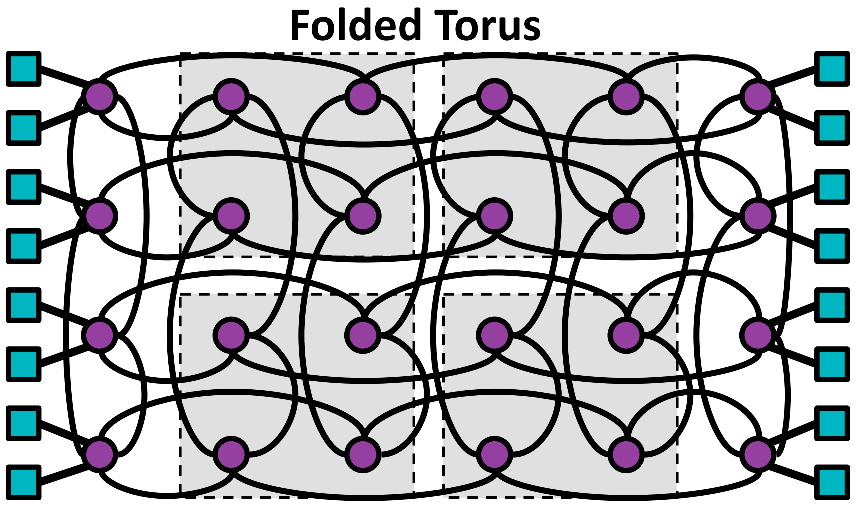
Double Butterfly



Optimized for E-W traffic (cores →memory)

The ButterDonut

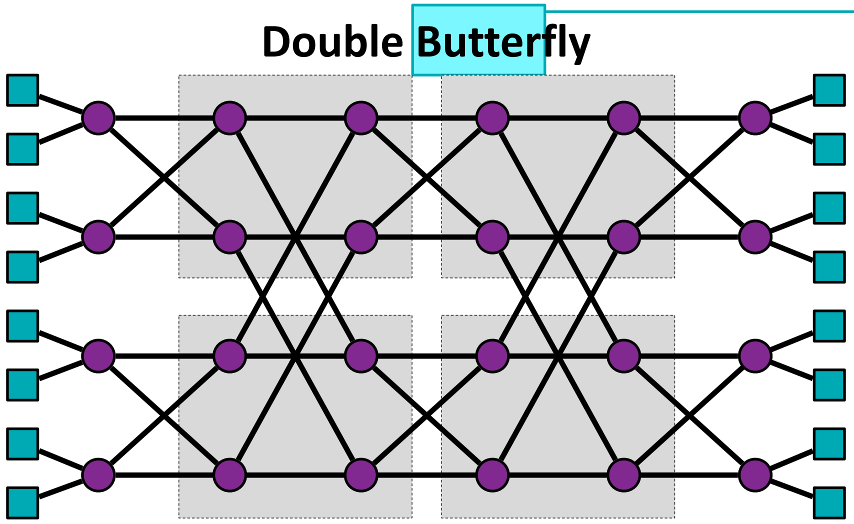




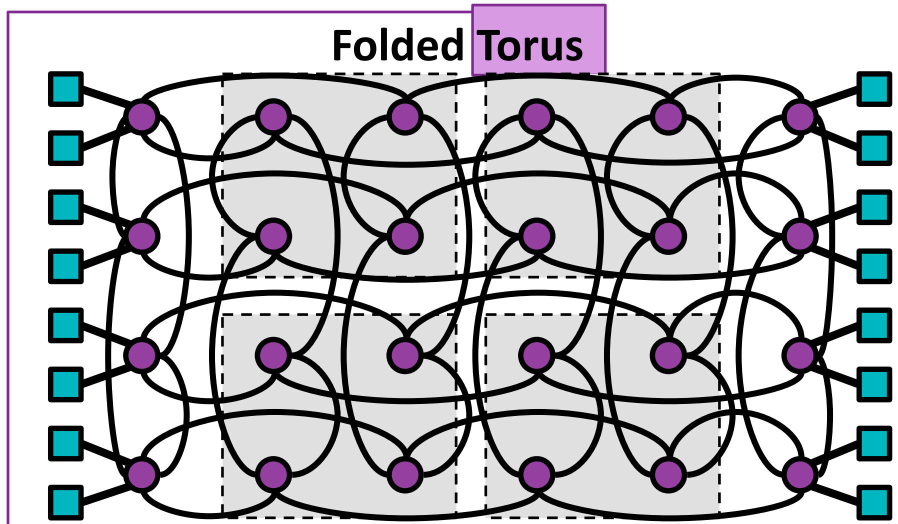
Optimized for E-W traffic (cores →memory)

Balanced, Fewer hops, +20% links

The ButterDonut



Optimized for E-W traffic (cores →memory)



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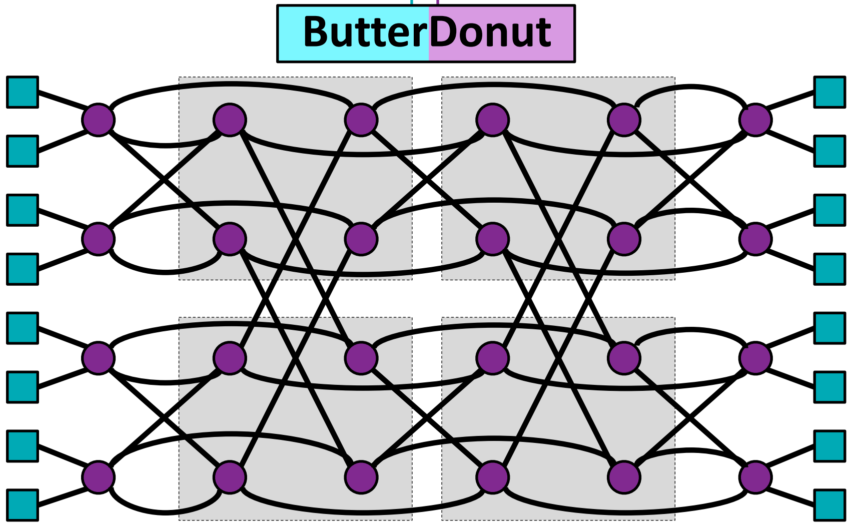

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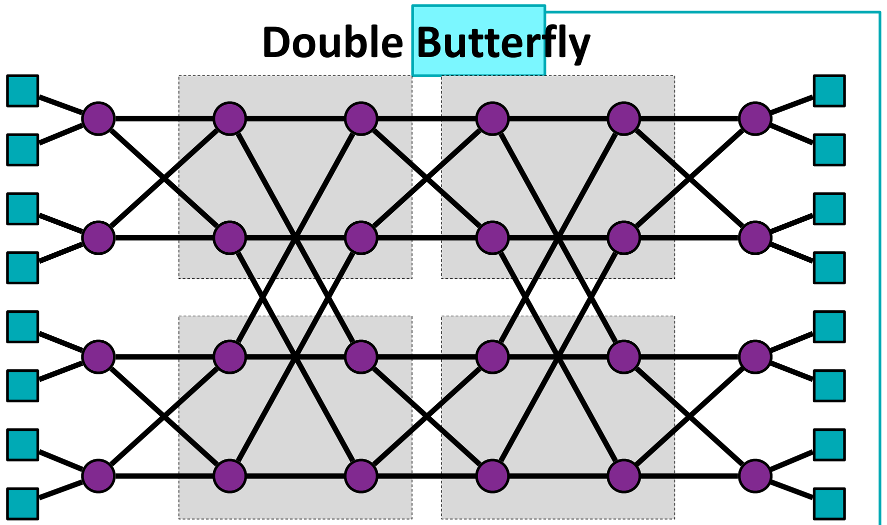

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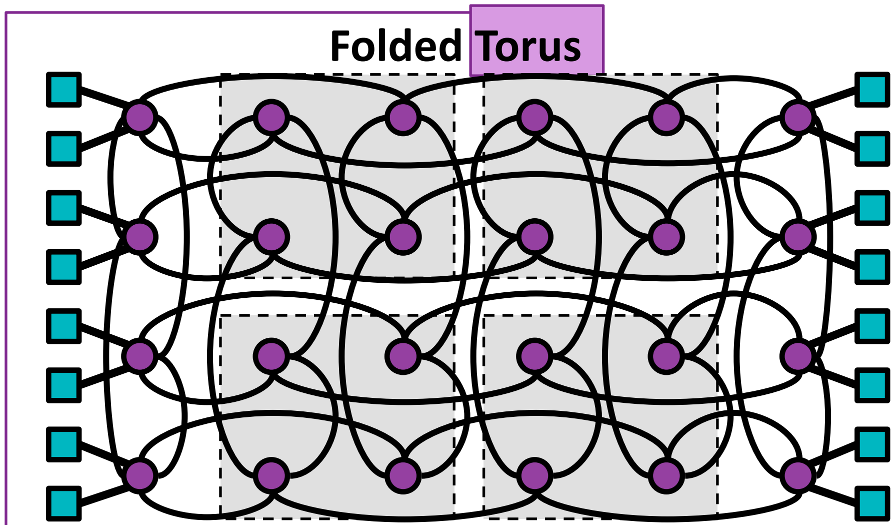

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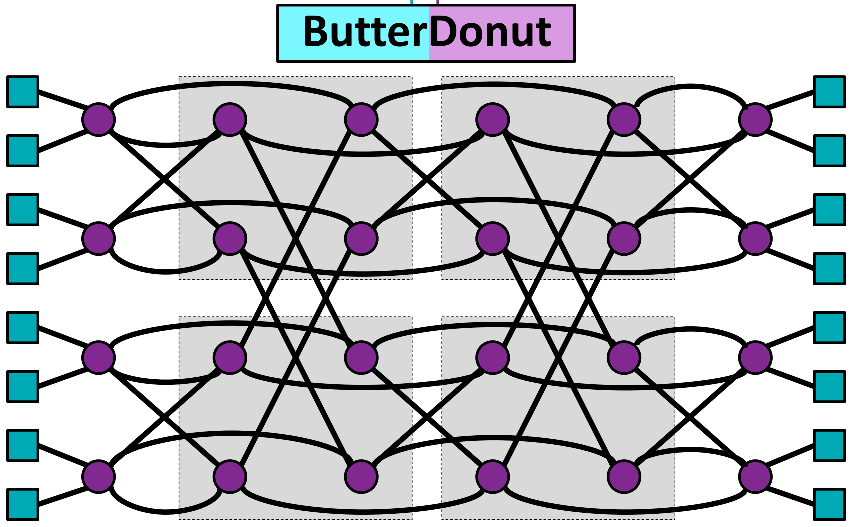


Smaller diameter

Lower Avg. Hop Count

Higher Bisection BW

+10% links vs. DButterfly

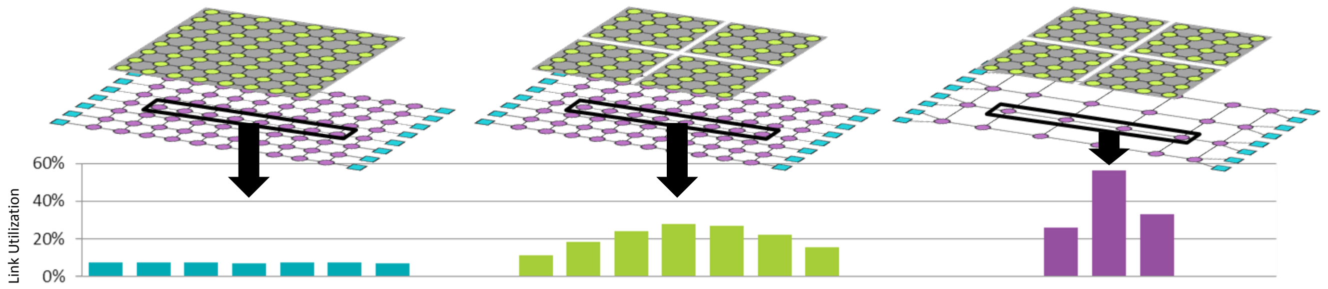
Interposer router misalignment

Interposer router misalignment

Monolithic 64-core chip on 2D Mesh

4x 16-core chips on 2D Mesh

4x 16-core chips on Concentrated Mesh



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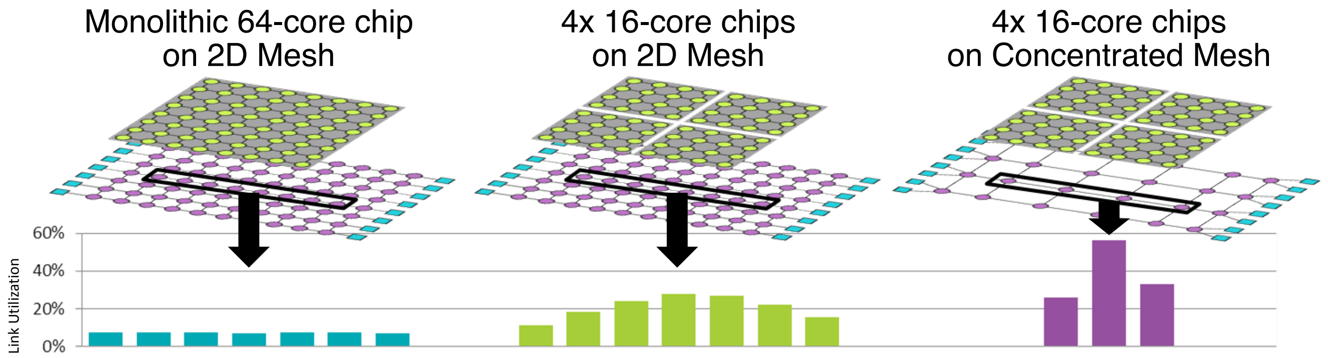
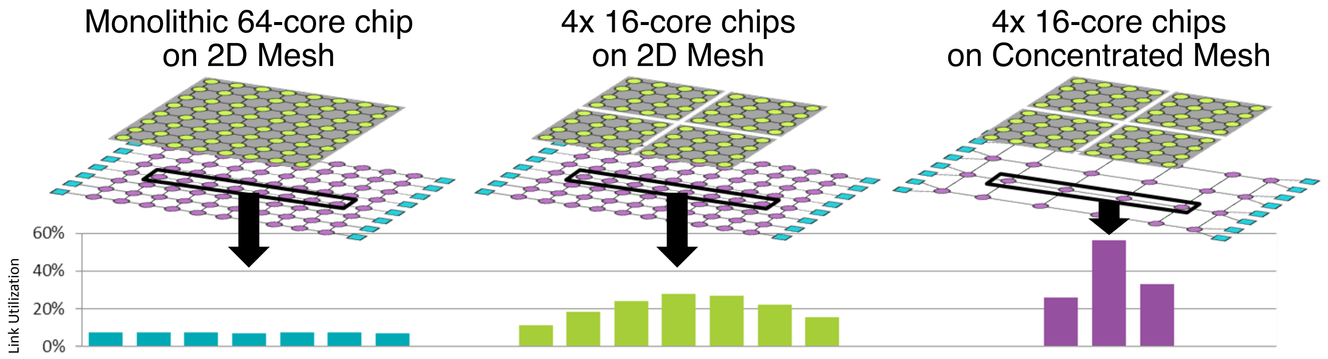


Bisection links are the primary bottleneck

Interposer router misalignment



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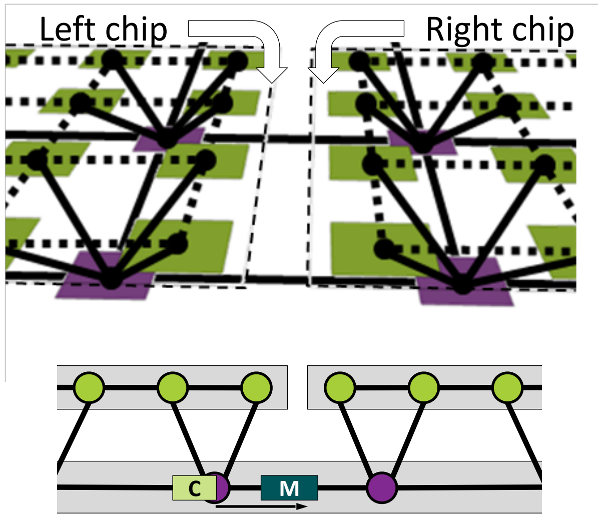

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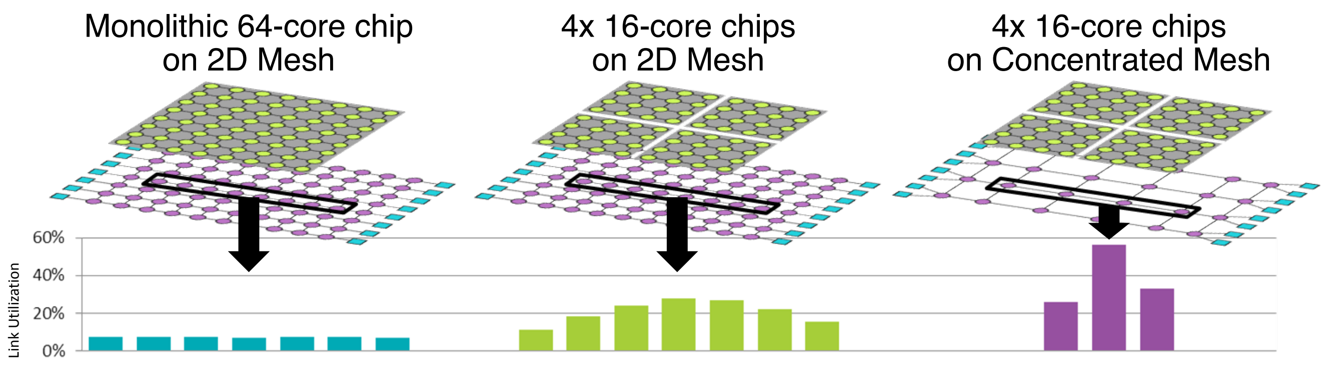

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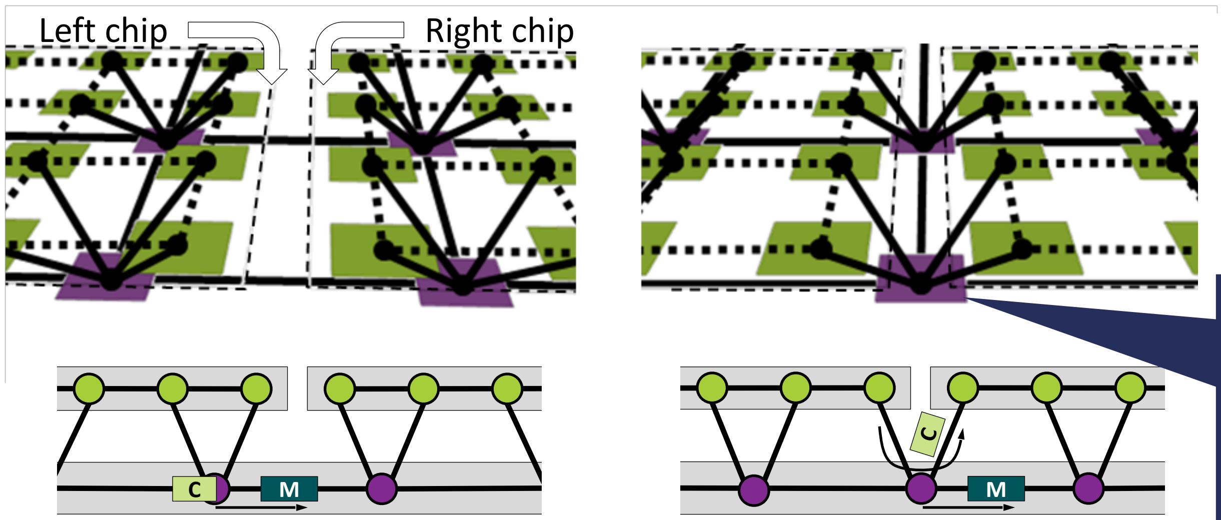
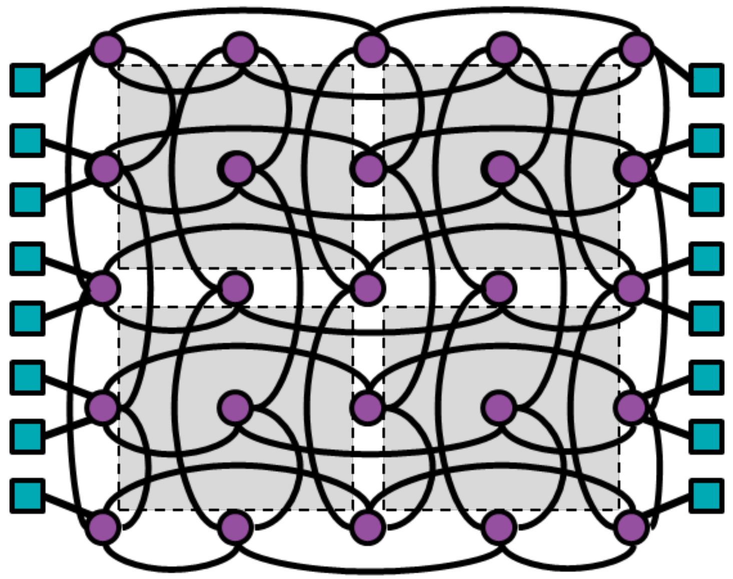


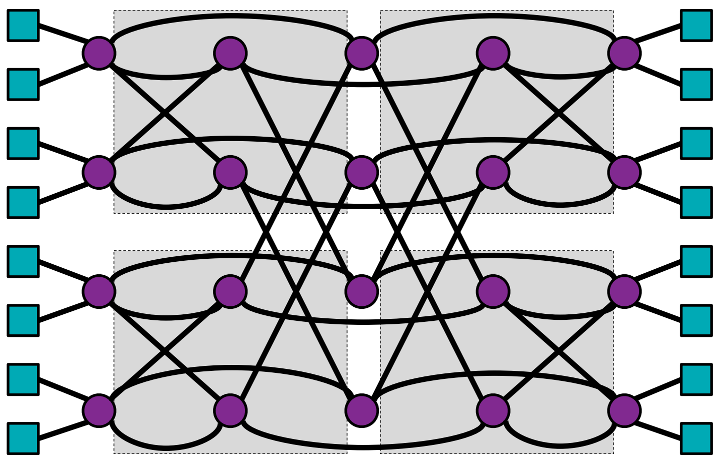
“Misaligned” router placed in between chips

Misaligned Topologies

Folded Torus(X+Y)



Misaligned ButterDonut(X)



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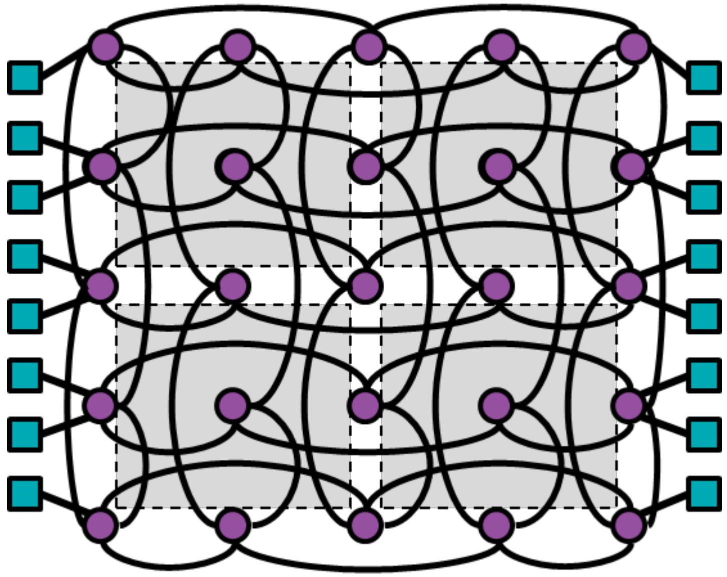

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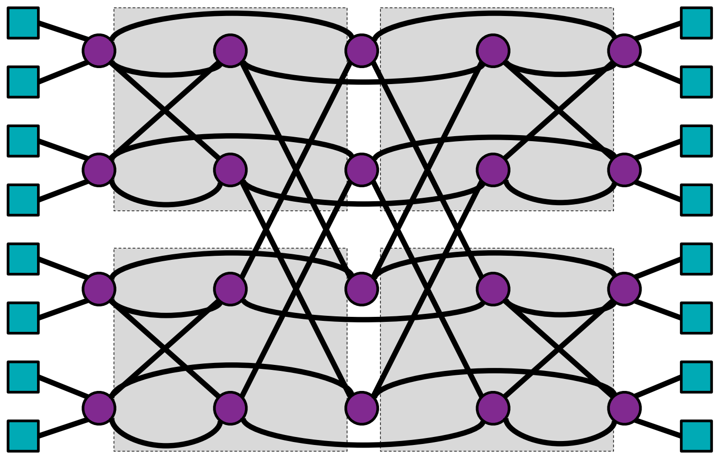

😁 Small # routers

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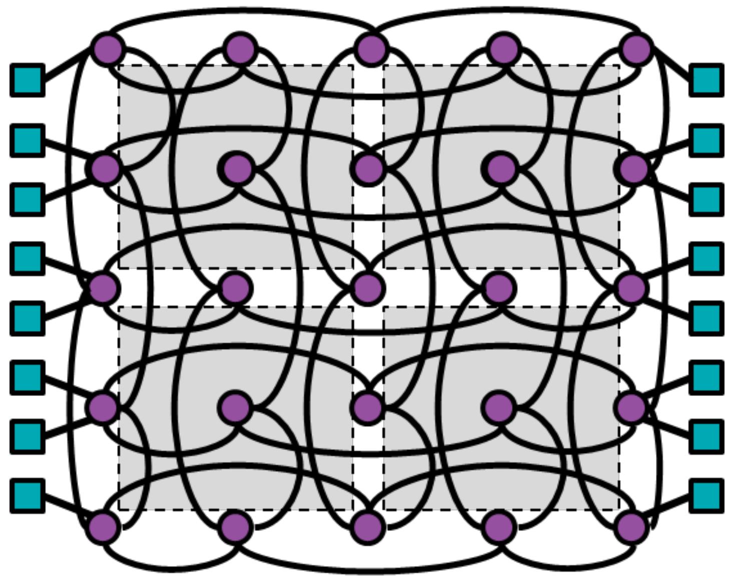

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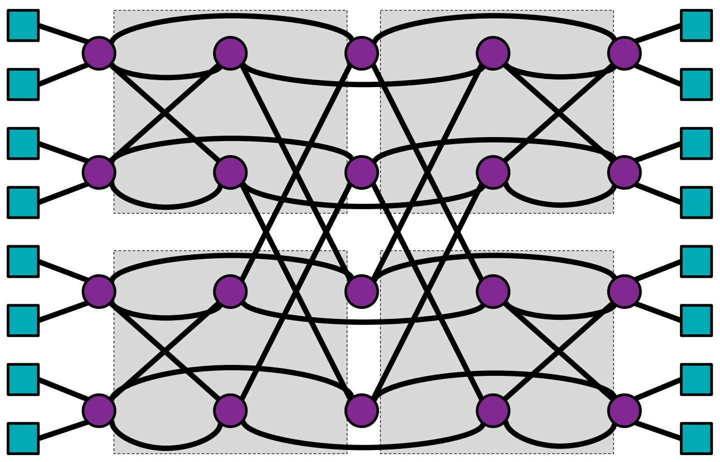

- 😁 Small # routers
- 😁 Small # links*

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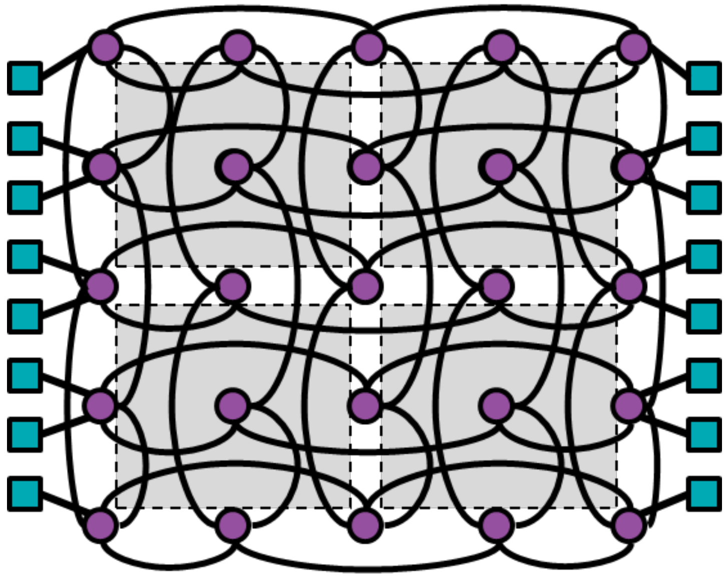

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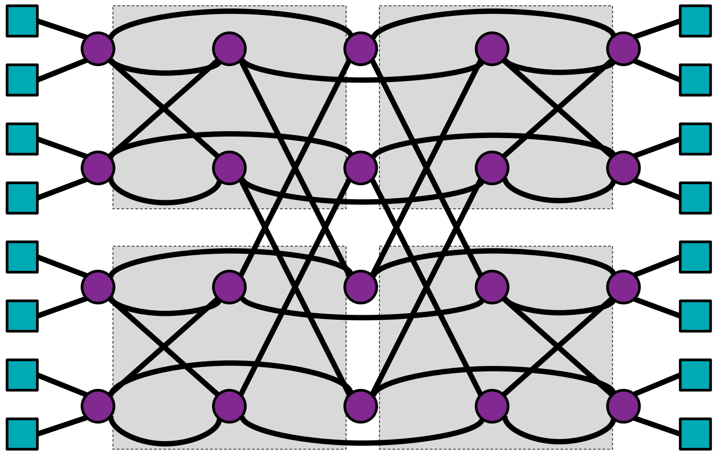
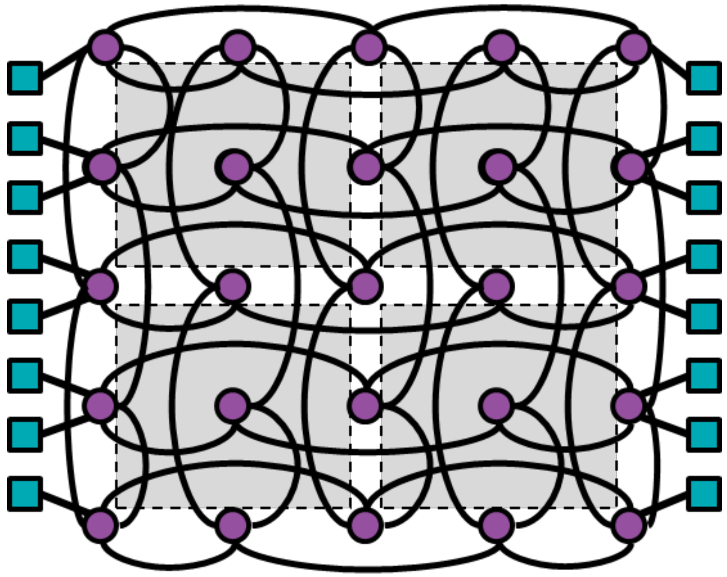


- 😁 Small # routers
- 😁 Small # links*
- 😁 Small diameter

Misaligned Topologies

Folded Torus(X+Y)



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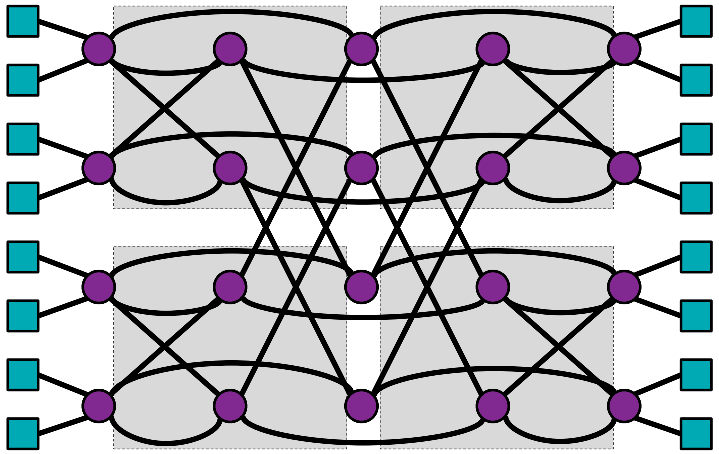

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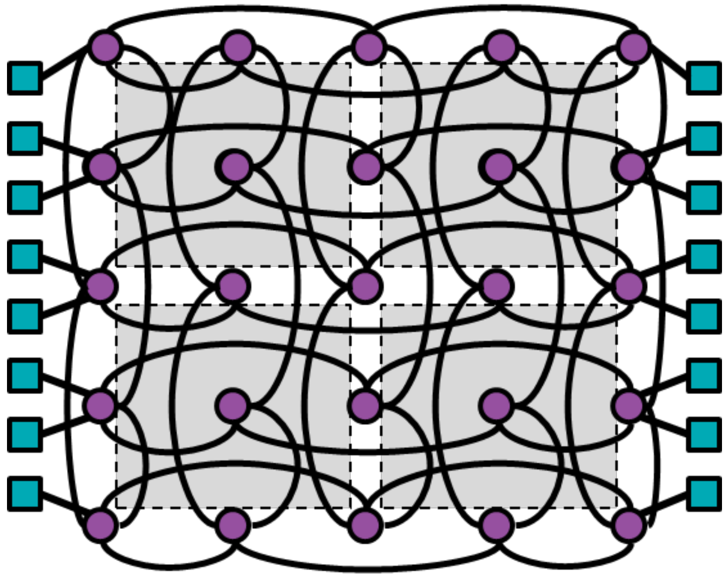

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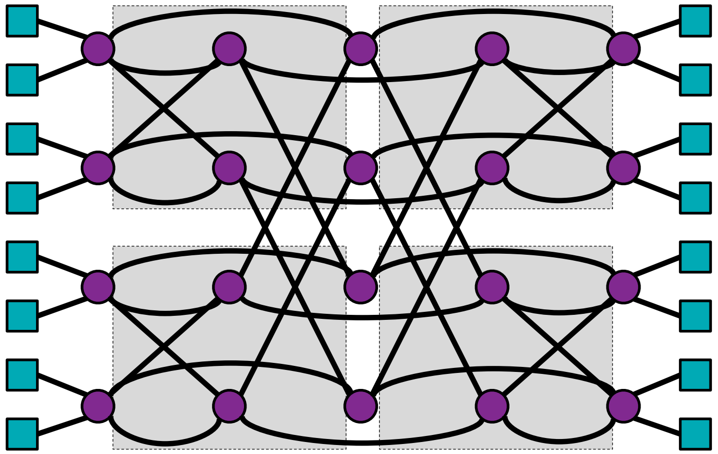

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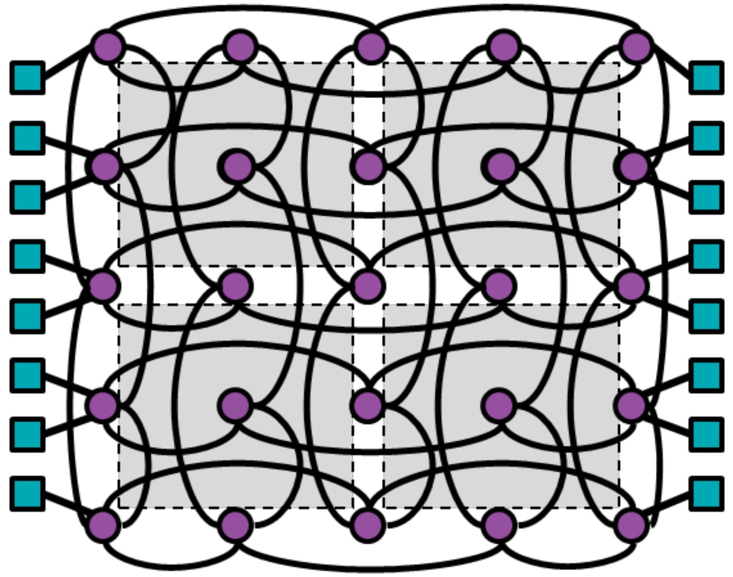

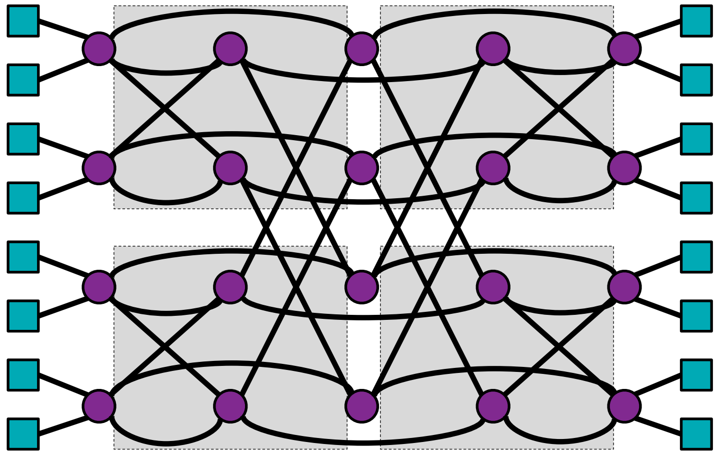

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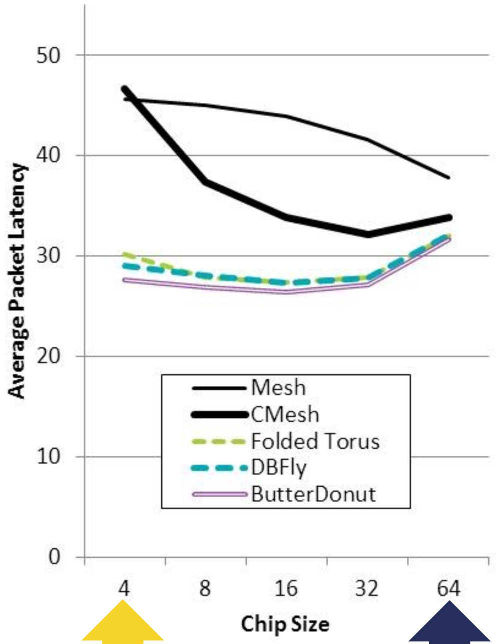
Hybrid topology + misalignment gets you best of everything (almost)

Main takeaway: Disintegration is promising

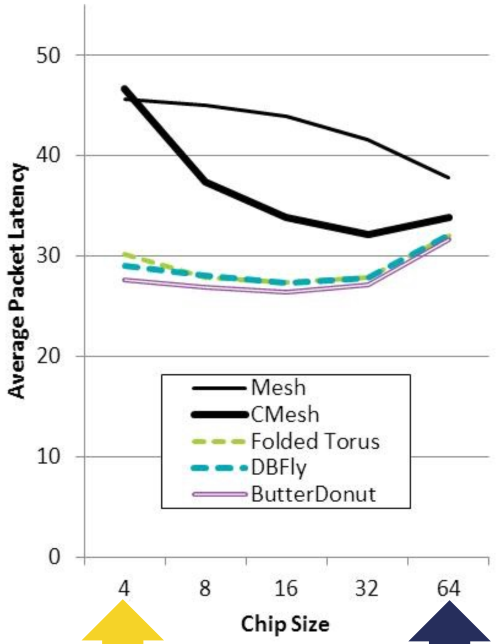


16x Quad-core chips

1x 64-core chip

Main takeaway: Disintegration is promising

Can design an interposer NoC topology to overcome disintegration-induced fragmentation of SoC



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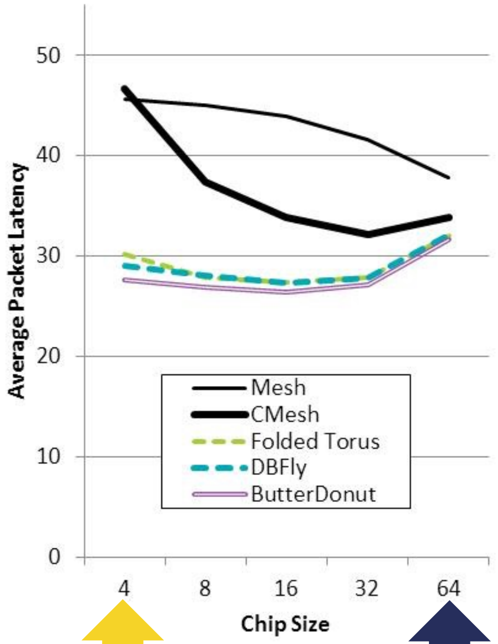

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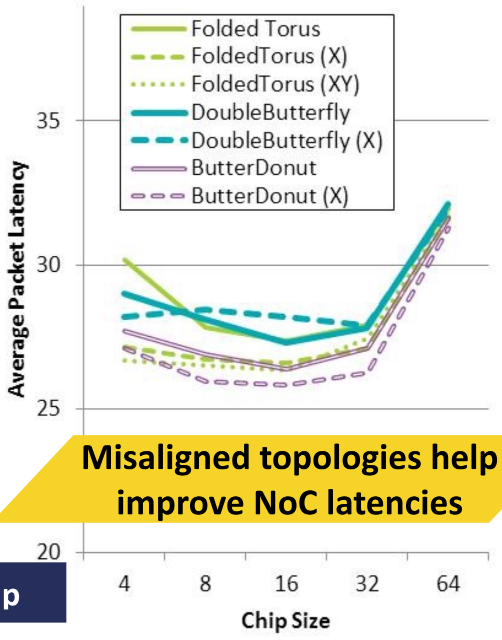

Misaligned topologies help improve NoC latencies

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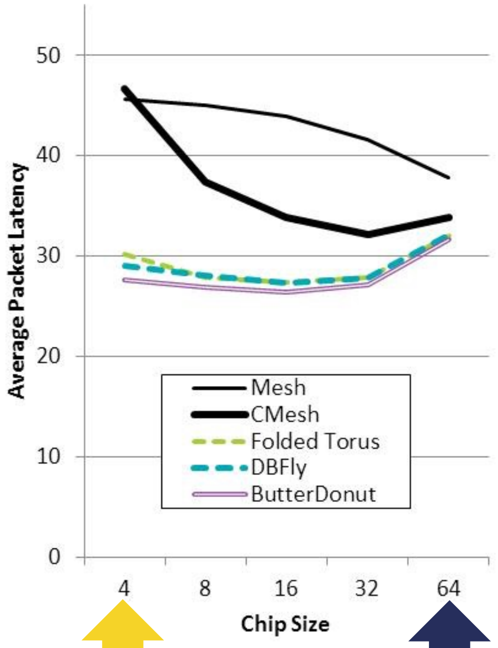

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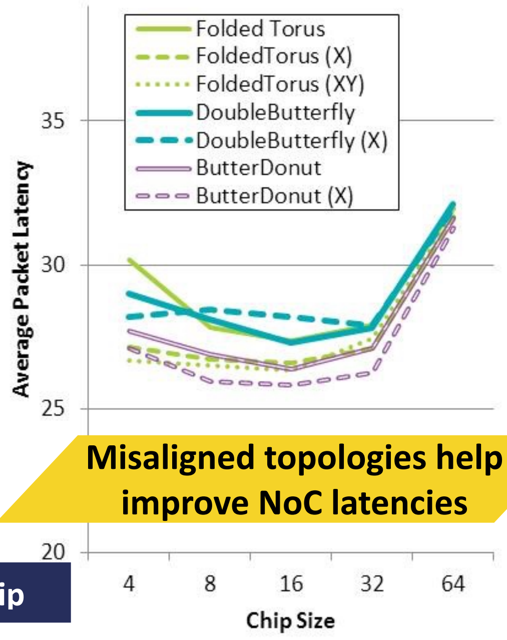

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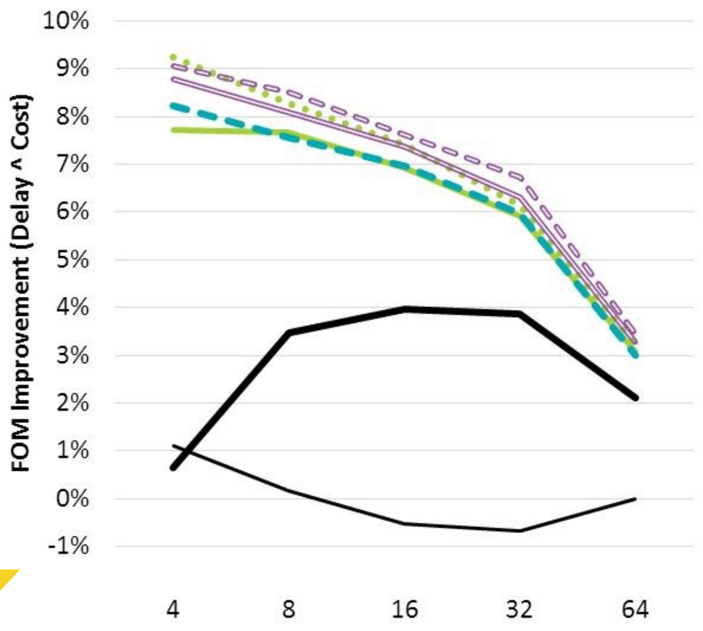
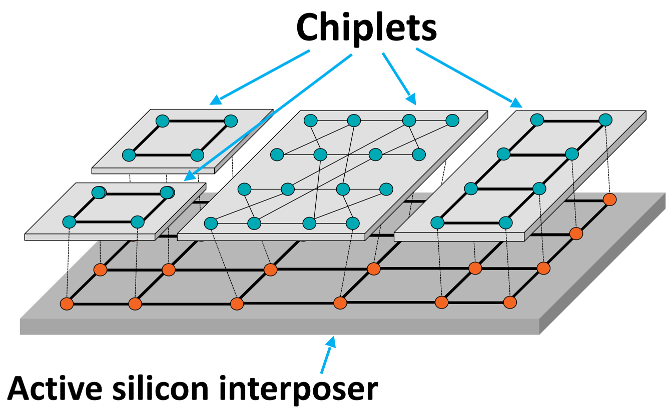


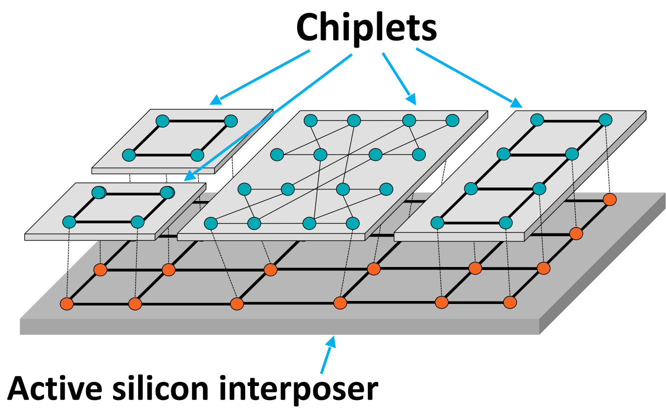
You <u>can</u> go too far…

Disintegration is promising… but how to route?



Disintegration is promising… but how to route?

Now we have a NoC that spans both chiplets and interposer



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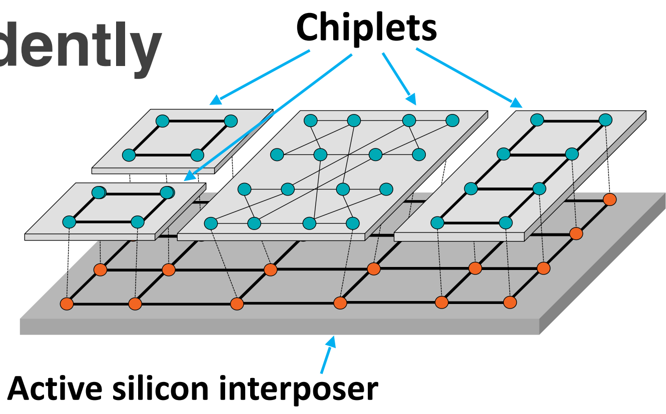
Each chiplet may be designed independently



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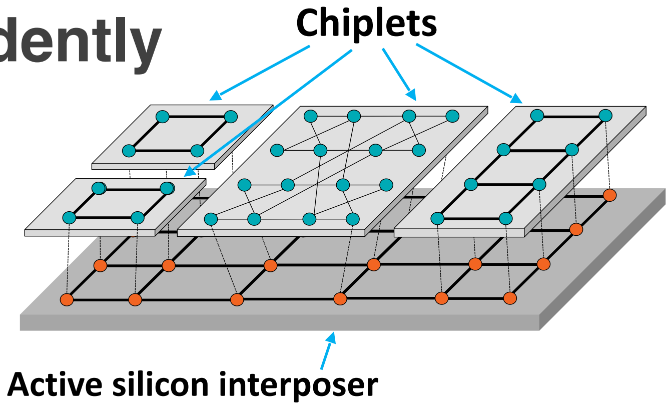
Goals:

- Free to choose NoC topology on chiplet
- Free to choose local routing algorithm within chiplet (deadlock free)



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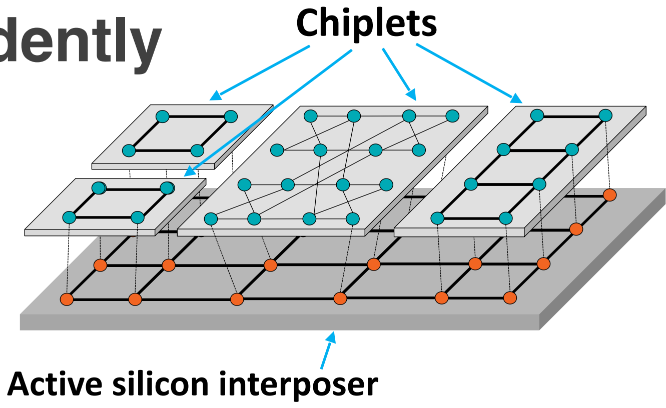
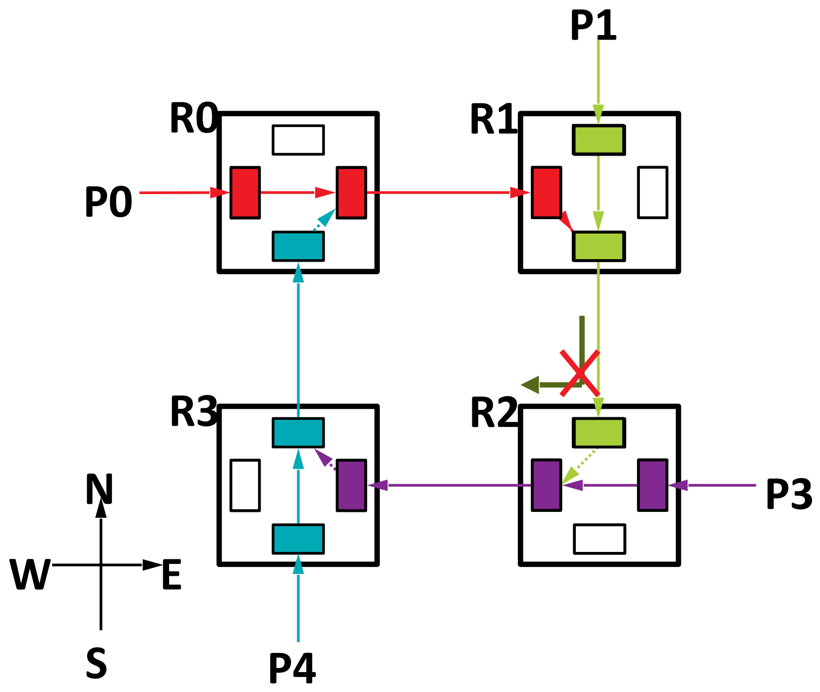


Problem: Even though NoCs for chiplets and interposer are individually deadlock free, how do you ensure the final composed system is still correct?

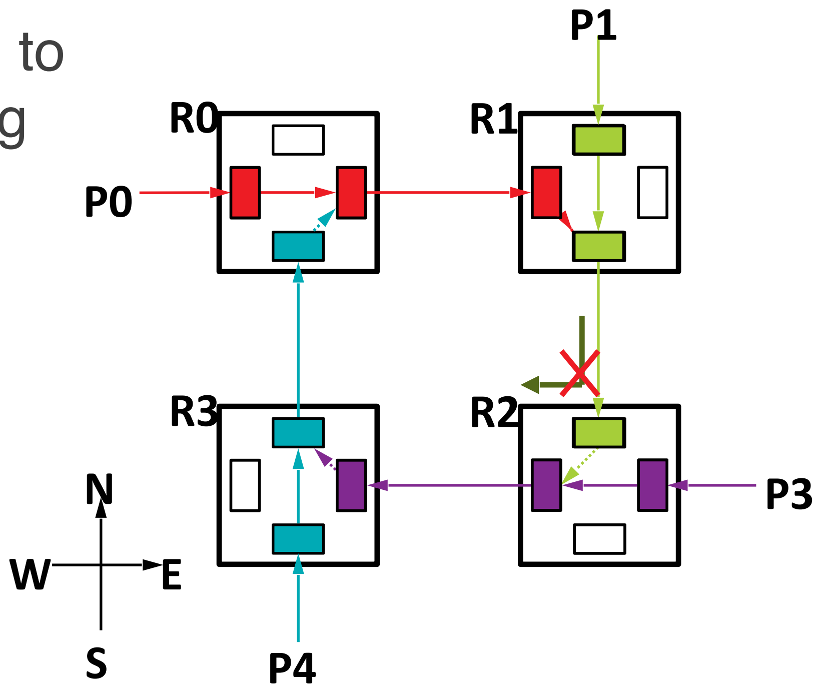
Deadlock primer



Deadlock primer

Deadlock

Can occur when packets are allowed to hold some resources while requesting others



Deadlock primer

Deadlock

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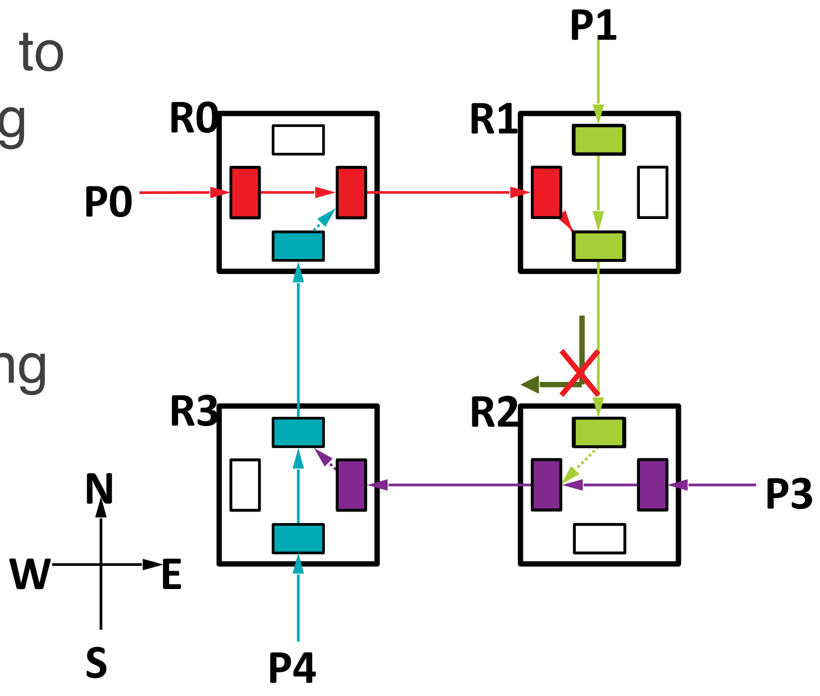
Deadlock avoidance

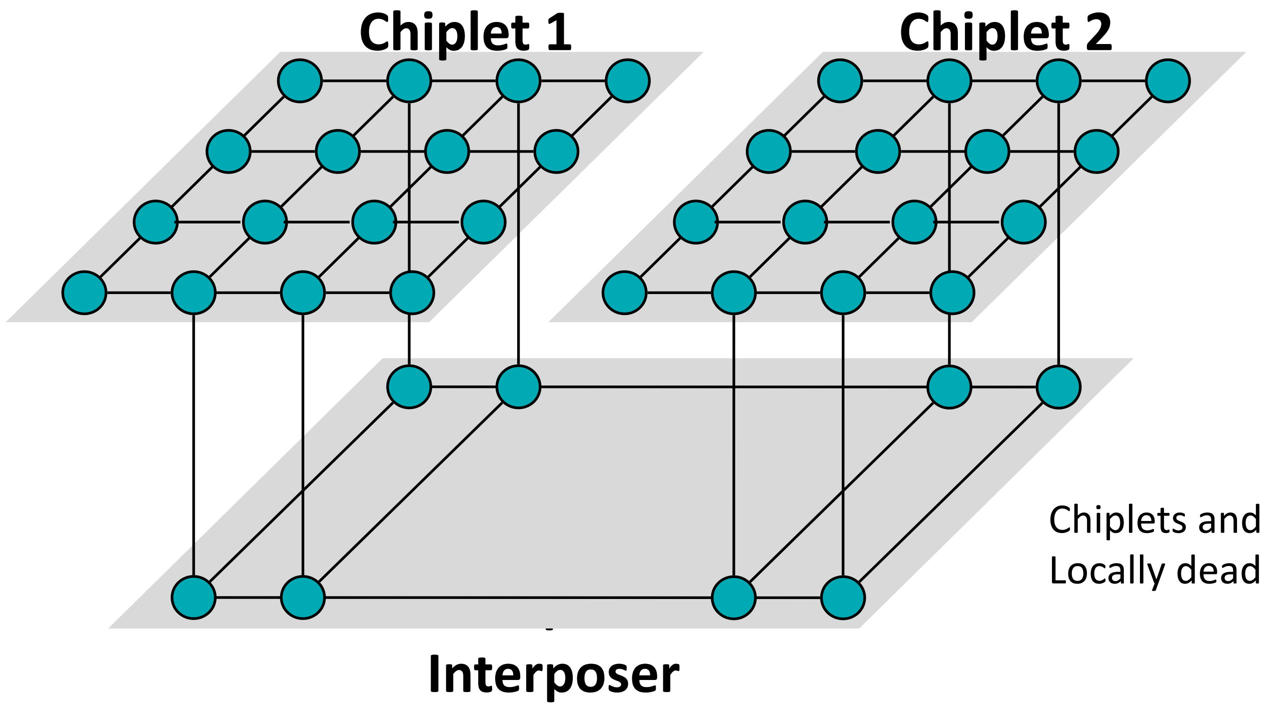
Avoid dependency cycles from forming

Example: Turn restrictions



Deadlock in Chiplet-based Systems

Deadlocks can occur even if individual chiplets are deadlock free



Chiplets and interposer use X-Y routing.
Locally deadlock free.

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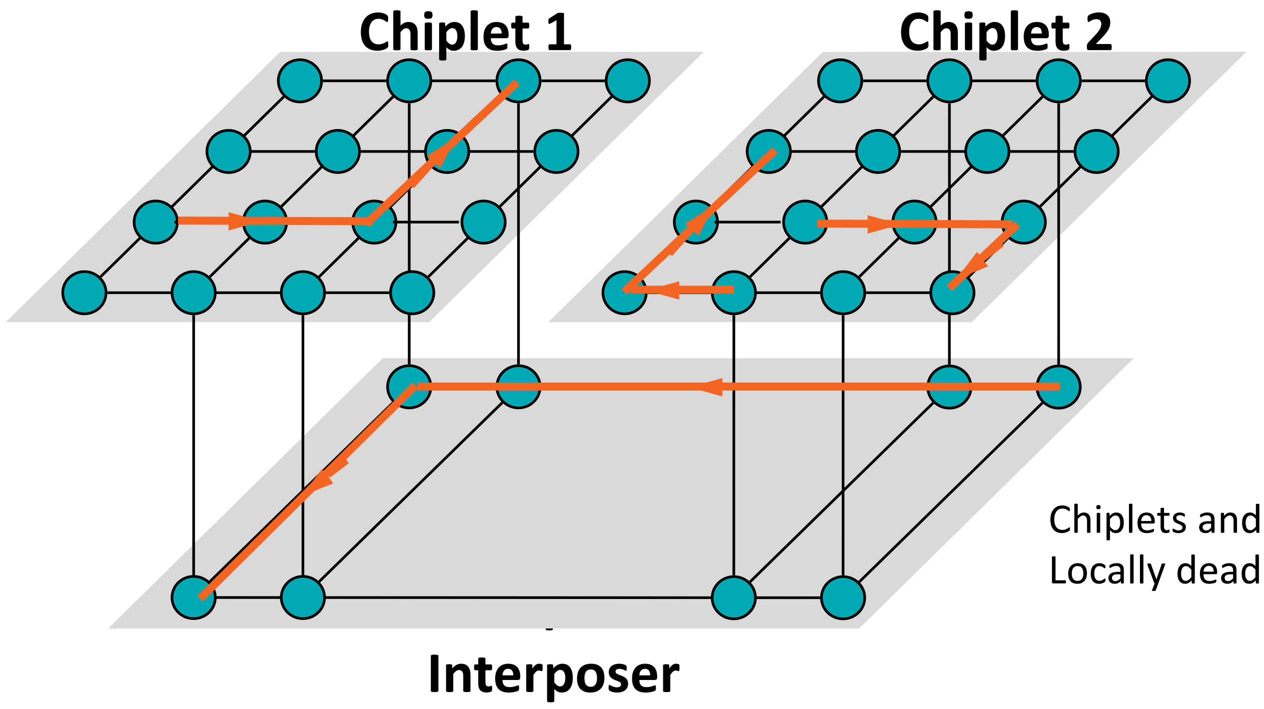

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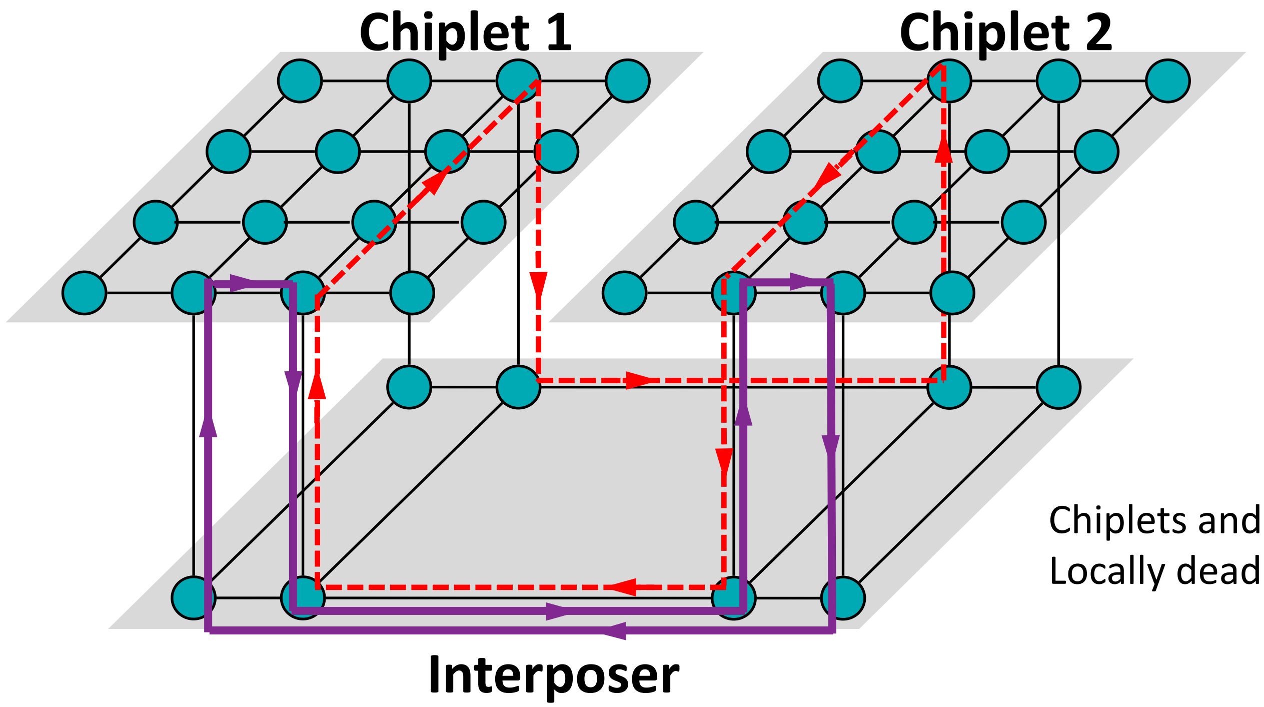

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Scalable analysis

- Analyze entire composition of NoCs and all possible paths
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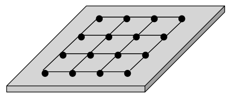

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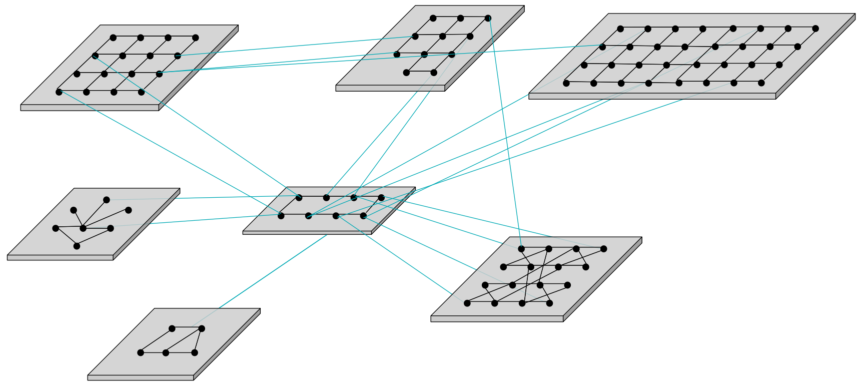

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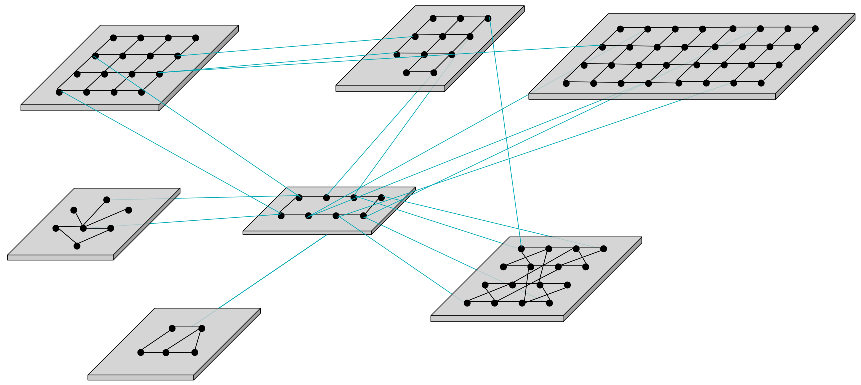

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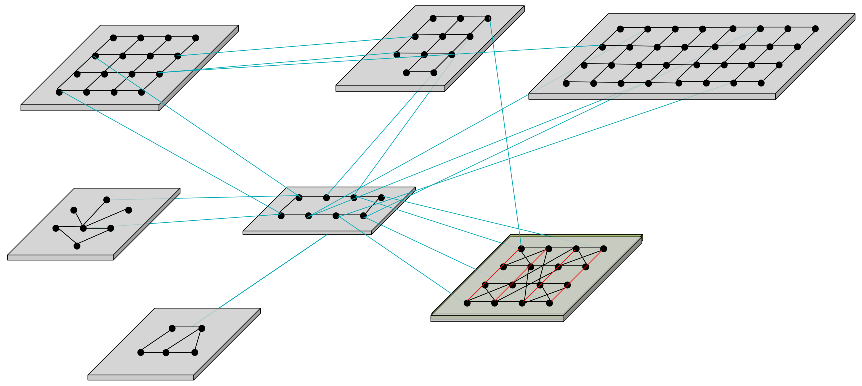

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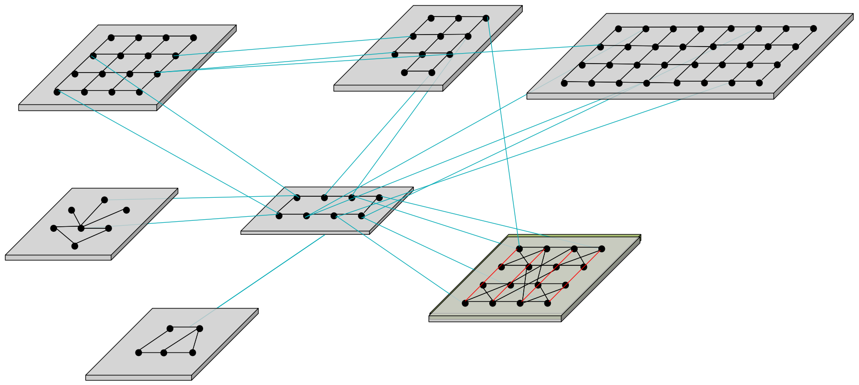

Local optimized chiplets

- Allow local optimization independent of final SoC organization

Lack info on other chiplets in system

- 3rd party may not want to share
- Other chiplets may not have been designed/finalized yet
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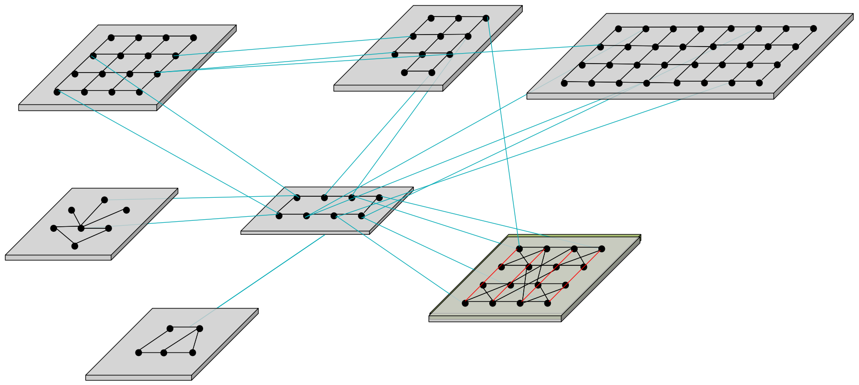

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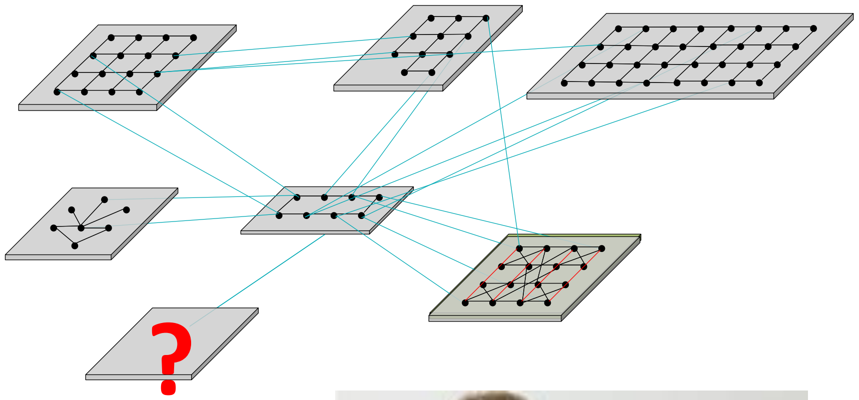

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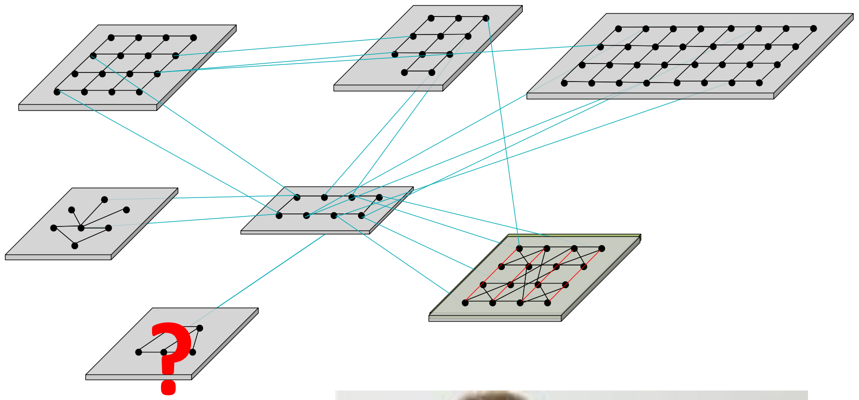

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- final

Chiplet composability is a HARD problem

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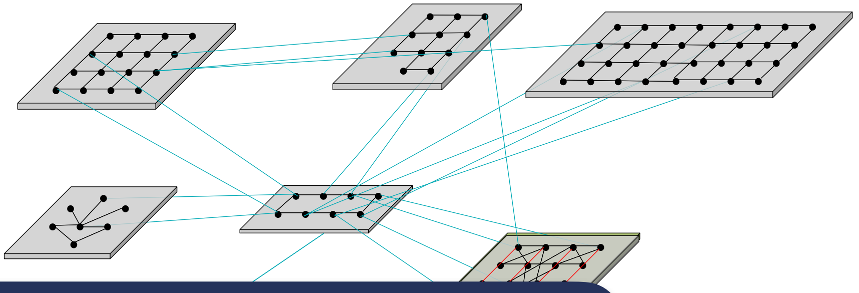

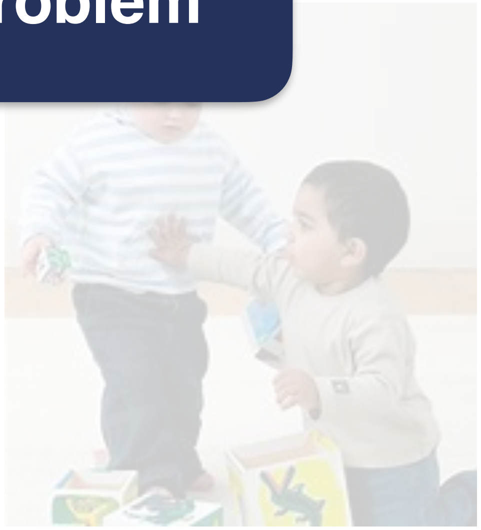

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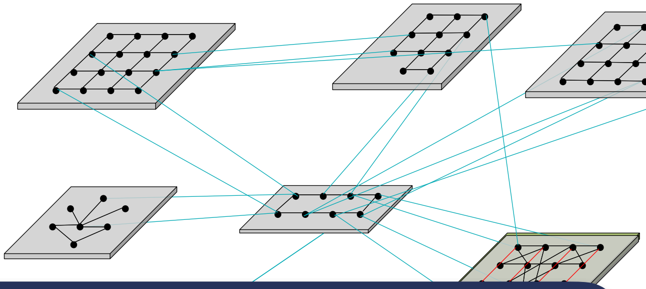
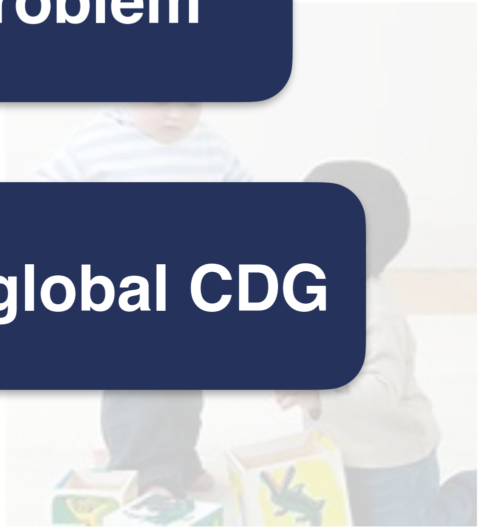


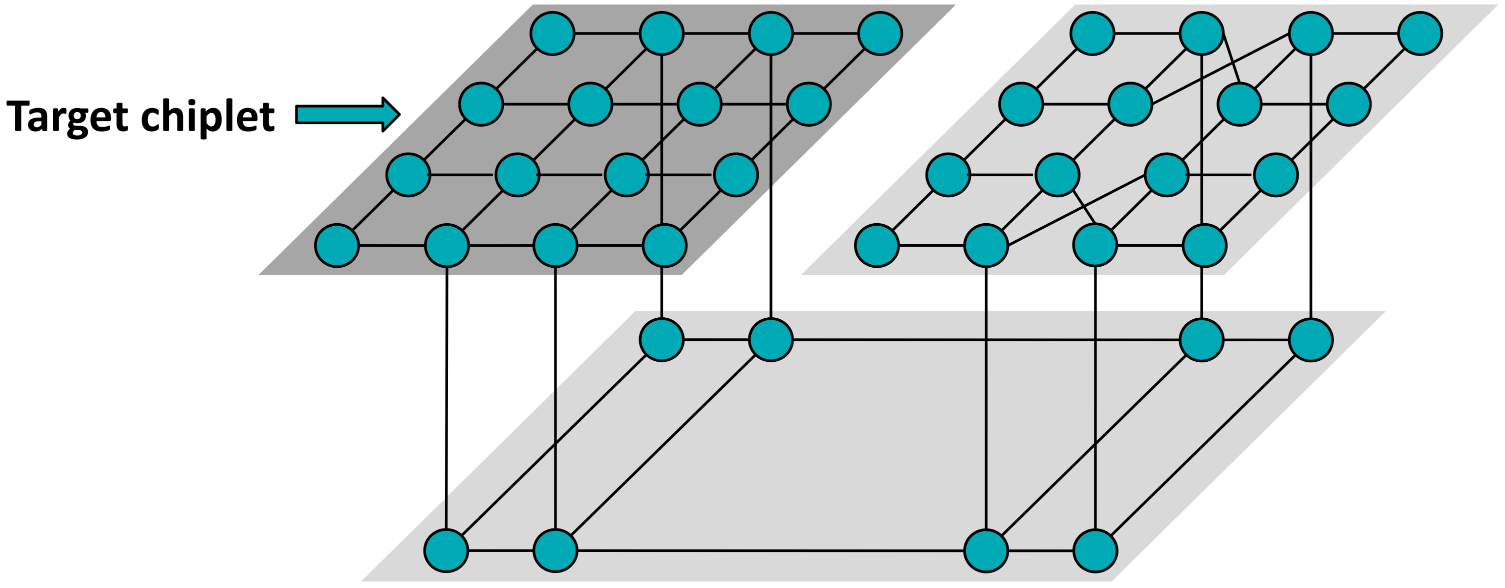


Chiplet composability is a HARD problem

Need a composable approach without global CDG

Our Methodology: Composable Routing

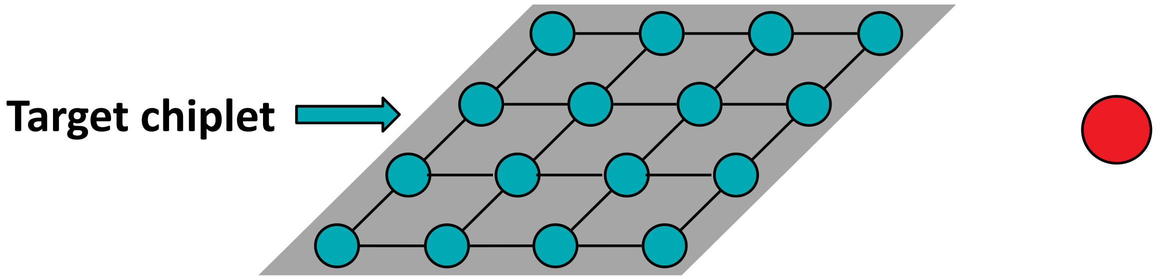
Step 1: Abstract node



Our Methodology: Composable Routing

Step 1: Abstract node

Abstract rest of the system with a single node (key insight)



Our Methodology: Composable Routing

Step 1: Abstract node

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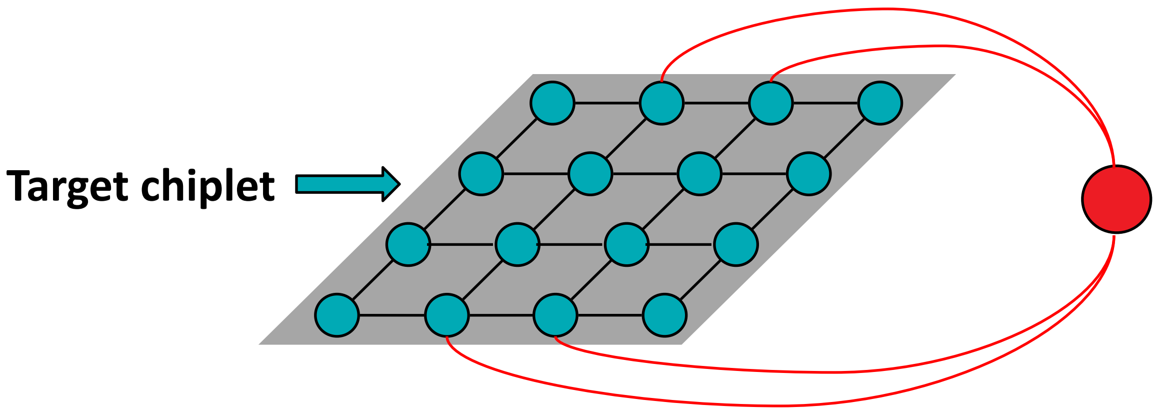
- Connect the chiplet to the abstract node



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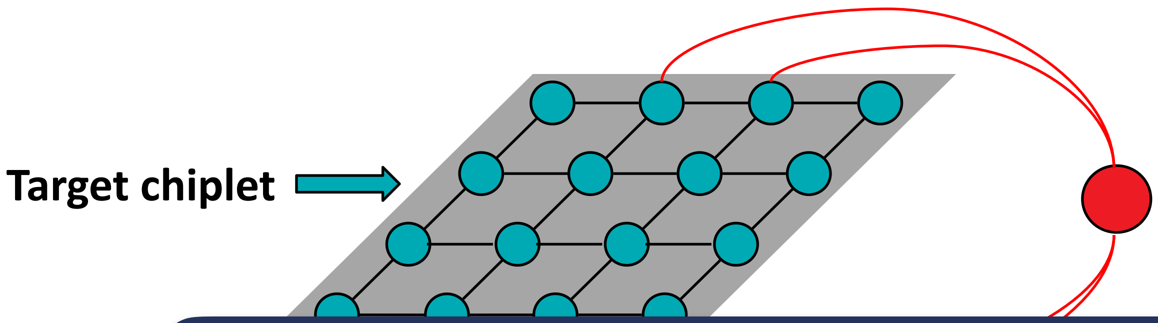
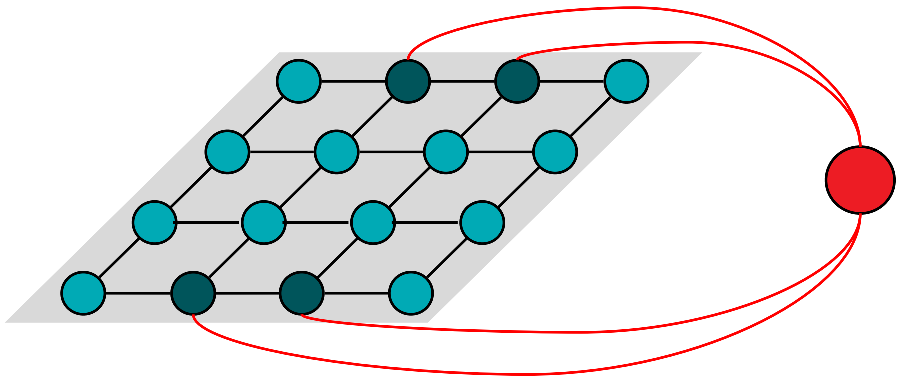


The new system must be deadlock free

Our Methodology: Composable Routing

Step 2: Turn restrictions

Apply turn restrictions **only at boundary nodes**



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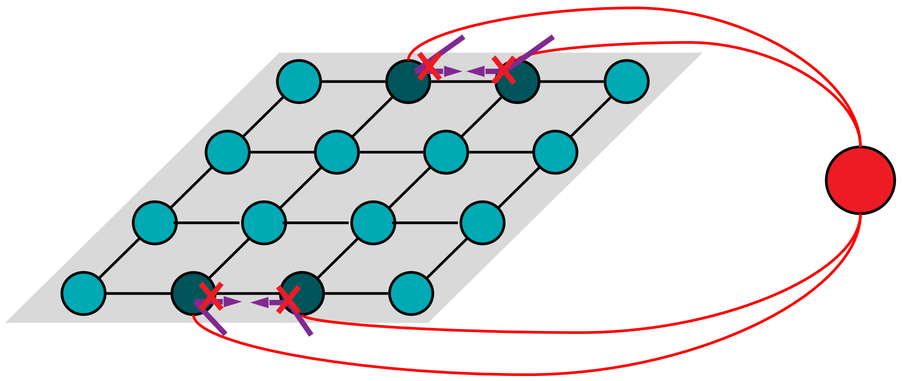

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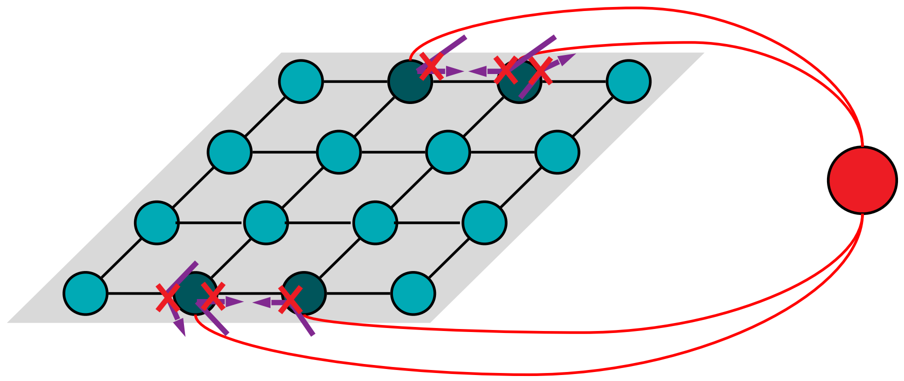

Our Methodology: Composable Routing

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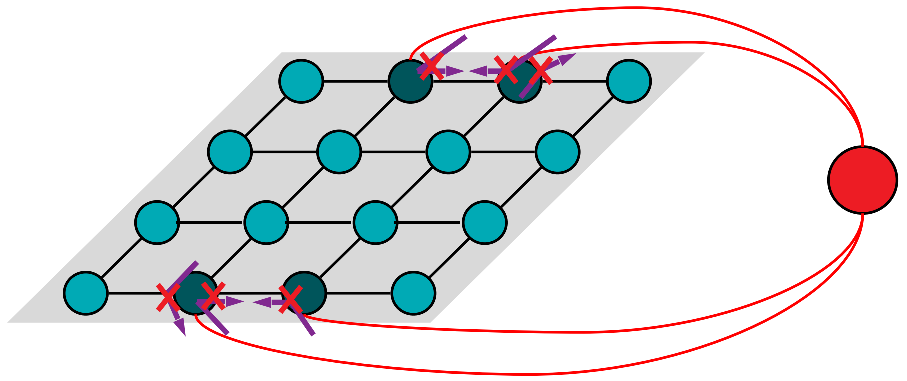

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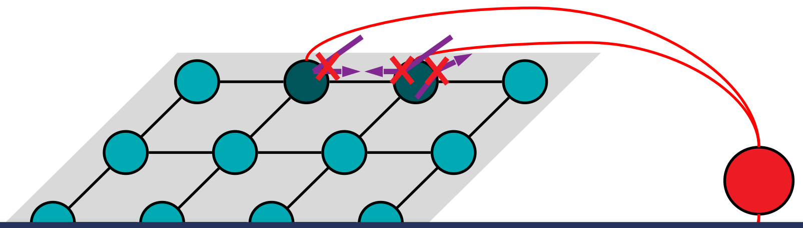
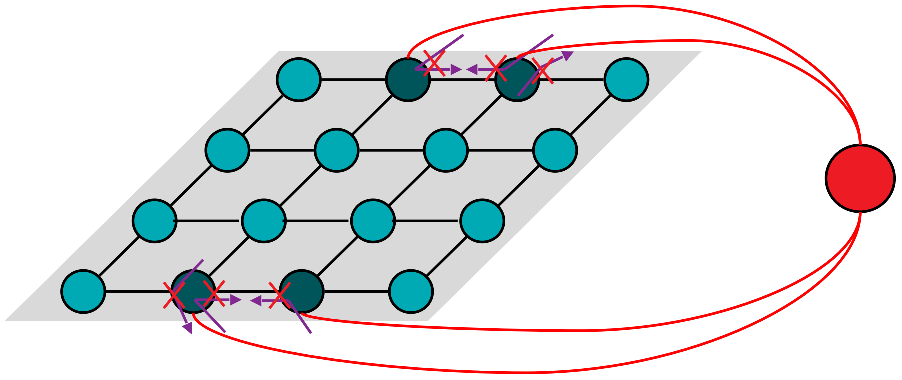


Messages must be routed through the correct boundary nodes

Our Methodology: Composable Routing

Step 3: Reachability

Propagate inbound reachabilities to the interposer (system integrator)



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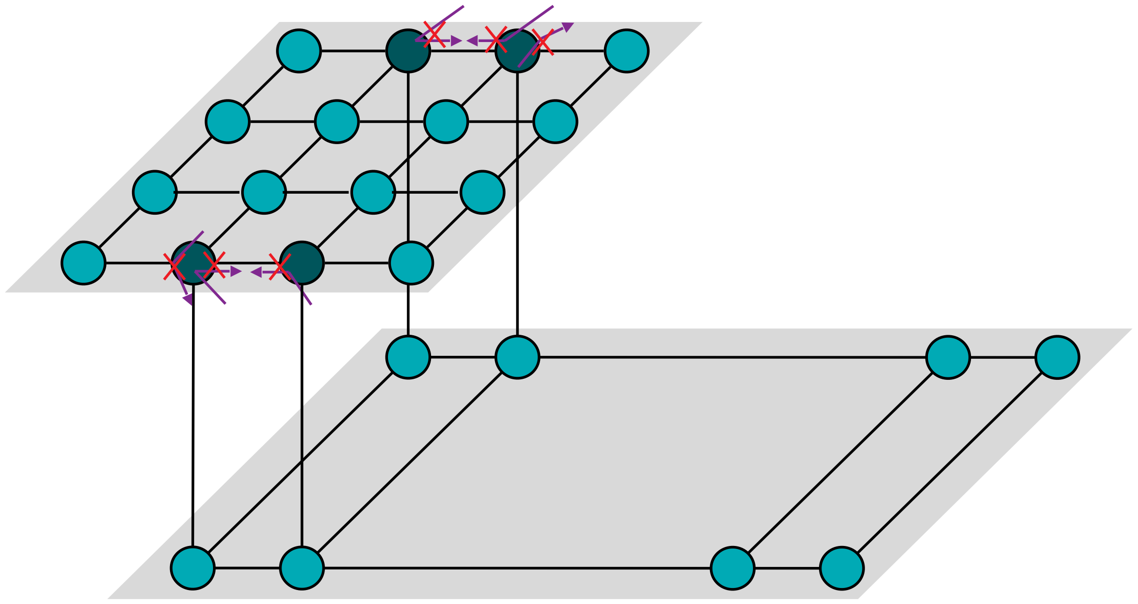

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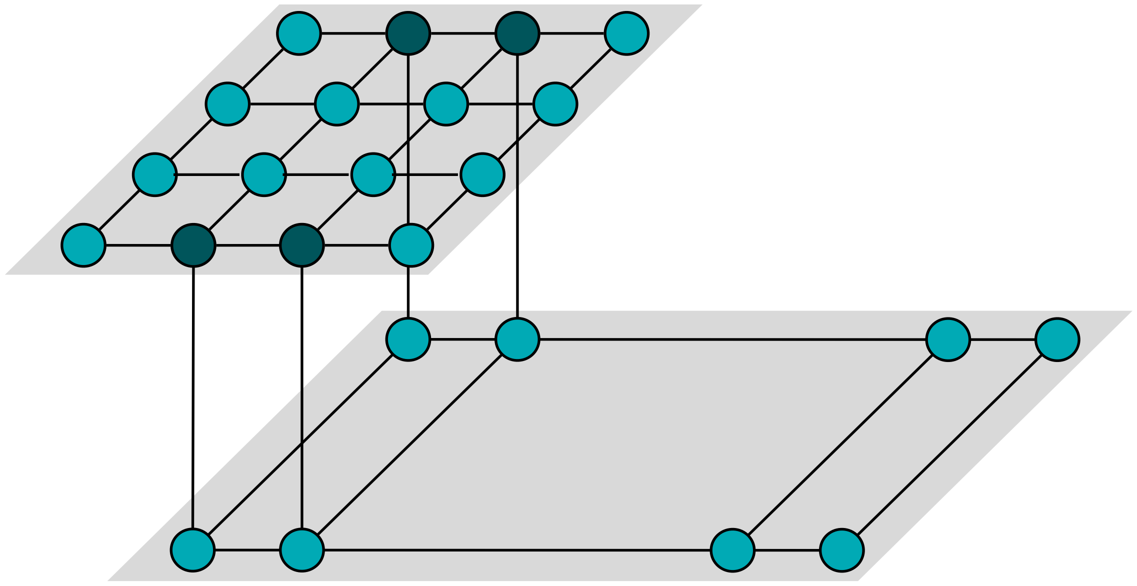

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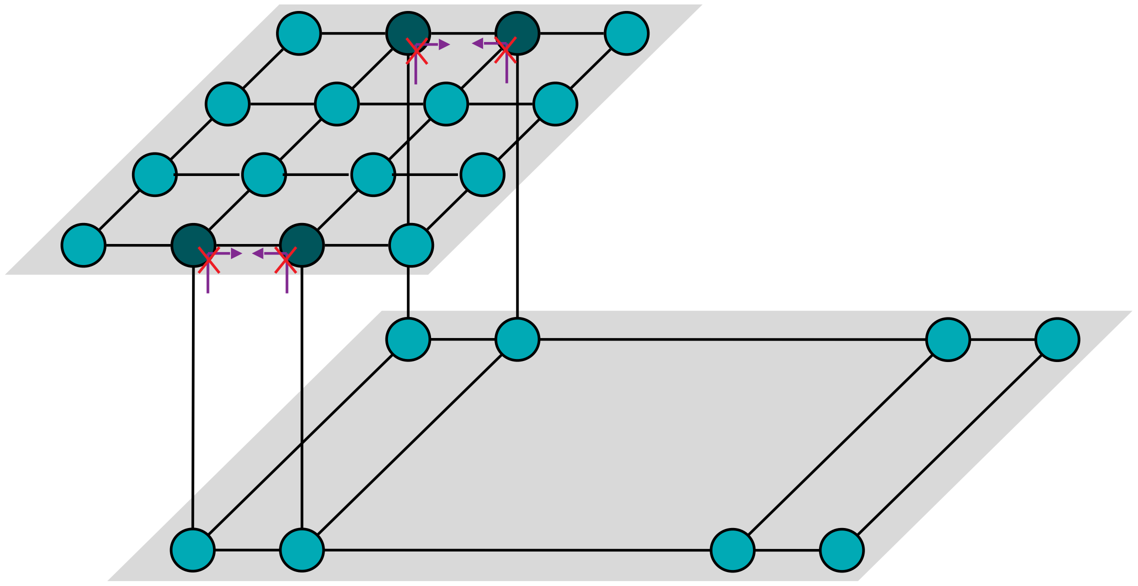

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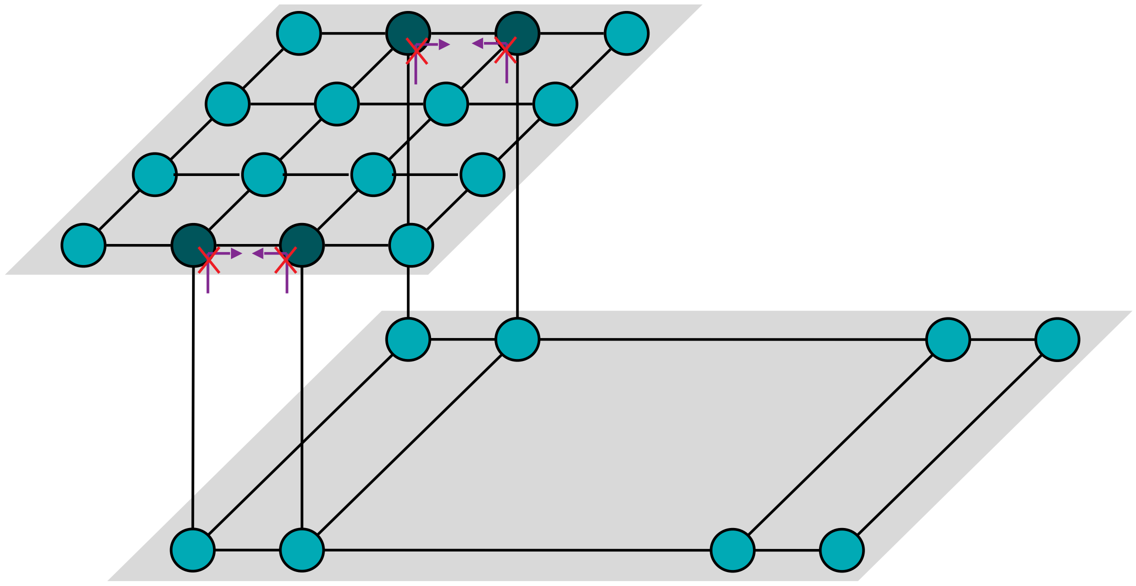
Program interposer routing tables at integration



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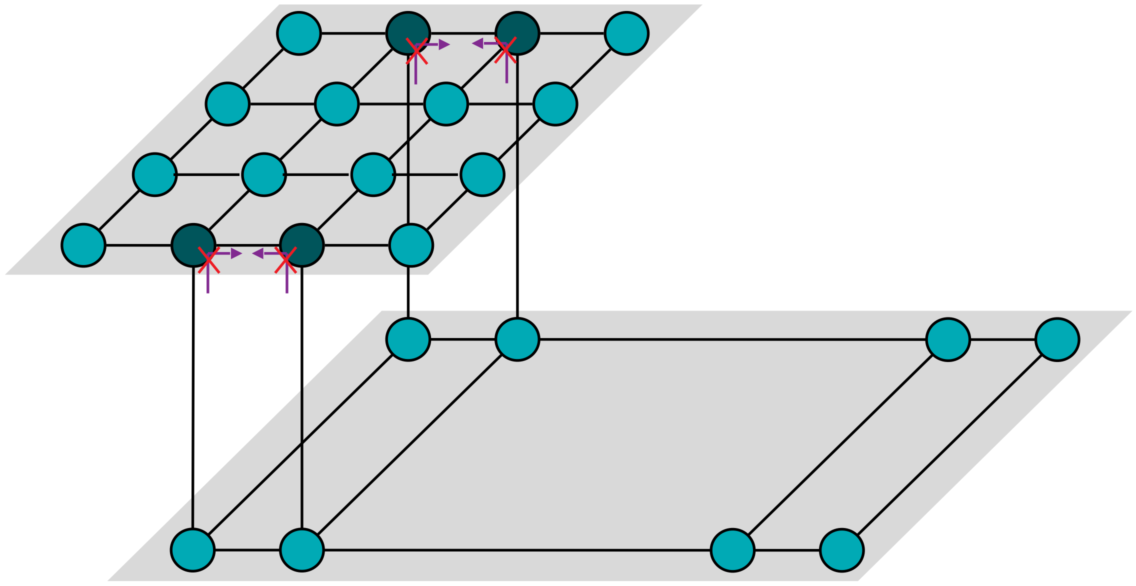

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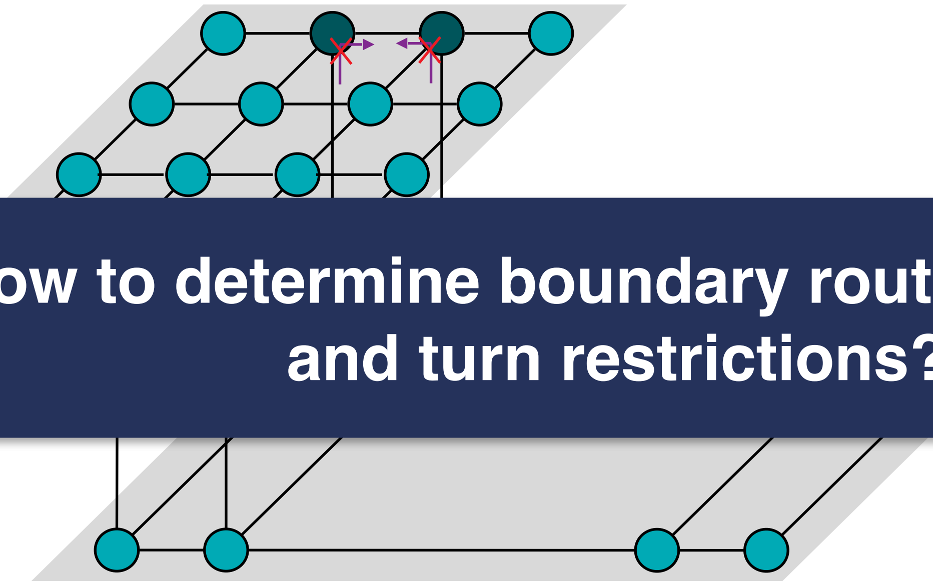

How to determine boundary router locations and turn restrictions?

Our Methodology: Composable Routing

Boundary router placement

- Physical constraints
- Load balancing
- Route distance

Turn restriction

- Distance to/from boundary node
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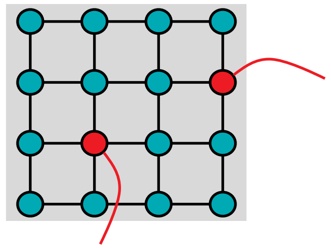

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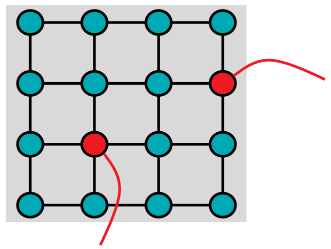

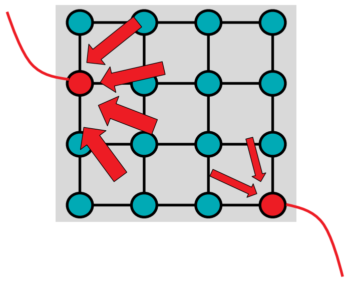

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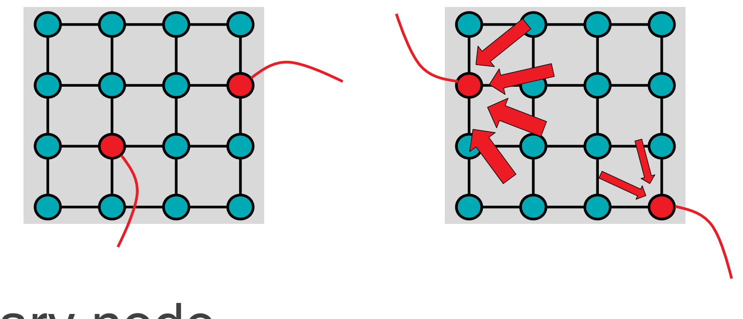

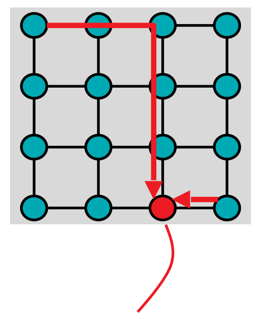

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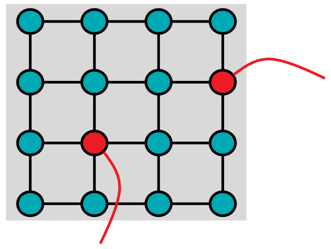

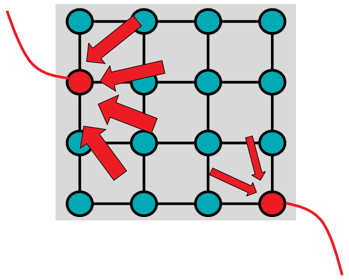

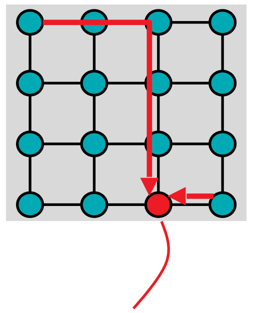

Turn restriction

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- Load balance

Objective function

- Distance
- Reachability

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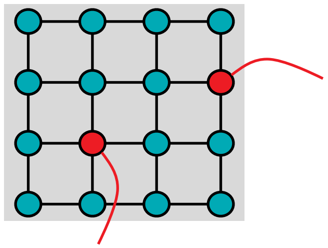

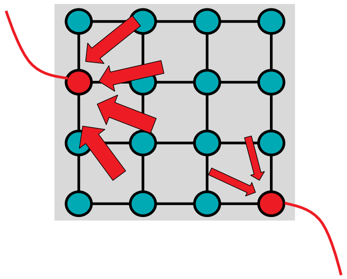

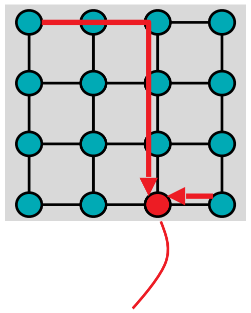

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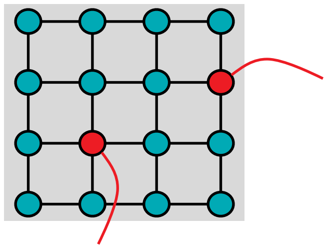

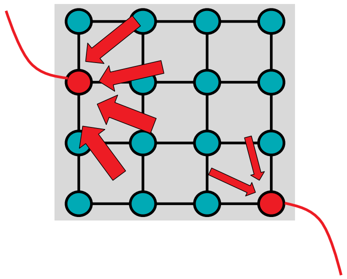

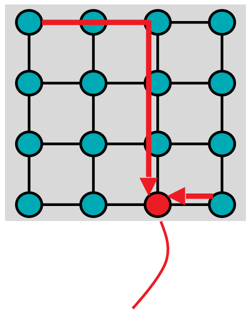

Turn restriction

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- Loa

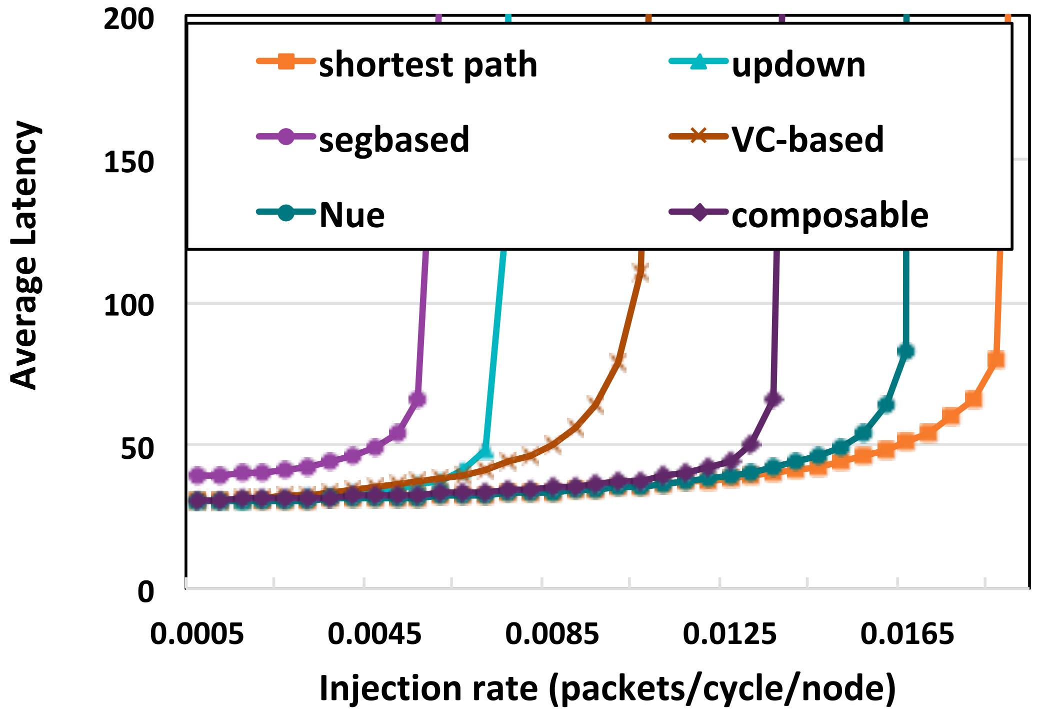
Obje

- Dist
- Rea

Our objective: minimize

$$\frac{\textit{average distance}}{\textit{average reachability}}$$

Composable Routing Take-aways



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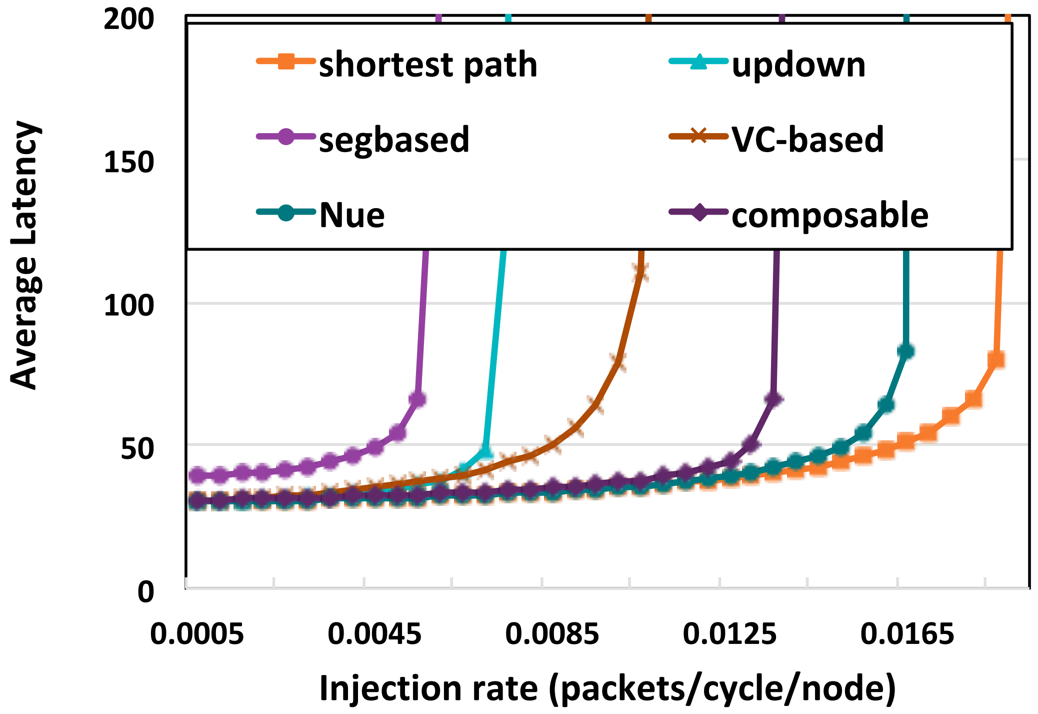

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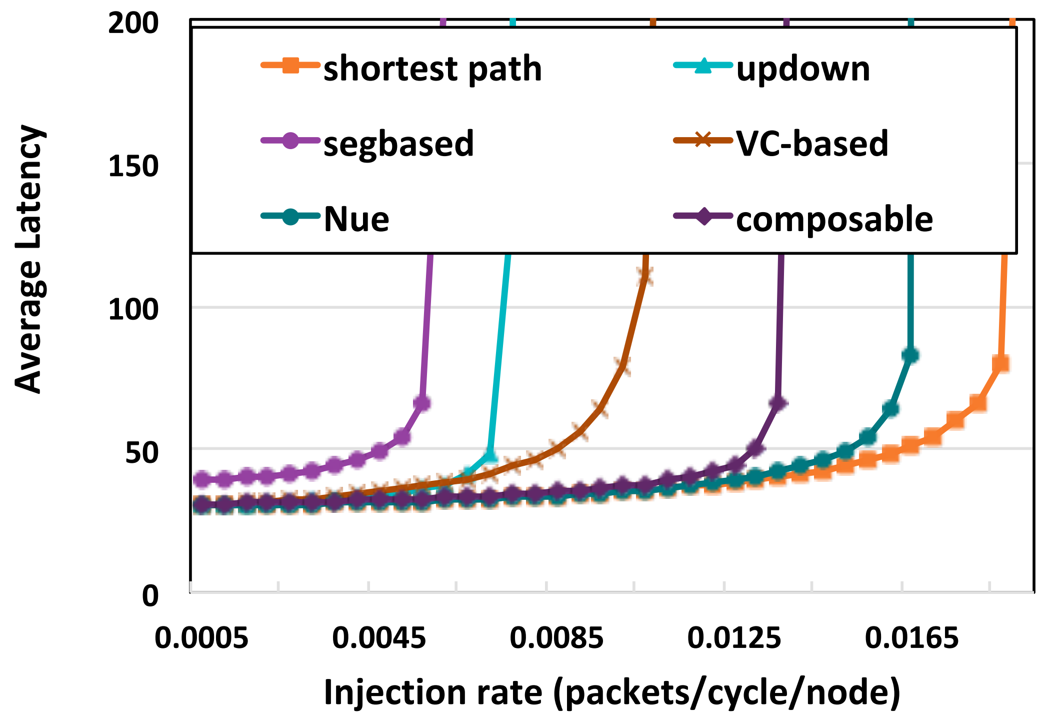

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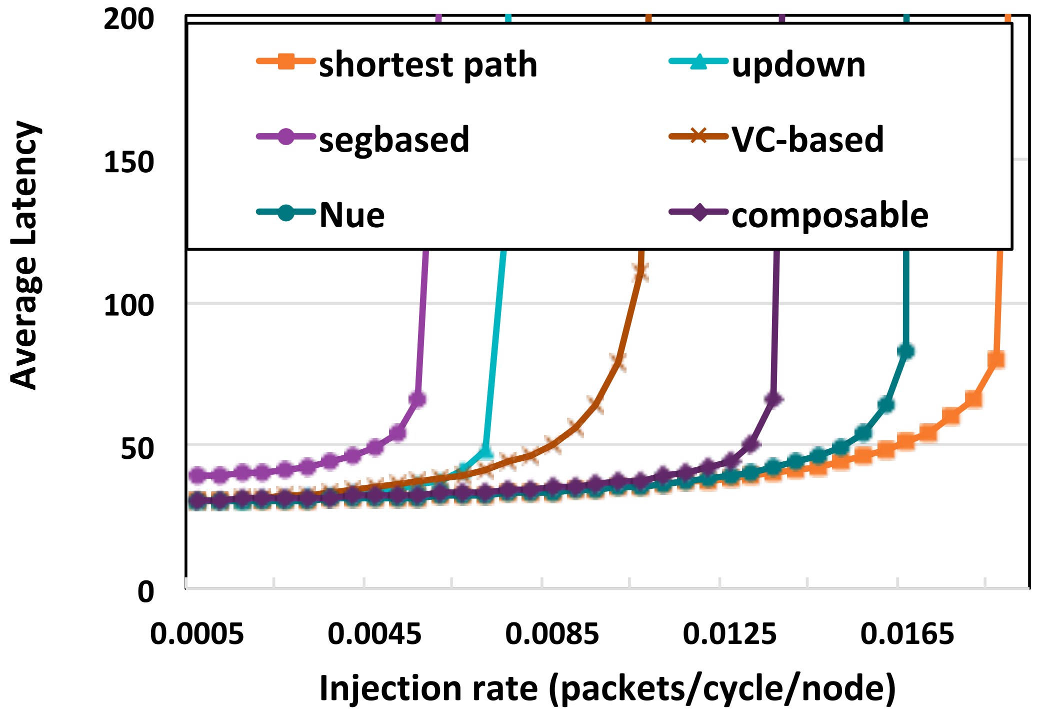

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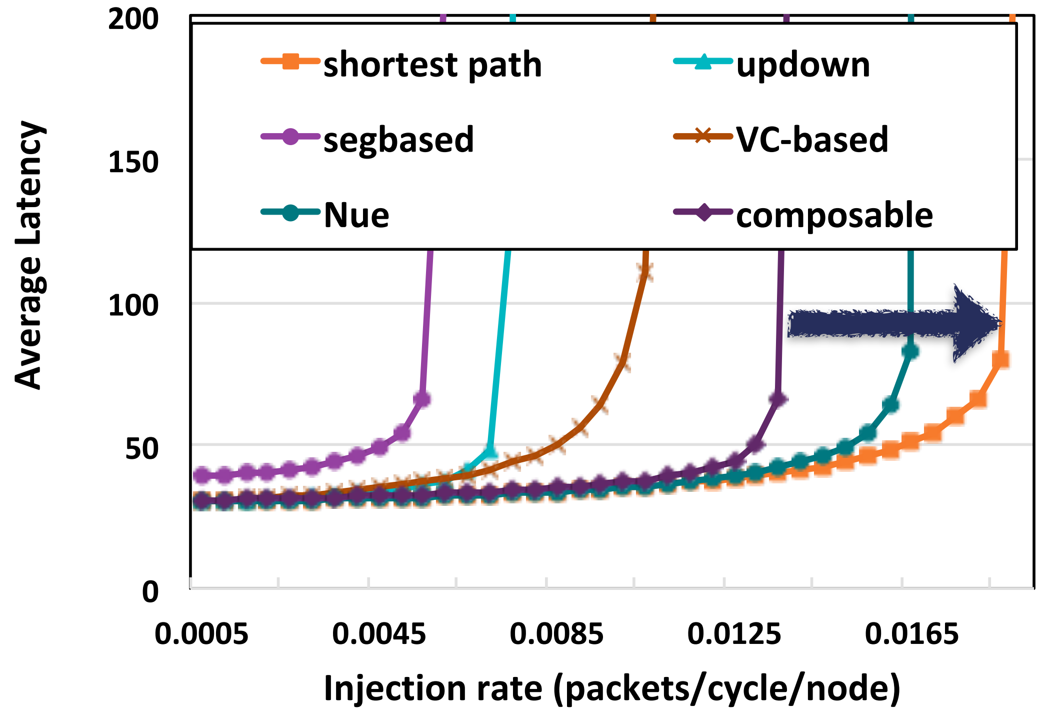

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What are the open challenges and opportunities?

Challenges: Active Interposer

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Passive interposers currently in fashion

- Can manufacture minimally active interposer with reasonable cost

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Opportunity to offload more functionality to interposer

- System monitoring, security features, auxiliary compute devices

Challenges: Process

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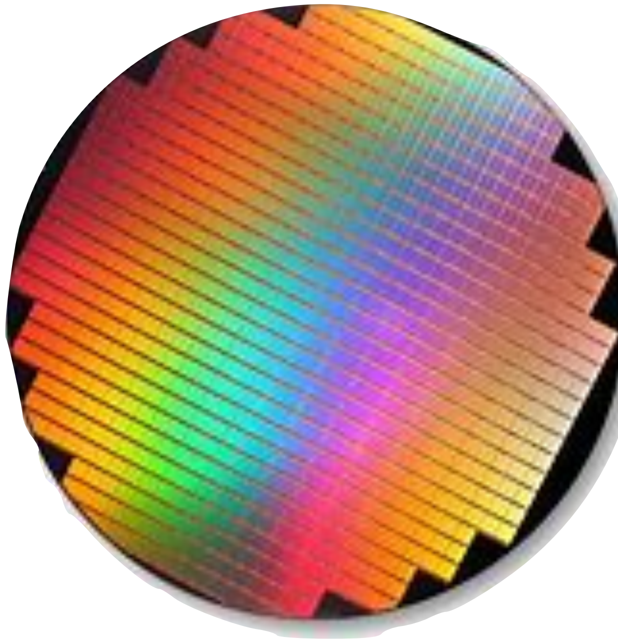
Die-to-die variations in re-integrated SoC

- Additional timing or voltage margins
- Less efficient, lower performance



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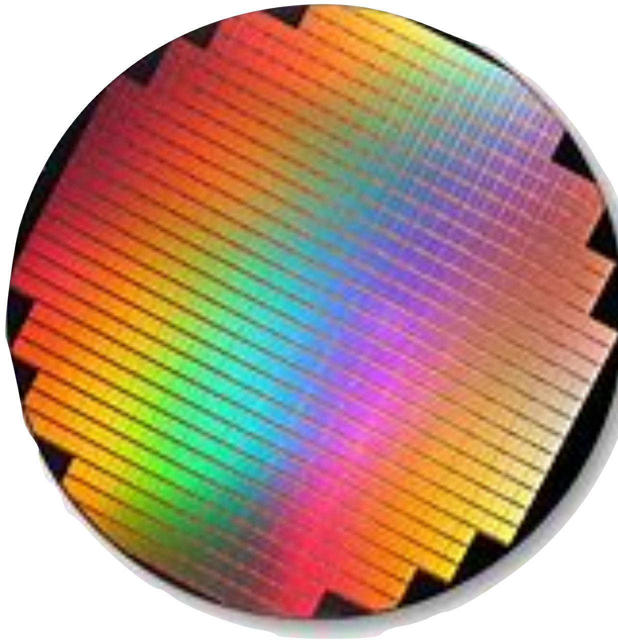

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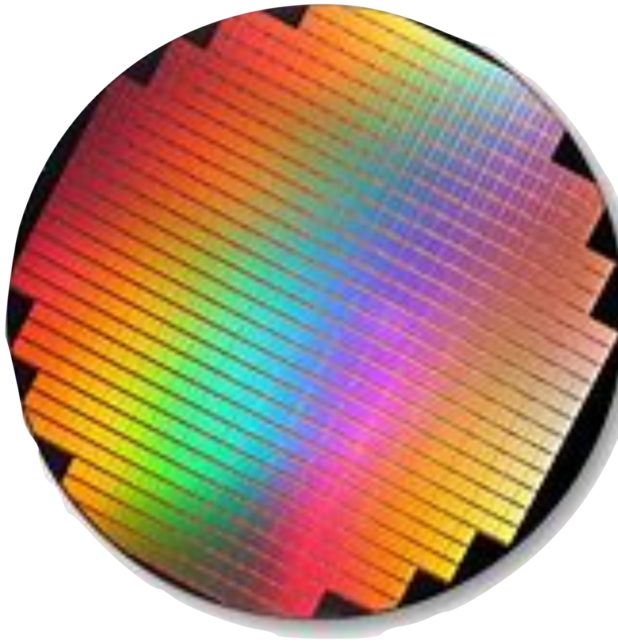
DVFS management

Mitigate overheads of clock crossings



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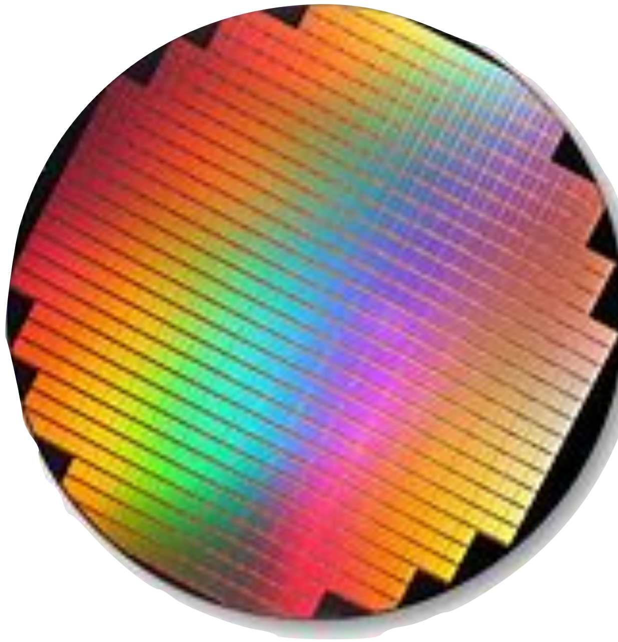

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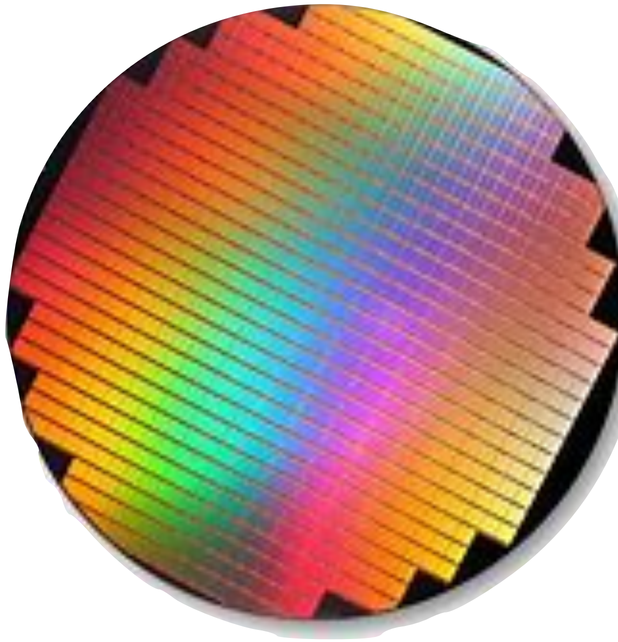

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3D NoC spanning multiple process technologies?

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Alternative chiplet placements?

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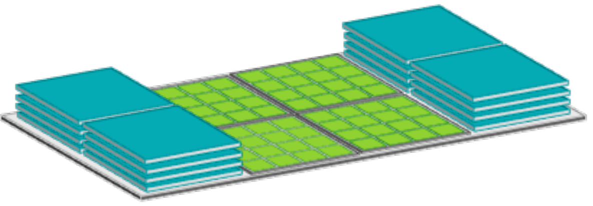

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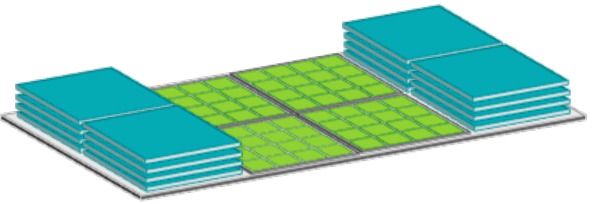

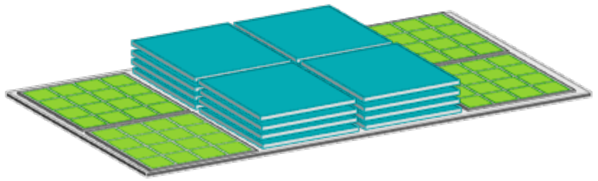

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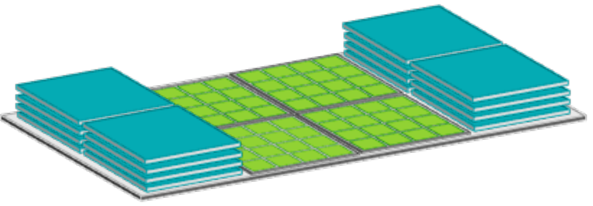
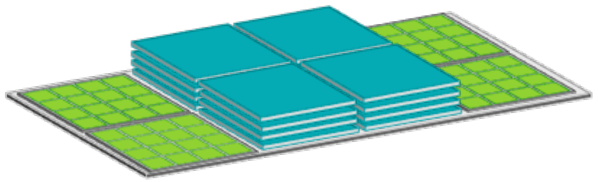
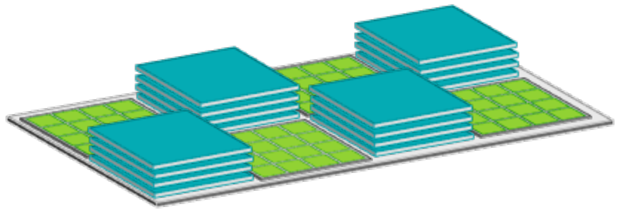

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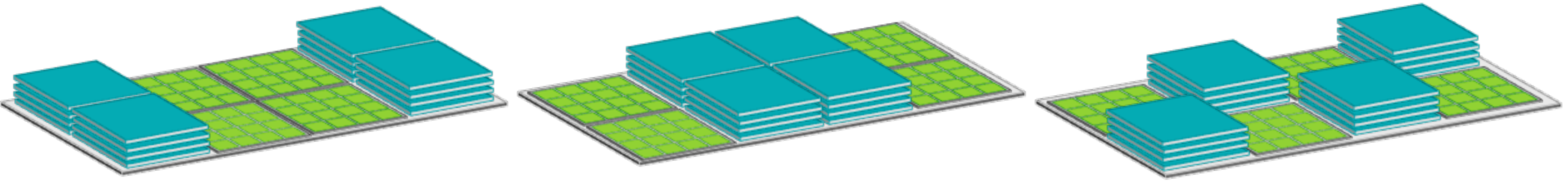

Change NoC traffic patterns — new bottlenecks, new opportunities

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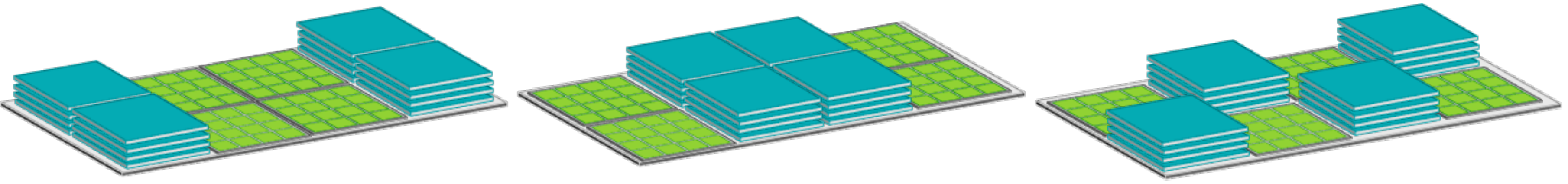
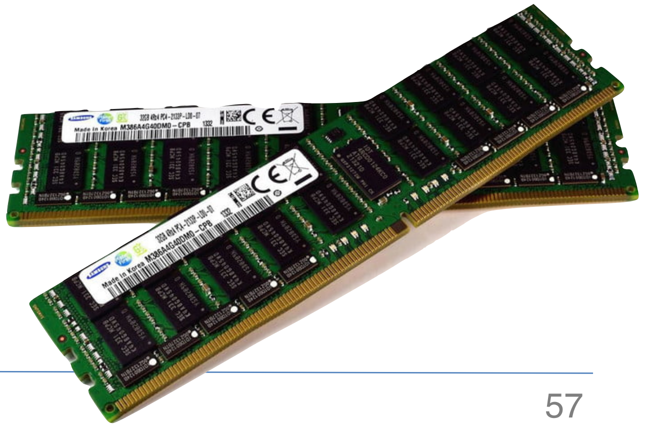


Change NoC traffic patterns — new bottlenecks, new opportunities

Interaction between in-package memory stacks and external memories?



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Additional challenges

- Interfaces
- QoS
- Coherence

Conclusions

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Disintegrate chips

Build cost-effective LARGE SoCs

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Reintegrate with an active silicon interposer

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Open questions and opportunities for research!

Acknowledgements

Graduate Students

Ajay Kannan, Zimo Li

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UofT, Natural Science and Engineering Research Council

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