NoC ArC 2015

Eighth International Workshop on

Network on Chip Architectures

To be held in conjunction with the
48th Annual IEEE/ACM International Symposium on Microarchitecture
December 6, 2015
Waikiki, Hawaii

http://nocarc.unikore.it/

General Co-Chairs

Maurizio Palesi
Kore University, Italy

Masoud Daneshtalab
Univ. of Turku, Finland, and KTH Sweden

Xiaohang Wang
South China University of Technology, China

TPC Co-Chairs

Masoumeh Ebrahimi
Univ. of Turku, Finland

Riccardo Locatelli
STMicroelectronics

Important Dates

Abstract submission deadline
September 1, 2015

Full paper submission deadline
September 8, 2015

Author notification
October 7, 2015

Camera-ready version due
October 18, 2015

NoCArc Workshop
December 6, 2015

General Information

We are now entered in the so called many-core era. The International Technology Roadmap for Semiconductors foresees that the number of Processing Elements (PEs) that will be integrated into a System-on-Chip (SoC) will be in the order of thousand within the 2020. As the number of communicating elements increases, there is a need for an efficient, scalable and reliable communication infrastructure. As technology geometries shrink to the deep submicron regime, however, the communication delay and power consumption of global interconnections become the major bottleneck. The Network-on-Chip (NoC) design paradigm, based on a modular packet-switched mechanism, can address many of the on-chip communication issues such as performance limitations of long interconnects, and integration of large number of PEs on a chip.

The goal of NoCArc workshop is to provide a forum for researchers to present and discuss innovative ideas and solutions related to design and implementation of multi-core systems on chip. The workshop will focus on issues related to design, analysis and testing of on-chip networks.

Areas of Interest

The workshop will focus on issues related to design, analysis and testing of on-chip networks. The topics of specific interest for the workshop include, but are not limited to:

NoC Architecture and Implementation
- Topologies, routing, flow control
- Managing QoS
- Timing, synchronous/asynchronous comm.
- Reliability issues
- Design methodologies and tools
- Signaling & circuit design for NoC links

NoC Analysis and Verification
- Power, energy and thermal issues
- Benchmarking with NoC-based systems
- Modeling, simulation, and synthesis
- Verification, debug and test
- Metrics and benchmarks

NoC Application
- Mapping of applications onto NoCs
- NoC case studies, application-specific NoC
- NoCs for FPGAs, CMPs and MPSoCs
- NoC designs for heterogeneous systems

On-Chip Communication Optimization
- Communication efficient algorithms
- Multi/many-core communication workload characterization and evaluation
- Energy efficient NoCs and energy minimization

NoC at System-level
- Design of memory subsystem
- NoC support for memory and cache access
- OS support for NoCs
- Programming models including shared memory, message passing and novel programming models
- Issues related to large-scale systems (datacenters, supercomputers) with NoC-based systems as building blocks

Emerging NoC Technologies
- Wireless, Optical, and RF
- NoCs for 3D and 2.5D packages

Besides regular papers, papers describing *work in progress* or incomplete but sound new innovative ideas related to the workshop theme are also encouraged.

Submission Guidelines

Both research and application-oriented papers are welcome. All papers should be submitted electronically by EasyChair. Submissions must be limited to 6 pages. Please, visit the workshop webpage for additional information about the submission process.