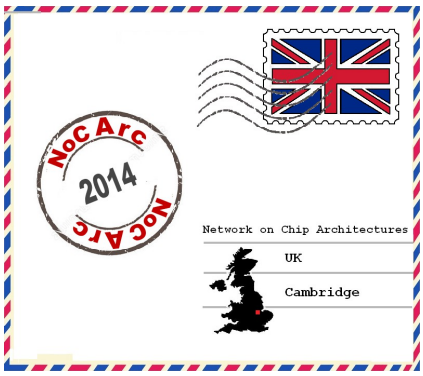

Seventh International Workshop on

Network on Chip Architectures

To be held in conjunction with the
47th Annual IEEE/ACM International Symposium on Microarchitecture
December 13 (or 14), 2014
Cambridge, UK

http://nocarc.unikore.it/

General Co-Chairs

Maurizio Palesi
Kore University, Italy

Masoud Daneshtalab
Univ. of Turku, Finland

Xiaohang Wang
Guangzhou Inst. of Advanced Technology, China

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Farhad Mehdipour
Kyushu University, Japan

Giorgos Dimitrakopoulos
Democritus University of Thrace, Greece

Publicity Chair

Masoumeh Ebrahimi
Univ. of Turku, Finland

Important Dates

Abstract submission deadline
September 1, 2014

Full paper submission deadline
September 8, 2014

Author notification
October 7, 2014

Camera-ready version due
October 18, 2014

NoCArc Workshop
December 13 or 14, 2014

General Information

Modern Systems-on-Chip (SoCs) today contains hundreds of Intellectual Properties (IPs)/cores, including, programmable processors, co-processors, accelerators, application-specific IPs, peripherals, memories, reconfigurable logic, and even analog blocks. We are now entered in the so called many-core era. The International Technology Roadmap for Semiconductors foresees that the number of Processing Elements (PEs) that will be integrated into a SoC will be in the order of thousand within the 2020. As the number of communicating elements increases, there is a need for an efficient, scalable and reliable communication infrastructure. As technology geometries shrink to the deep submicron regime, however, the communication delay and power consumption of global interconnections become the major bottleneck. The Network-on-Chip (NoC) design paradigm, based on a modular packet-switched mechanism, can address many of the on-chip communication issues such as performance limitations of long interconnects, and integration of large number of PEs on a chip.

The goal of the workshop is to provide a forum for researchers to present and discuss innovative ideas and solutions related to design and implementation of many-core systems-on-chip. This workshop will focus on issues related to design, analysis and testing of on-chip networks. We also look for new type of NoC-based computing paradigms inspired by biological systems to solve hard computational problems such as learning, recognition, and complex decision making.

Areas of Interest

The workshop will focus on issues related to design, analysis and testing of on-chip networks. We also look for new type of NoC-based computing paradigms inspired by biological systems to solve hard computational problems such as learning, recognition, and complex decision making.

The topics of specific interest for the workshop include, but are not limited to:

- Topologies selection and synthesis for NoCs and MPSoCs
- Routing algorithms and router micro-architectures
- QoS in on-chip communication
- Mapping of cores to NoC slots
- Power and energy issues
- Fault tolerance and reliability issues
- Memory architectures for NoC
- Dynamic on-chip network reconfiguration
- Modeling and evaluation of on-chip networks
- On-chip interconnection network simulators and emulators
- Analytical analysis methods for NoC performance and other properties
- Verification, debug and test of NoC
- 3D NoC architectures
- Emerging technologies and new design paradigms
- Industrial case studies of SoC designs using the NoC paradigm
- Heterogeneity
- NoC-based Brain-like computing device
- NoC-based platform for DNA sequencing
- HPC application and computer servers

Besides regular papers, papers describing work in progress or incomplete but sound new innovative ideas related to the workshop theme are also encouraged.

Submission Guidelines

Both research and application-oriented papers are welcome. All papers should be submitted electronically by EasyChair. Submissions must be limited to 6 pages. Please, visit the workshop webpage for additional information about the submission process.