Fifth International Workshop on

Network on Chip Architectures

December 1, 2012

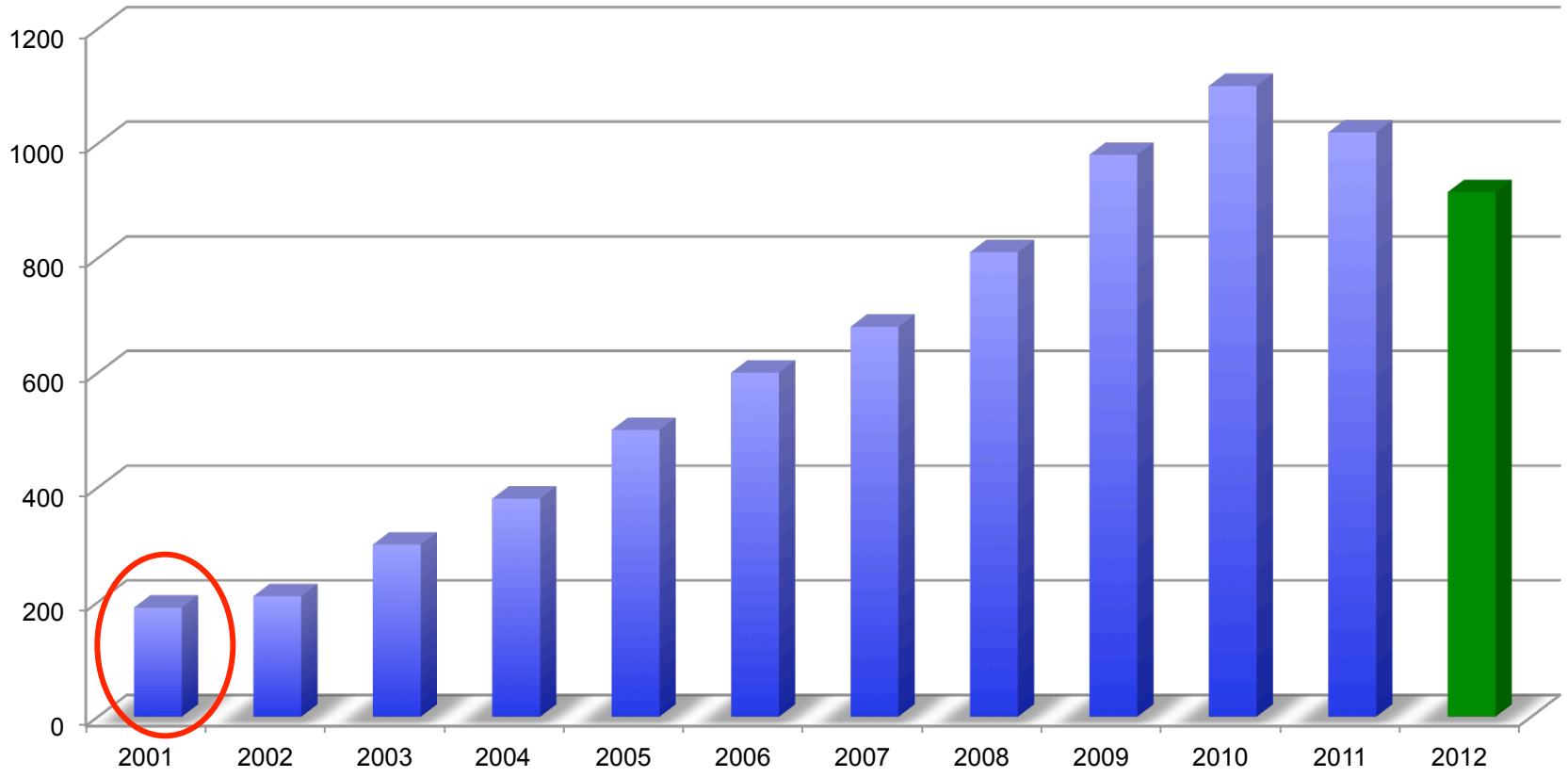
Vancouver, BC, Canada

About NoCArc

- Focus of the Workshop
  - Issues related to design, analysis and testing of on-chip networks
- Areas of Interest
  - Performance analysis
  - Routing algorithms and router micro-architectures
  - Power and energy issues
  - Fault tolerance and reliability
  - Memory architectures
  - Design space exploration and tradeoff analysis
  - Validation, debug and test
  - Industrial case studies
- Goal of the Workshop
  - To provide a forum for researchers to present and discuss innovative ideas and solutions related to design and implementation of multi-core systems on chip

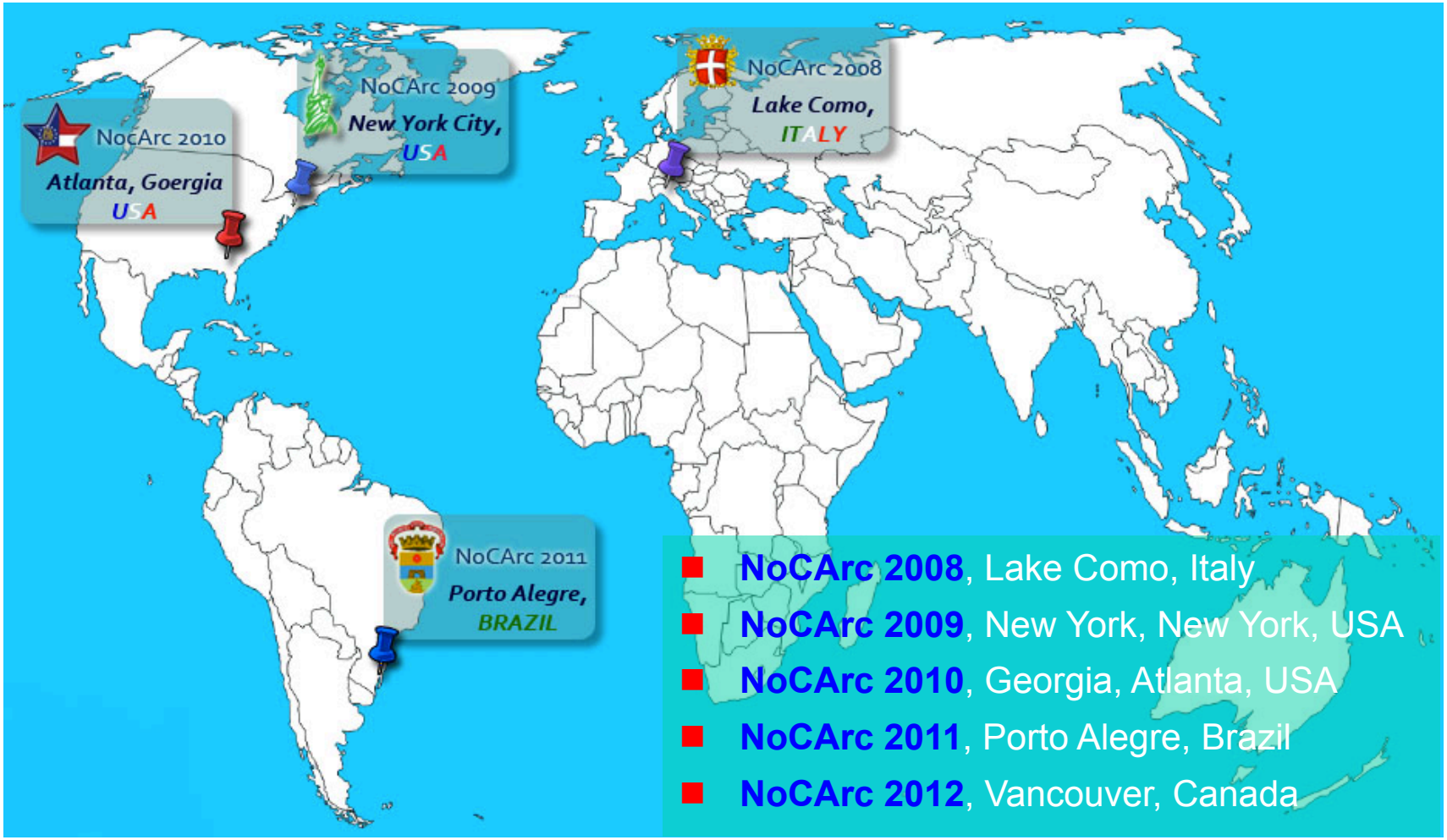
Number of Publications

Number of Publications in the NoC area (IEEE Xplorer)



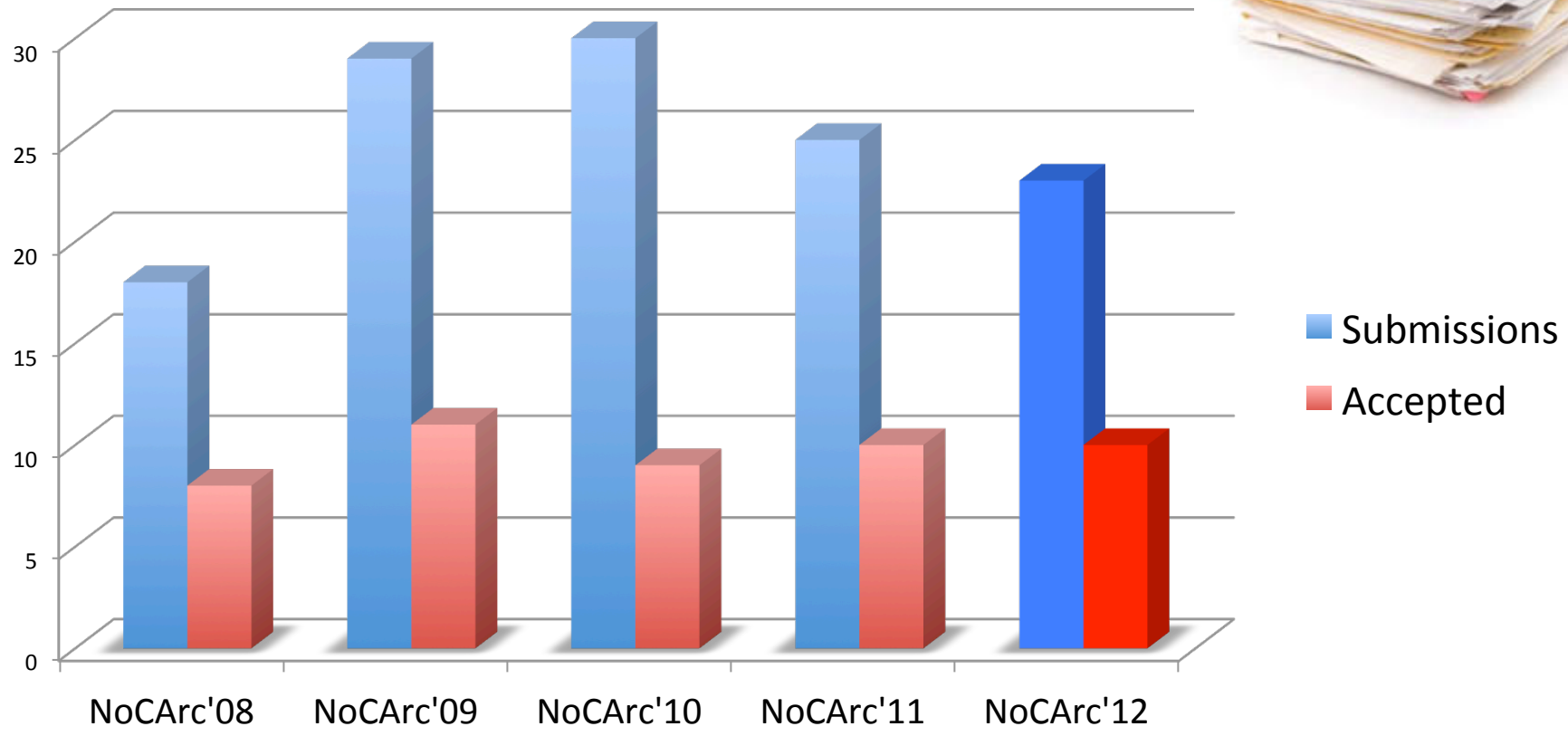
Routing Packets not Wires,
Dally and Towles, DAC'01

Past Editions

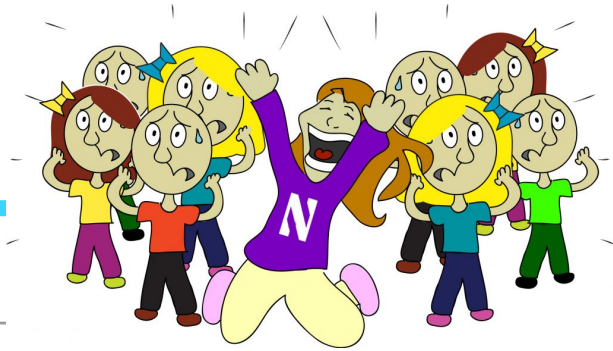


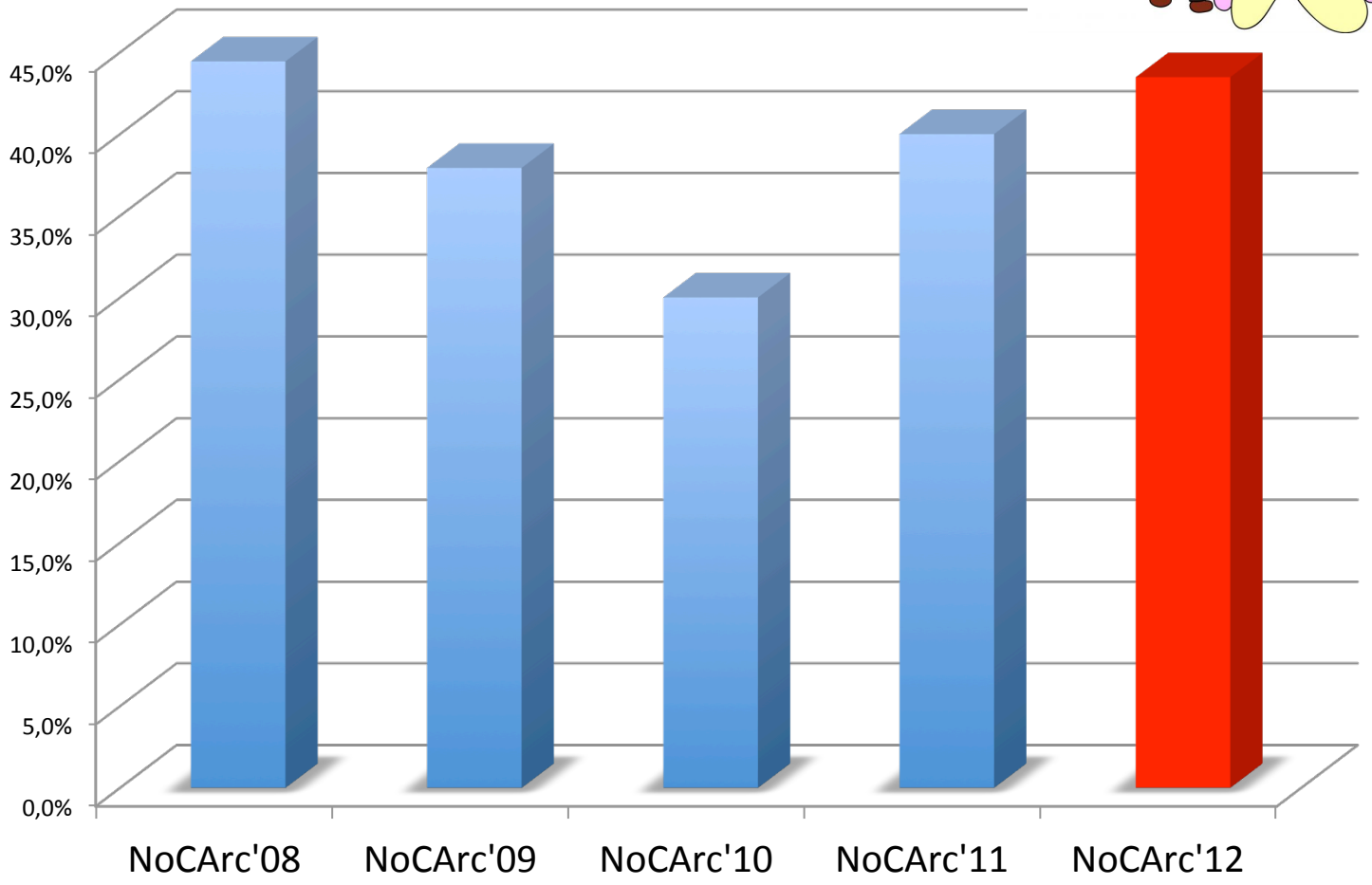
- **NoCArc 2008**, Lake Como, Italy
- **NoCArc 2009**, New York, New York, USA
- **NoCArc 2010**, Georgia, Atlanta, USA
- **NoCArc 2011**, Porto Alegre, Brazil
- **NoCArc 2012**, Vancouver, Canada

Submissions

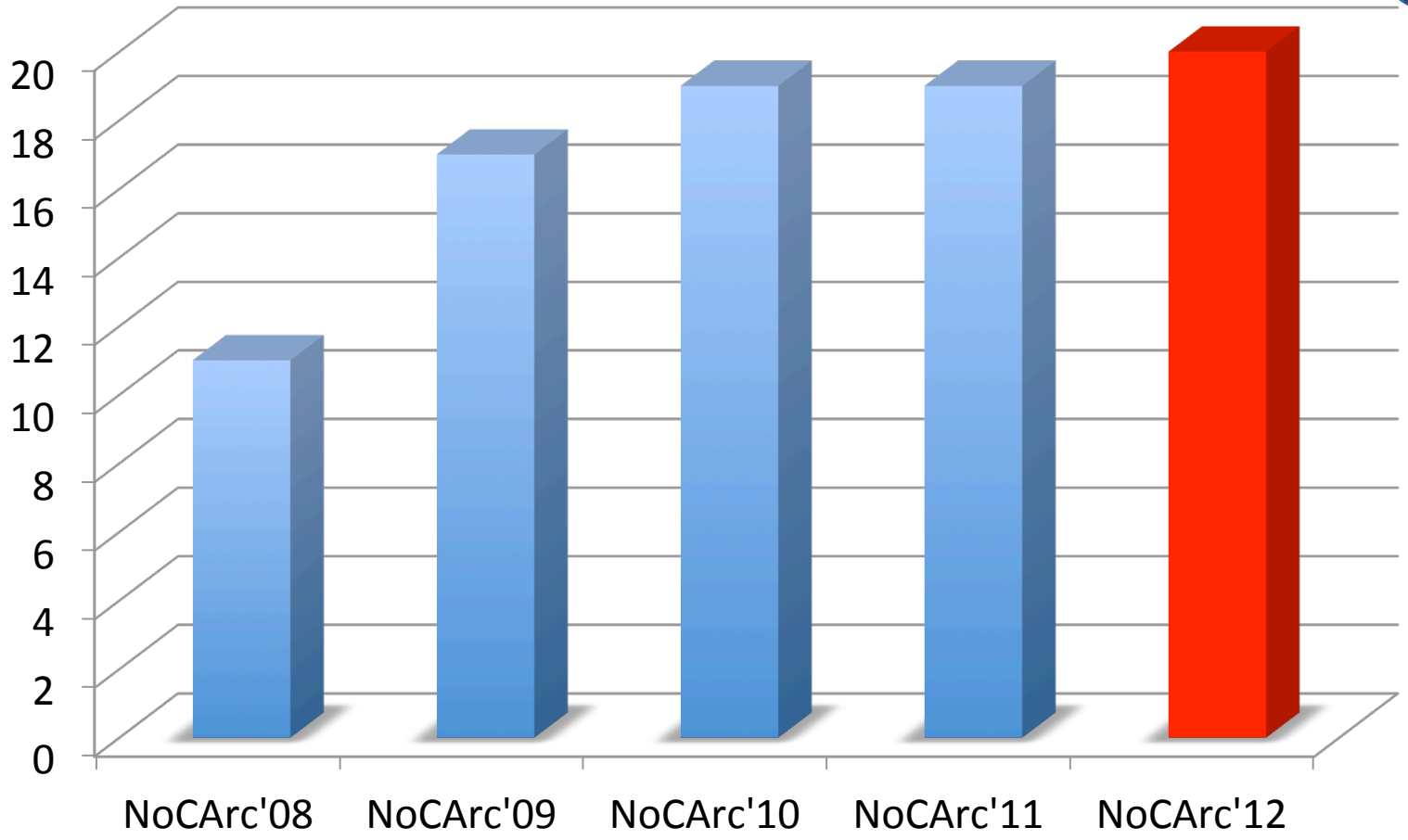


Acceptance Rate





Countries


20
18
16
14
12
10
8
6
4
2
0
NoCArc'08
NoCArc'09
NoCArc'10
NoCArc'11
NoCArc'12

Review

- 22 submissions, 29 TPC members
- Review assignment
  - ➔ Assignment based on reviewers' expertises plus slightly manual adjustment to balance the workload
  - ➔ Each paper was assigned to 4 TPC members
- All papers received 4 reviews

Paper Selection

- No face-to-face meeting for paper selection
- Selection criteria
  - ➔ Based on the review scores (average, and average weighted by reviewer's confidence)
    - ✓ Higher scored papers were accepted
- Finally, 10 papers were accepted

Program

- Sessions
  - 09:00 – 10.00 - Keynote Talk (Alex Yakovlev)
  - 10:30 - 12:10 - *Session I*
    - ✓Emerging Architectures & Technologies
  - 13:15 - 14:30 – *Session II*
    - ✓3D Design
  - 15:30 - 17:30 – *Session III*
    - ✓Arbitration, Routing and Link Design

Journal Special Issue

- IET Computer & Digital Techniques
  - ➔ Special Issue on Emerging On-Chip Networks and Architectures

Organizers and Program Committee

- Organizers and TPC Chairs
  - ➔ Maurizio Palesi, *Kore University, Italy*
  - ➔ Terrence Mak, *The Chinese University of Hong Kong*
- Technical Program Committee

Paul Ampadu, *University of Rochester, USA*
Federico Angiolini, *iNoCs, Switzerland*
Giuseppe Ascia, *University of Catania, Italy*
Davide Bertozzi, *University of Ferrara, Italy*
Masoud Daneshtalab, *University of Turku, Finland*
Giorgos Dimitrakopoulos, *Univ. of Thrace, Greece*
Masoumeh Ebrahimi, *University of Turku, Finland*
Natalie Enright Jerger, *Univ. of Toronto, Canada*
José Flich Cardo, *UPV, Spain*
Martti Forsell, *VTT, Finland*
Yuho Jin, *New Mexico State University, USA*
Shashi Kumar, *Jönköping University, Sweden*
Zhonghai Lu, *KTH, Sweden*
Radu Marculescu, *CMU, USA*
Chrysostomos Nicopoulos, *Univ. of Cyprus, Cyprus*
Juan Manuel Orduña Huertas, *UPV, Spain*
Gianluca Palermo, *Politecnico di Milano, Italy*
Partha P. Pande, *Washington State University, USA*
Sudeep Pasricha, *Colorado State University, USA*
Davide Patti, *University of Catania, Italy*
Juha Plosila, *University of Turku, Finland*
Umit Y. Ogras, *Intel Corp., USA*
Amir-Mohammad Rahmani, *Univ. of Turku, Finland*
Alberto Scandurra, *STMicroelectronics, Italy*
Christof Teuscher, *Portland State University, USA*
Xiaohang Wang, *Zhejiang University, China*
Vittorio Zaccaria, *Politecnico di Milano, Italy*

Keynote Talk

Developing Survival Instincts in Computing Systems

Alex Yakovlev

School of Electrical and Electronic Engineering Newcastle University
Newcastle upon Tyne, UK

alex.yakovlev@ncl.ac.uk

Session I (10.30 – 12.00)

- **Emerging Architectures & Technologies** (*Chair:* Chrysostomos Nicopoulos)
  - ➔**10.30** Network on Metachip Architectures (*I. Hanninen, W. Buckhanan, G. Bernstein and M. Niemier*)
  - ➔**11.00** Surface Wave Communication Systems for On-chip and Off-Chip Interconnects (*A. Karkar, T. Mak, A. Yakovlev, T. Kenneth and R. Aldujaily*)
  - ➔**11.30** A Structural Analysis of Evolved Complex Networks-on-Chip (*H. Chung, A. P. Asnodkar and C. Teuscher*)

Session II (13.30 – 15.00)

- **3D Design** (*Chair:* Jing-Jia Liou)
  - ➔**13.30** Power Efficiency of Wavelength-Routed Optical NoC Topologies for Global Connectivity of 3D Multi-Core Processors (*L. Ramini, D. Bertozzi*)
  - ➔**14.00** Deadlock-Free and Plane-Balanced Adaptive Routing for 3D Networks-on-Chip (*N. Dahir, T. Mak, A. Yakovlev, R. AlDujaily and P. Missailidis*)
  - ➔**14.30** A High-Efficiency Low-Cost Heterogeneous 3D Network-on-Chip Design (*T. C. Xu, P. Liljeberg, J. Plosila and H. Tenhunen*)

Session III (15.30 – 17.00)

- **Arbitration, Routing & Link Design** (*Chair:* Alex Yakovlev)
  - ~~**15.30** Junction Based Routing: A Scalable Technique to Support Source Routing in Large NoC Platforms (*S. Badri, R. Holsmark and S. Kumar*)~~
  - **15.30** Position-Based Weighted Round-Robin Arbitration for Equality of Service in Many-Core Network-on-Chips (*H. Park and K. Choi*)
  - **16.00** Variability-Tolerant NoC Link Design (*E. Kamel, M. El-Kharashi and M. Abuelyazeed*)
  - **16.30** Low Power Flitwise Routing in an Unidirectional Torus with Minimal Buffering (*J. Mische and T. Ungerer*)