

Low Power Flitwise Routing in an Unidirectional Torus with Minimal Buffering

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Motivation

On-chip Networks for Embedded Systems

- ▶ Connect small cores by a NoC
- ▶ Routers must be small and power-efficient, too

Alternative Router Design

- ▶ Reduce area and power consumption
- ▶ Reduce complexity of router
- ▶ Provide acceptable network throughput

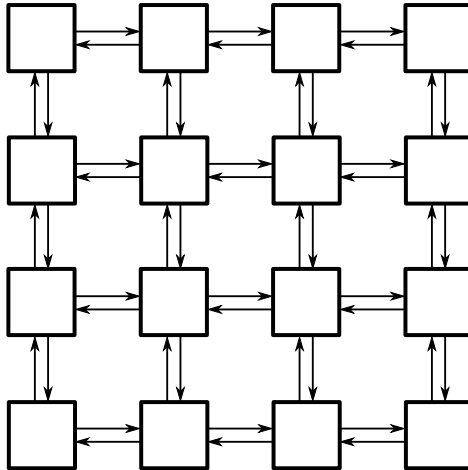


Router Microarchitecture

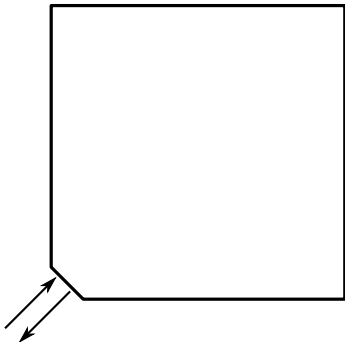
Routing Algorithm

Evaluation of Throughput and Costs

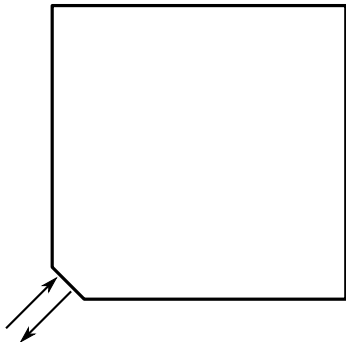
Conventional Router in a Mesh



Conventional Router Architecture

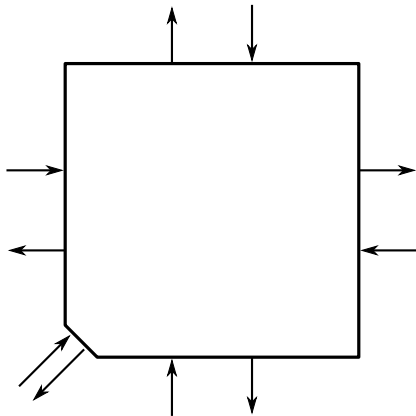


Conventional Router Architecture



mesh

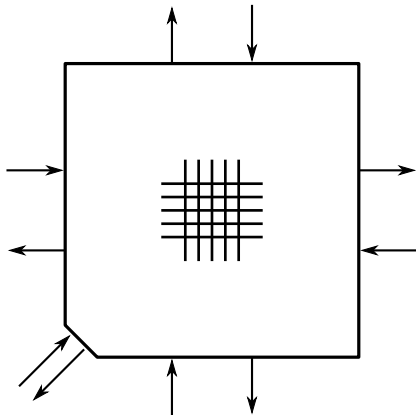
Conventional Router Architecture



mesh

- ▶ 4+1 input ports,
4+1 output ports

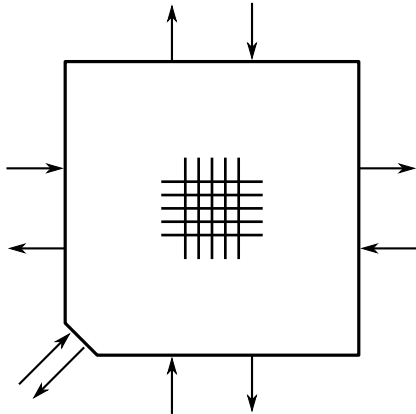
Conventional Router Architecture



mesh

- ▶ 4+1 input ports,
4+1 output ports
- ▶ 5x5 crossbar

Conventional Router Architecture

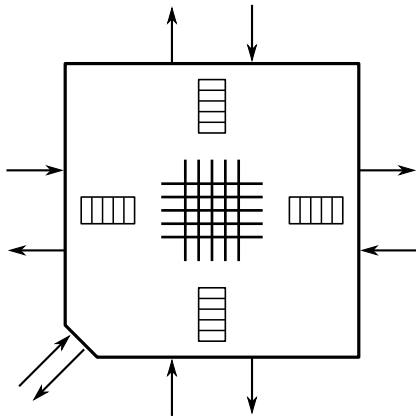


mesh

- ▶ 4+1 input ports,
4+1 output ports
- ▶ 5x5 crossbar

wormhole routing

Conventional Router Architecture



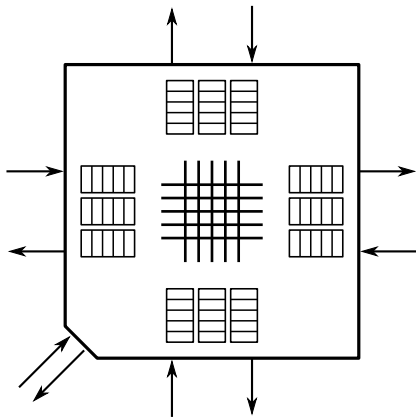
mesh

- ▶ 4+1 input ports,
4+1 output ports
- ▶ 5x5 crossbar

wormhole routing

- ▶ input or output buffers

Conventional Router Architecture



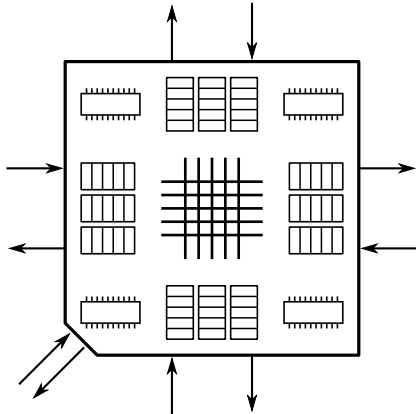
mesh

- ▶ 4+1 input ports,
4+1 output ports
- ▶ 5x5 crossbar

wormhole routing

- ▶ input or output buffers
- ▶ buffers for
virtual channels

Conventional Router Architecture



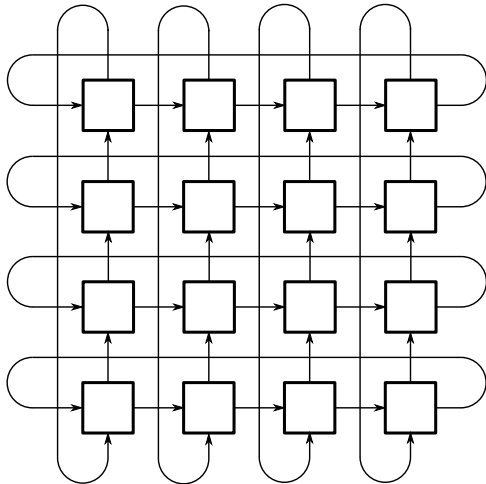
mesh

- ▶ 4+1 input ports,
4+1 output ports
- ▶ 5x5 crossbar

wormhole routing

- ▶ input or output buffers
- ▶ buffers for
virtual channels
- ▶ pipelined logic

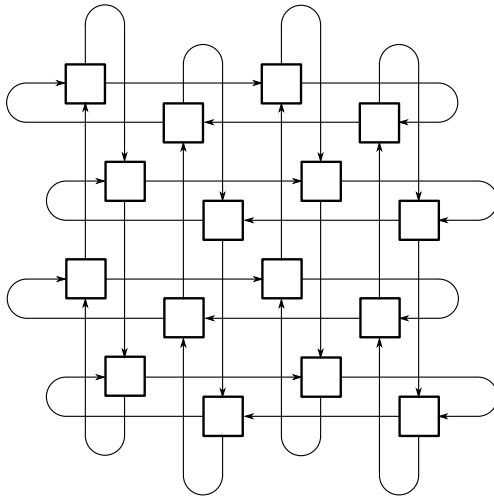
Unidirectional Torus

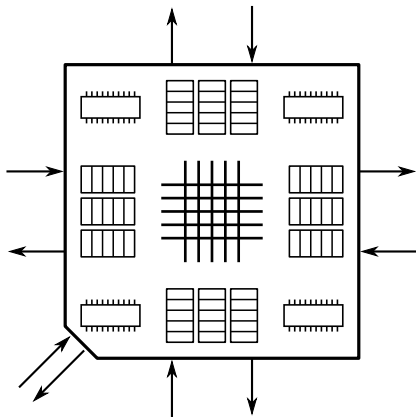


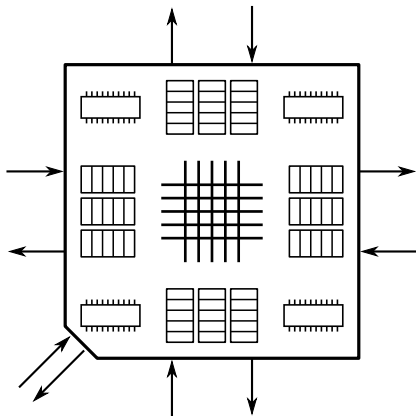
comparison with mesh

	bidirectional	
1×	bandwidth	o
0.5×	#ports/links	+
2×	link length	-
1×	link area	o
0.5×	link capacity	-

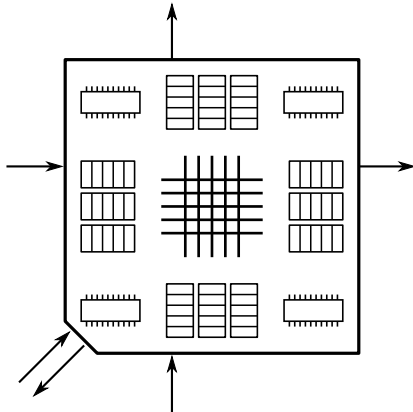
Folded Unidirectional Torus





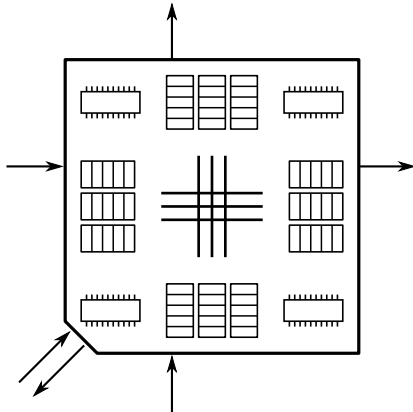


unidirectional torus



unidirectional torus

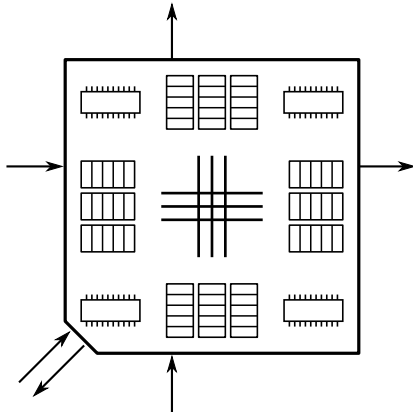
- ▶ 2+1 input ports,
2+1 output ports



unidirectional torus

- ▶ 2+1 input ports,
2+1 output ports
- ▶ 3x3 crossbar

Reducing Router Complexity

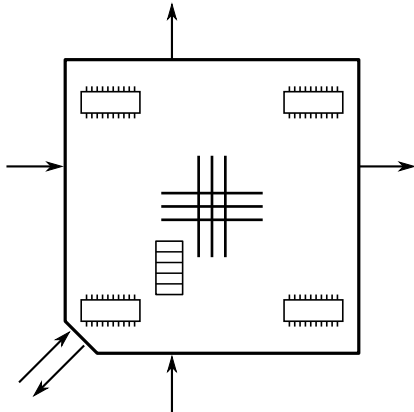


unidirectional torus

- ▶ 2+1 input ports, 2+1 output ports
- ▶ 3x3 crossbar

semi-bufferless routing

Reducing Router Complexity



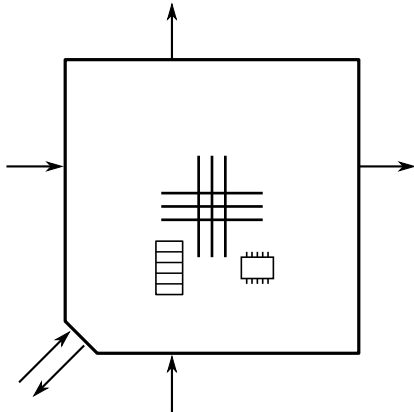
unidirectional torus

- ▶ 2+1 input ports,
2+1 output ports
- ▶ 3x3 crossbar

semi-bufferless routing

- ▶ 1 buffer

Reducing Router Complexity

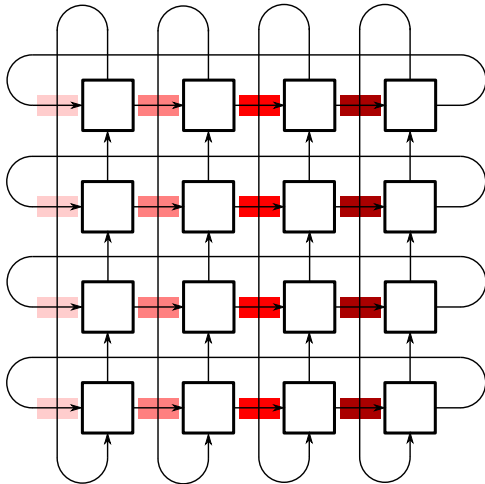


unidirectional torus

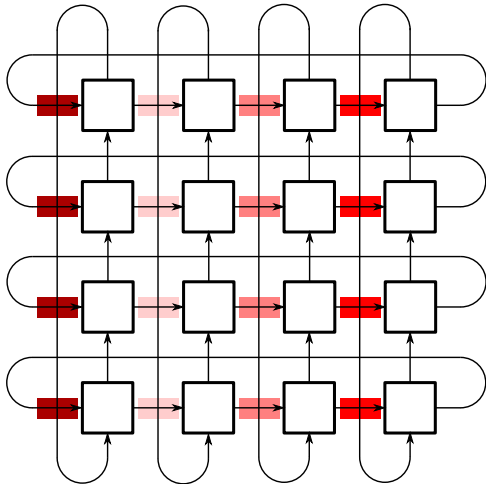
- ▶ 2+1 input ports,
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semi-bufferless routing

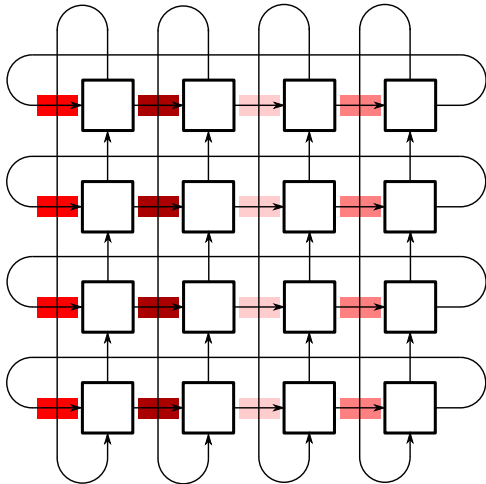
- ▶ 1 buffer
- ▶ simplified routing logic



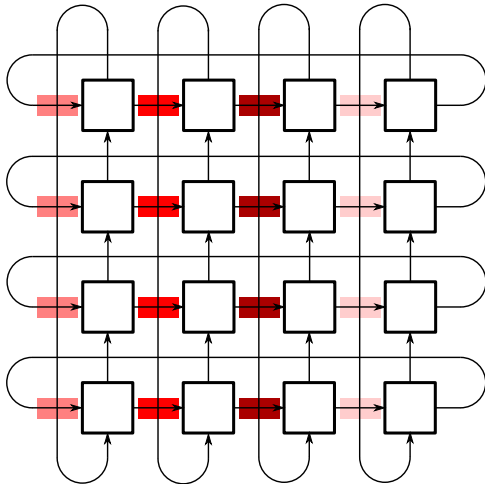
- ▶ constantly rotating x-rings



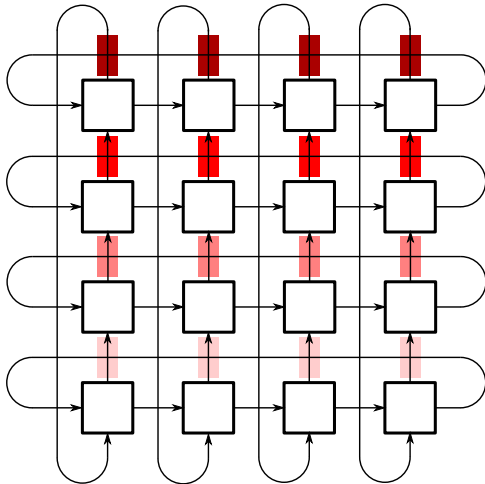
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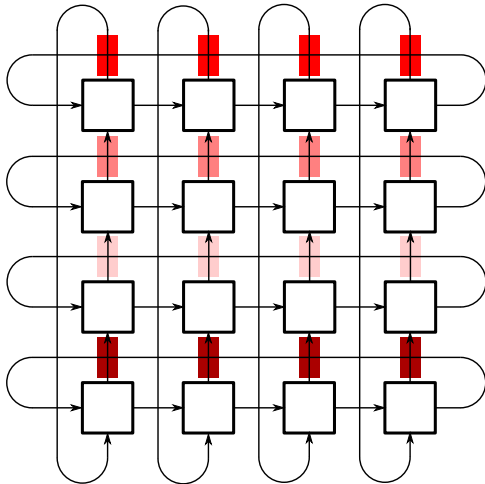
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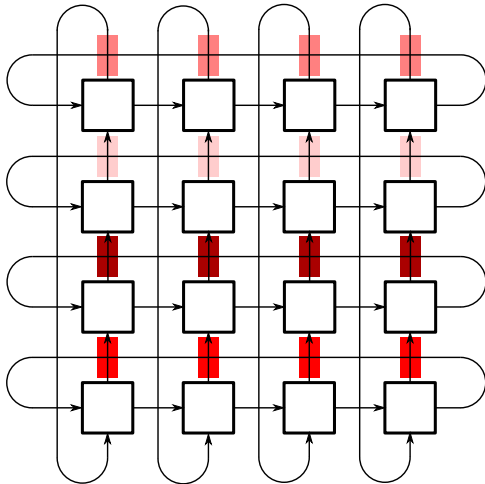
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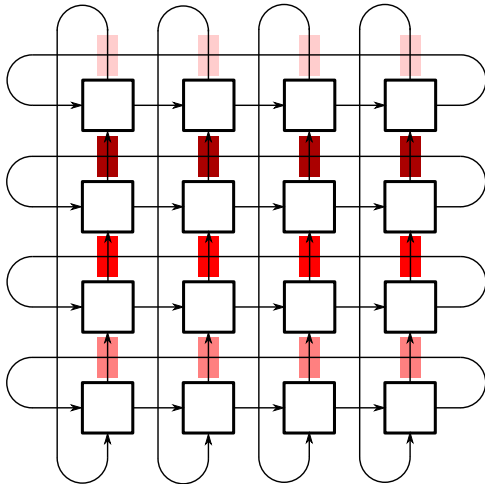
- ▶ constantly rotating x-rings
- ▶ constantly rotating y-rings



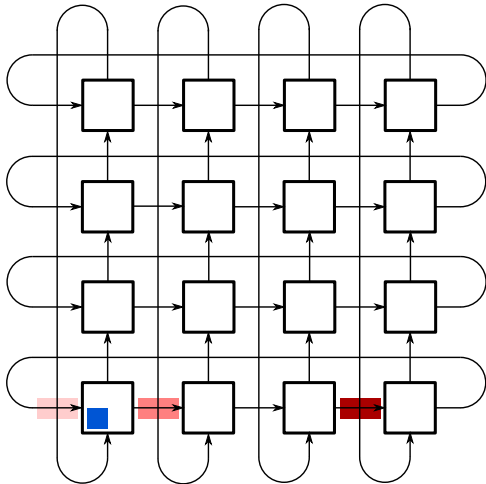
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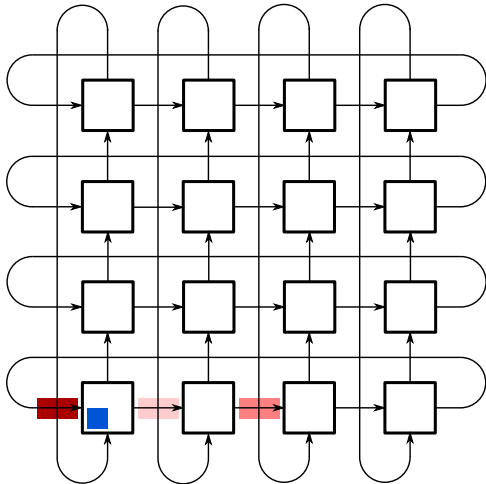
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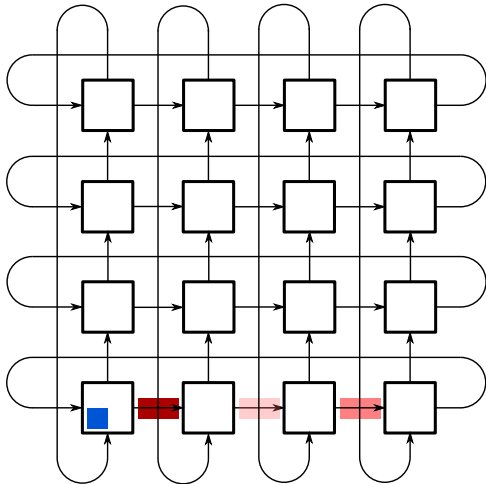
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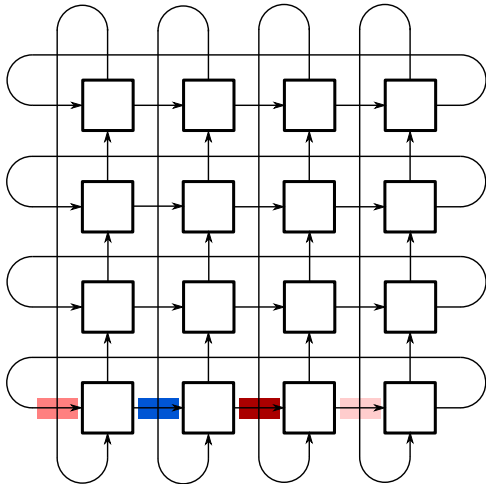
- ▶ constantly rotating x-rings
- ▶ constantly rotating y-rings
- ▶ enter x-ring if empty slot



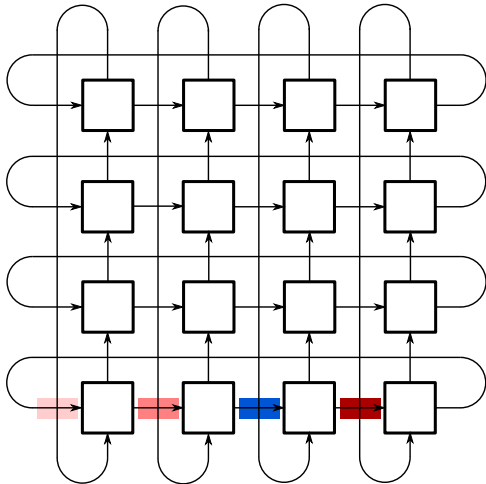
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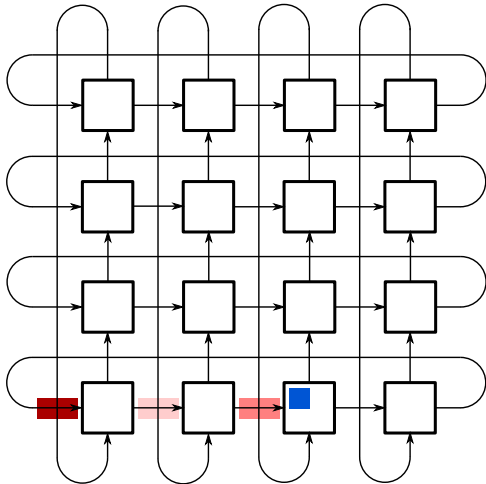
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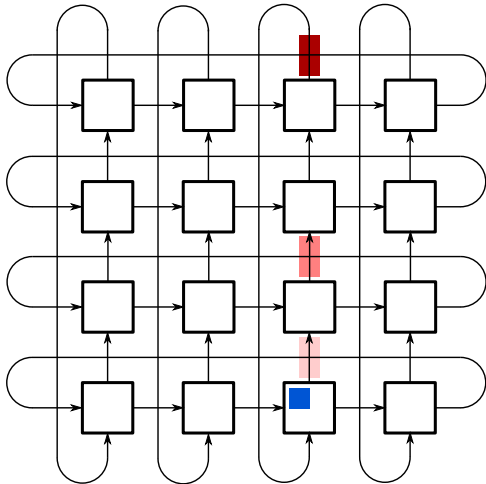
- ▶ constantly rotating x-rings
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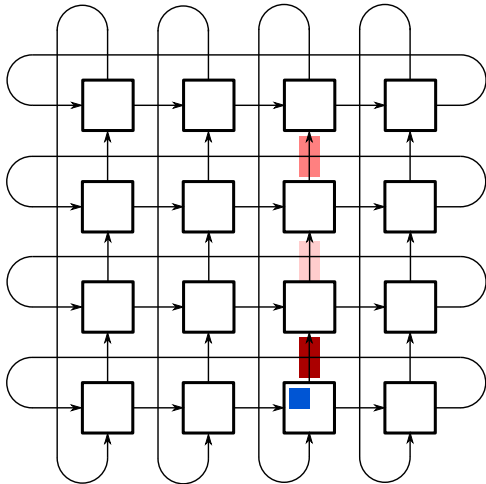
- ▶ constantly rotating x-rings
- ▶ constantly rotating y-rings
- ▶ enter x-ring if empty slot
- ▶ x transport



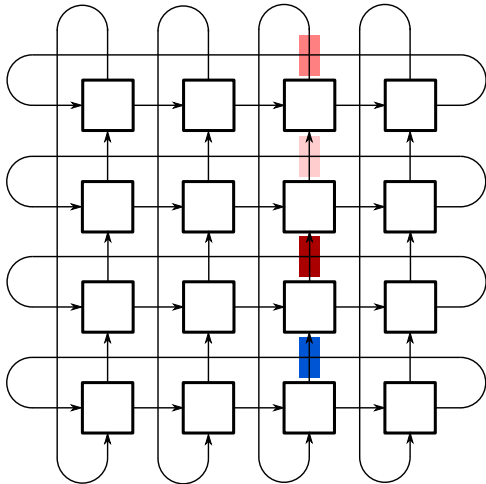
- ▶ constantly rotating x-rings
- ▶ constantly rotating y-rings
- ▶ enter x-ring if empty slot
- ▶ x transport
- ▶ turn to corner buffer



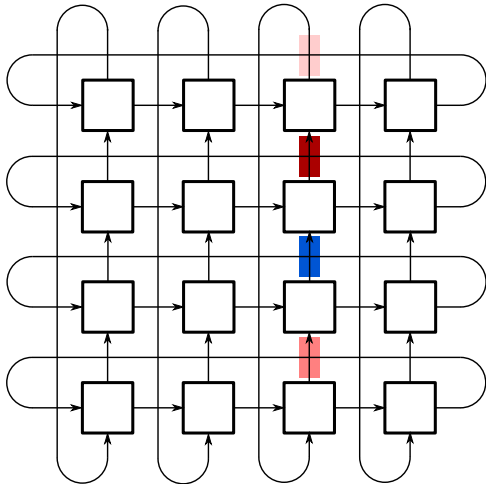
- ▶ constantly rotating x-rings
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- ▶ enter x-ring if empty slot
- ▶ x transport
- ▶ turn to corner buffer
- ▶ enter y-ring if empty slot



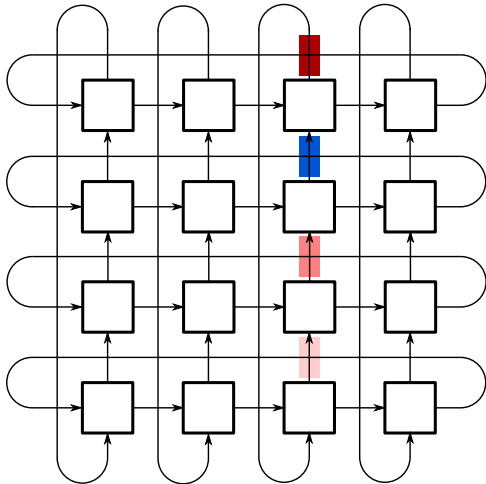
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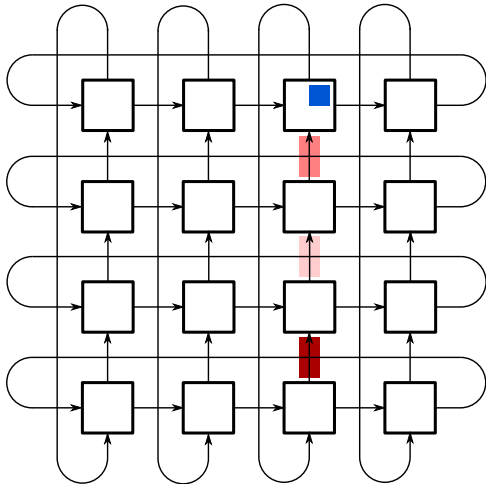
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- ▶ enter y-ring if empty slot
- ▶ y transport



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- ▶ x transport
- ▶ turn to corner buffer
- ▶ enter y-ring if empty slot
- ▶ y transport

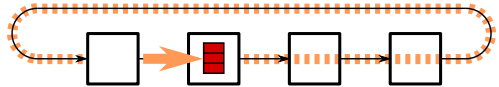


- ▶ constantly rotating x-rings
- ▶ constantly rotating y-rings
- ▶ enter x-ring if empty slot
- ▶ x transport
- ▶ turn to corner buffer
- ▶ enter y-ring if empty slot
- ▶ y transport
- ▶ eject

Conflicts

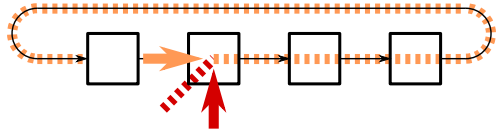
Corner buffer full

→ extra round



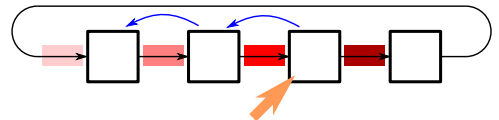
Conflict at local eject port

→ extra round



No free slot

→ request from predecessor



Flow Control

Single Flit Packets

- ▶ Enable large data chunks by preserving flit order
- ▶ Simplify flow control

Preserving flit order

- ▶ Fixed route (X-Y)
- ▶ Preserve order in extra rounds

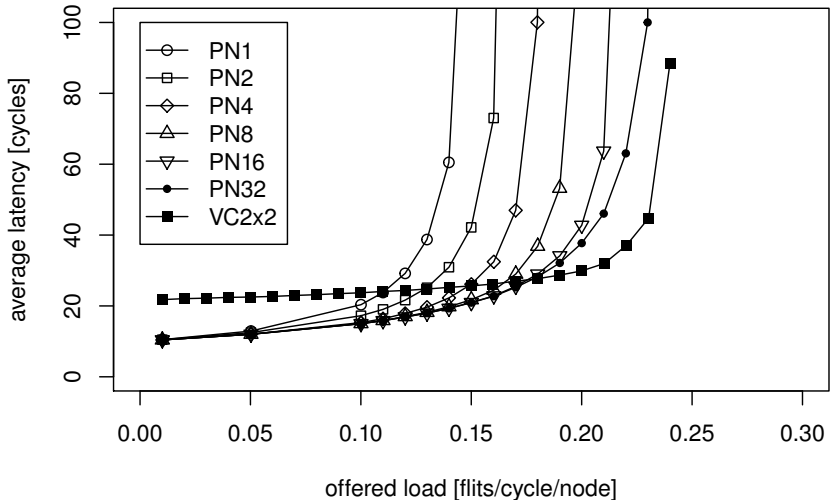
Overhead

- ▶ Each flit carries destination → increase link width
- ▶ In return: save head flit

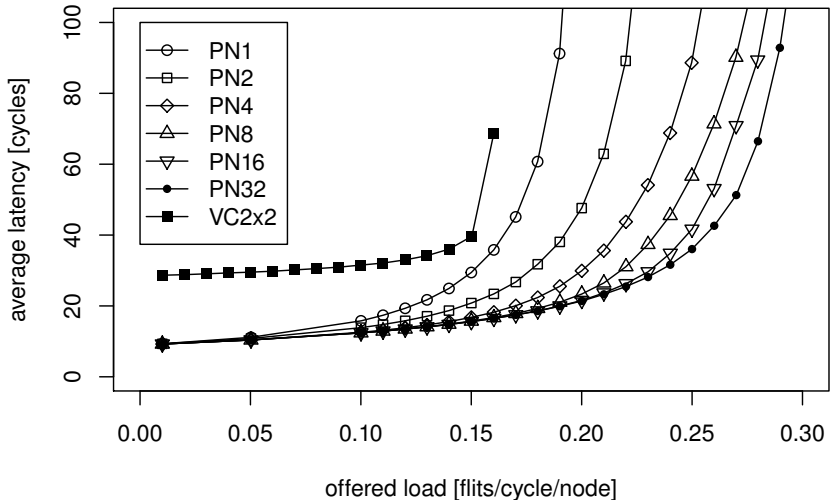


- ▶ Main focus: comparability with other low power router publications
- ▶ Baseline: conventional router with 2 buffers per input port and 2 virtual channels (VC2x2)
- ▶ Throughput: synthetic traffic patterns from booksim
- ▶ Power/area: Orion 2.0 at 65nm

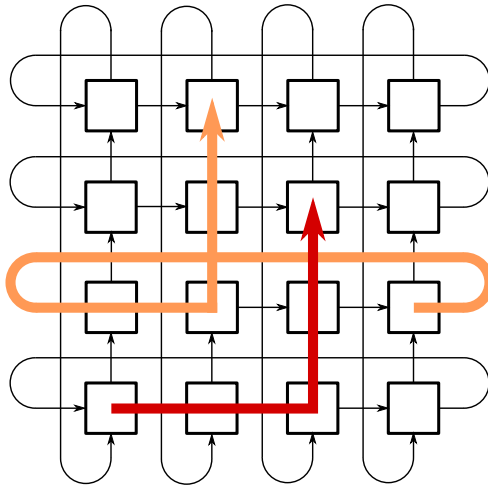
Uniform Random Traffic



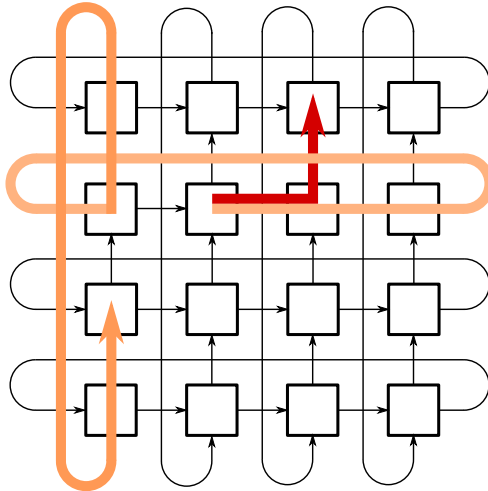
Tornado Traffic

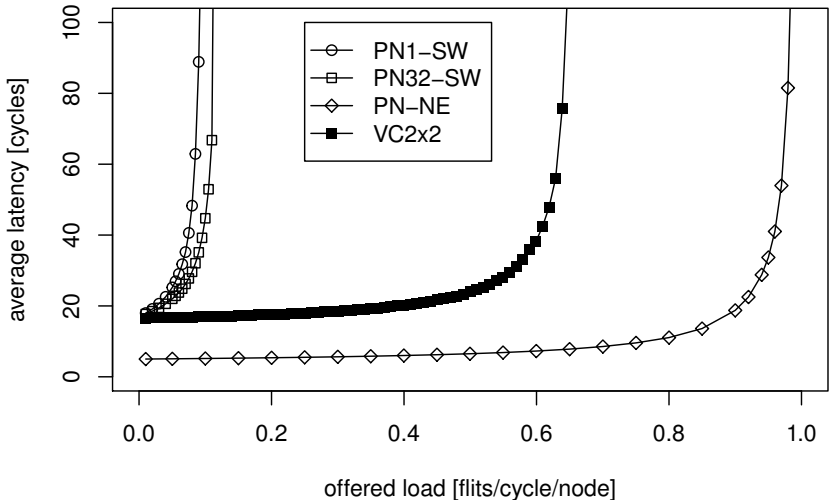


Tornado Traffic Pattern

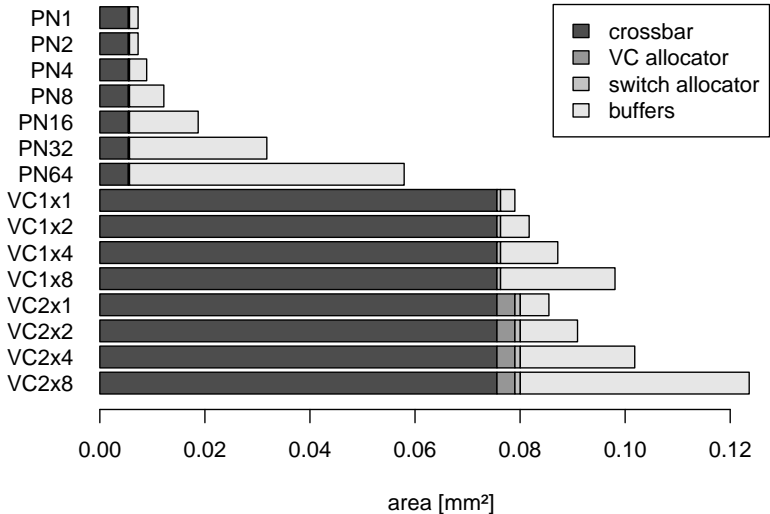


Neighbor Traffic Pattern

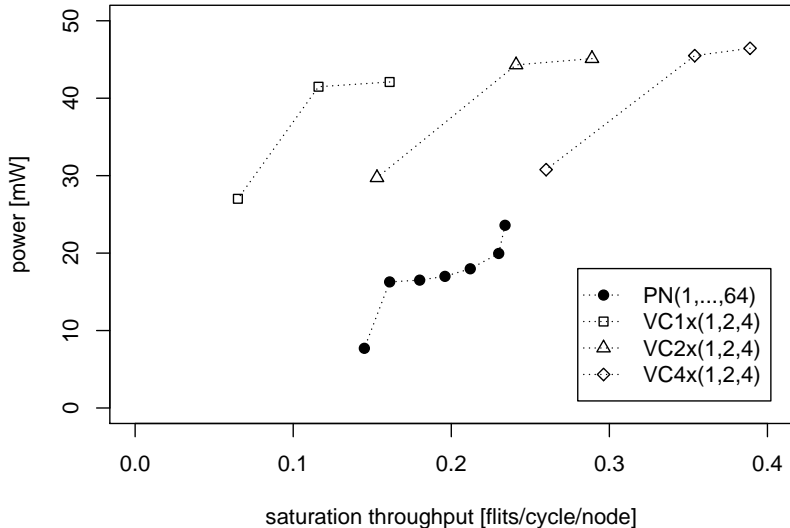




Area



Power vs. Throughput



Conclusion

Summary

- ▶ Semi-bufferless routing in an unidirectional torus
- ▶ Save energy by omitting packets, flow control and virtual channels
- ▶ Low power for low throughput

Future Work

- ▶ Real workloads
- ▶ Power modelling for structural size $< 65\text{nm}$ (DSENT / VHDL)
- ▶ Guaranteed Service (GS) for real-time applications

Thank You

