# Variability-Tolerant NoC Link Design

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# Presentation outline

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# Objectives

The proposed NoC link design methodology takes into considerations the effects of process variability. Delay variations are used to modify the link design parameters, like the optimal number of buffered sections and their gains to achieve 2 goals:

- Meeting the timing delay constraints with variability tolerant NoC links.

- Achieving a margin that is much lower than worst-case analysis by statistical timing analysis, leads to saving of power cost compared to worst-case.

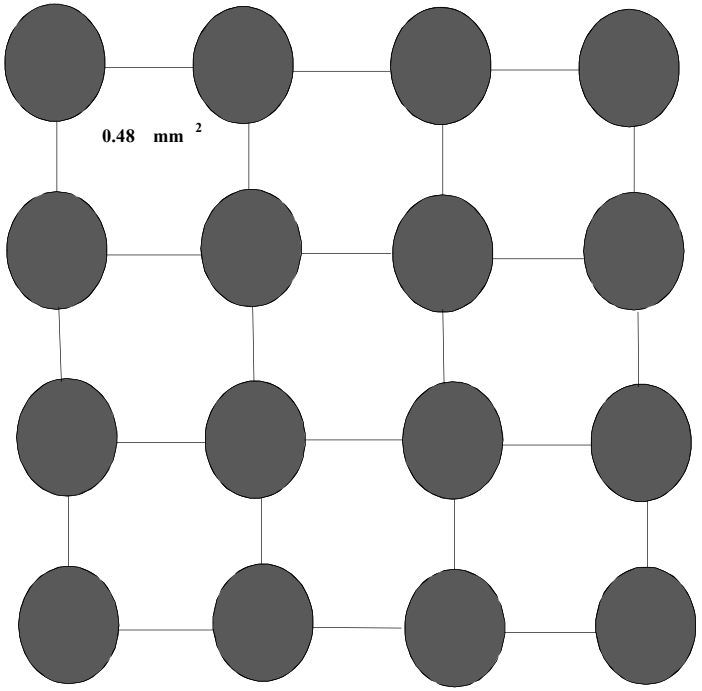
# Contributions

The contributions of this paper could be summarized as follows:

- Implementation of a design model that superimposes delay variations map on a NoC floor-plan to get the delay of each link.
- An integrated delay variations model that calculates systematic and random variability effects.
- Our design model also calculates the optimum number of repeaters and their gains.

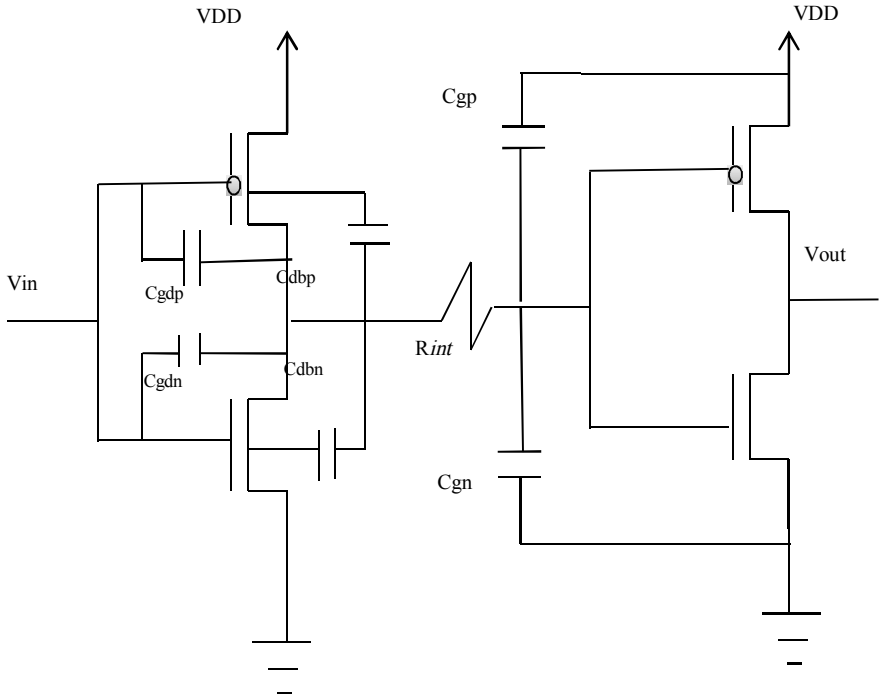
# Networks on Chip

- NoC architectures minimize global wiring delays because of their scalability, and optimized electrical properties.
- There are several used NoC topologies, like torus, mesh, stars, cube, etc.
- The topology selected is a 2D mesh, with a floor-plan shown. circles represent switches, lines represent links.



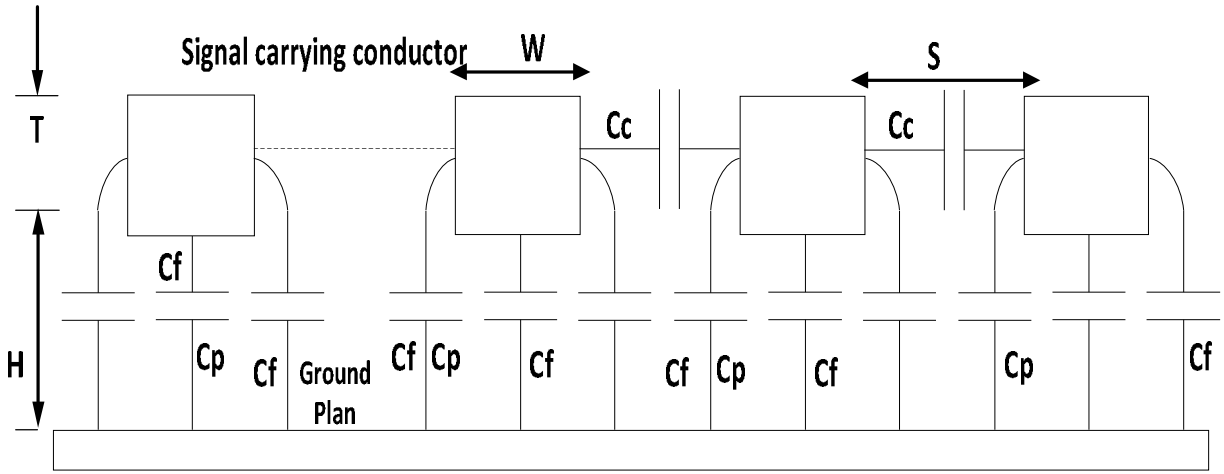
# Link delay model

- Each NoC link consists of sections of repeaters, as shown in the Figure.
- Each interconnect is modeled as a signal carrying conductor plan and a ground plan, separated by a dielectric and having interlayer, coupling and fringing capacitance.




**Circuit representation for An interconnect link composed of two-sections of repeaters.**

# Link delay model cont’




**Layout representation Interconnect line model for NoC links [3].**

$$C_{int} = \varepsilon(1.15\frac{W}{H} + 2.8\frac{T}{H}^{0.222} + 2(0.03\frac{W}{H} + 0.83\frac{T}{H} - 0.07\frac{T}{H}^{0.222})\frac{S}{H}^{-1.34})$$

$$R_{int} = \frac{\rho}{TW}$$

$$Td = 0.4R_{int}\ C_{int}\ L_{int}^{\ 2} + 0.7(R_{tr}\ C_{int}\ L_{int} + R_{tr}\ C_L + R_{int}\ C_L\ L_{int})$$

# Random variations model parameters

- Random variability effects do not have any spatial correlation and are random in nature like Random Dopant Fluctuation (RDF), Oxide Thickness Fluctuation (OTF), or Line Edge Roughness (LER).

- We compute random effects in threshold voltage (Vth), gate length (Lg), oxide thickness (Tox) , and Line width (W) using Hessian function of the numDeriv package of R.

- Variations in the previous parameters cause variations in the link resistive (Rtr , Rint) and capacitive components (Cint , Cox) and consequently cause variations in the link delay.

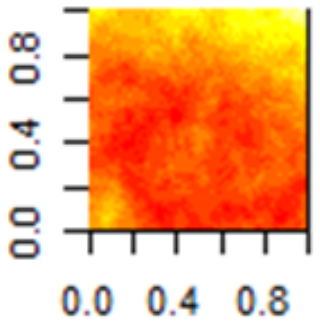
# Systematic variations model

- Systematic effects have spatial correlation and usually arise from lithography, chemical mechanical polishing (CMP), or etching fabrication steps, which cause systematic variations in gate length, threshold voltage or Line Width Roughness (LWR).

- Systematic variability effects have some spatial correlation $\rho(r)$, which means the variability at a point (x,y) is related to variability at neighbor points with a correlation field:

$$\rho(r) = \begin{cases} 1 - \dfrac{3r}{2X_L} + 0.5\left(\dfrac{r}{XL}\right)^3 & \text{if } r \le X_L \\ 0 & \text{if } r > XL \end{cases} \qquad (7)$$

- We generate within-die systematic variations maps calculated on (x,y) plans as shown in the figure.
- The maps represent gate length (Lg), threshold voltage (Vth), line width (W), and line height (H) for different technologies.




**Systematic variation map for a variable with Standard deviation 0.12 and characteristic Xl=1**

# Systematic variations model cont’

- Different variability sources in the front-end and the back-end fabrication processes cause delay variations that may be random or systematic.
- Front-end processes are those involved in the fabrication of devices, whereas back-end processes are those involved in the fabrication of interconnect.
- The generated variations maps for Lg, Vth, W, and H are superimposed on the NoC floor-plan to get the delay of each link in the NoC.
- The systematic delay deviation is estimated and repeated over100 dies to get the averge systematic delay deviations.

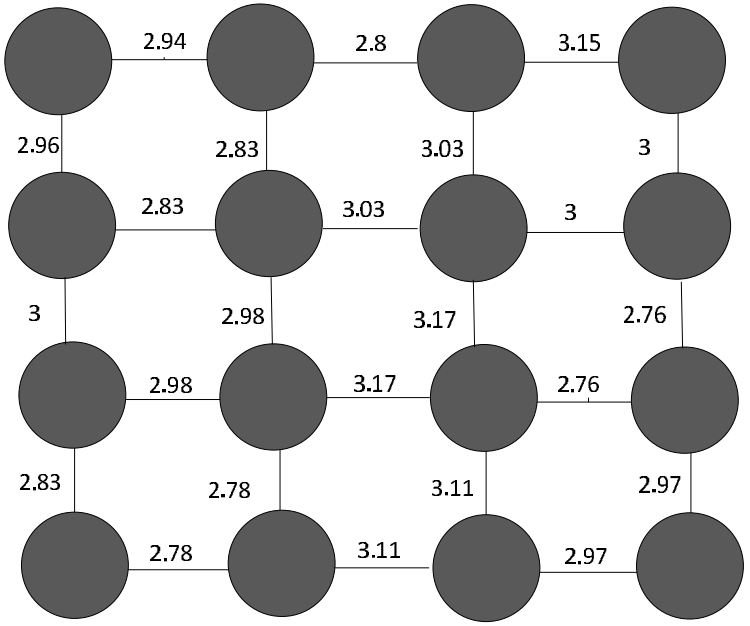



**Figure 4. A 4X4 NoC sample at 45 nm with delay on each link in ns.**

# Variability Model

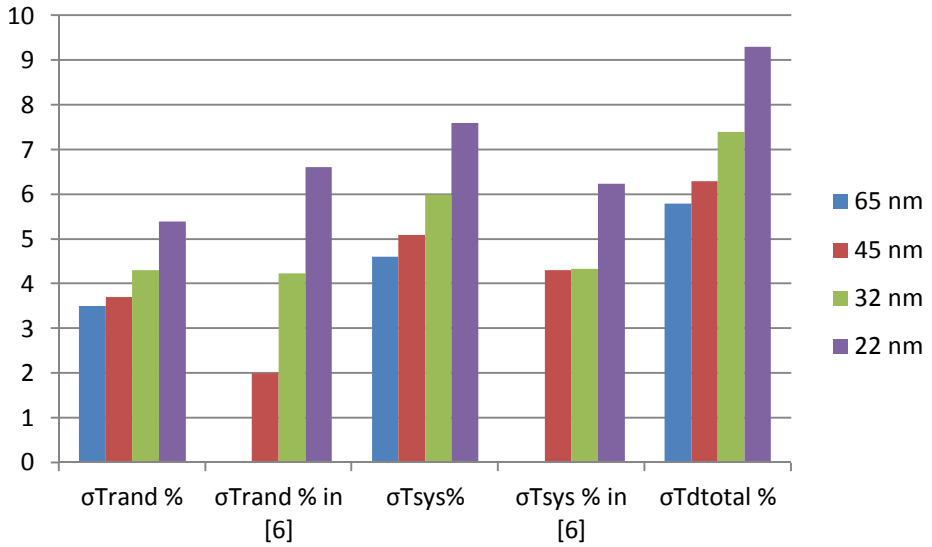
- The total delay variations can be expressed as:

$$\sigma \mathrm{Td}_{\mathrm{total}} = \sqrt{\sigma^2\ \mathrm{Td}_{\mathrm{rand}} + \sigma^2\ \mathrm{Td}_{\mathrm{sys}}}$$

- The results obtained by our variability model, are comparable to the values in [6], obtained by Spice simulation.
- The deviation due to random variations does not scale as the NoC mesh size scales. On the other hand, deviation due to systematic variations scales in accordance to (7), where r increases as the mesh size increases.

**Link delay mean and standard deviation due to random and systematic variation effects.**

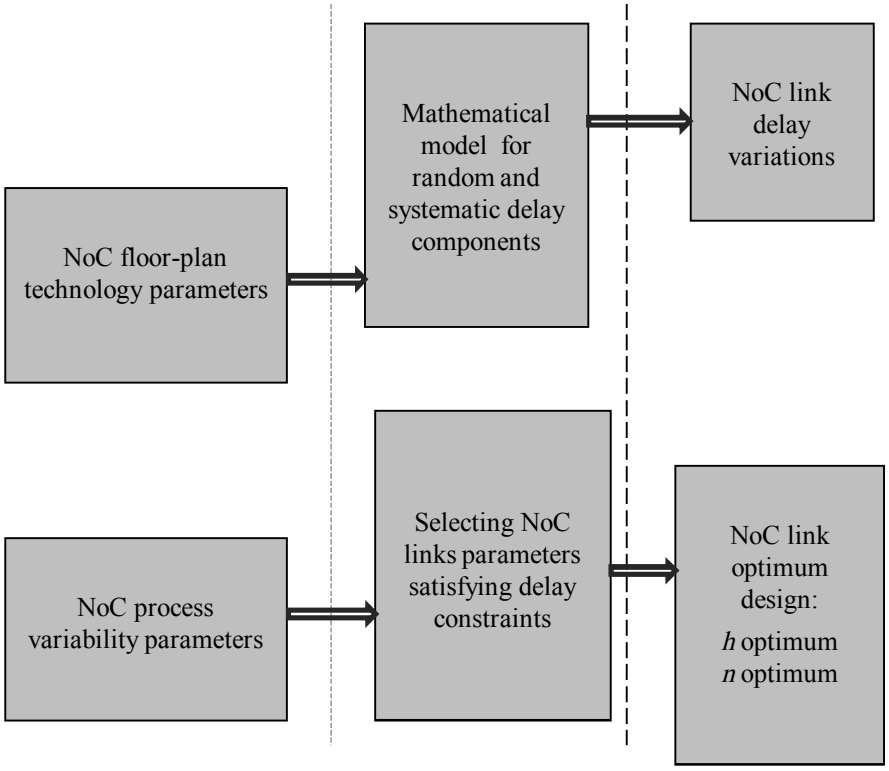
| Technology | σTrand % | σTrand % in [6] | σTsys% | σTsys % in [6] | σTdtotal % |
|---|---|---|---|---|---|
| 65 nm | 3.5 | NA | 4.6 | NA | 5.8 |
| 45 nm | 3.7 | 2 | 5.1 | 4.31 | 6.3 |
| 32 nm | 4.3 | 4.23 | 6 | 4.34 | 7.4 |
| 22 nm | 5.4 | 6.61 | 7.6 | 6.24 | 9.3 |



# Proposed design methodology

Our design methodology has 3 inputs:

- NoC floor-plan file, that contains x and y positions, width, and length information for each link in NoC.
- NoC process variability parameters like mean and standard deviation for different technologies.
- NoC link design constraints, i.e., maximum link delay.
- The output of our design methodology is the delay of NoC links, with systematic and random delay variations.




**Our proposed design methodology for NoC links.**

# Proposed design methodology cont'

- To have a variability-tolerant link design, a statistical link delay is calculated based on systematic and random variations in NoC link parameters.
- The statistical values for NoC link's capacitances $C_{int}$, $C_L$ and resistances $R_{tr}$, $R_{int}$ are used to calculate the statistical link delay $T_d$.
- Another output from our design methodology is the NoC link optimum number of repeaters and their gains.
- It is assumed buffers on the same link are close enough, so that systematic variations between them are really low, and can be ignored.
- NoC link with length $L_{int}$ and n repeaters, each having a gain h will have a delay $T_d$ given by:

$$Td = \frac{0.4\, R_{int}\, C_{int}\, L^2_{int}}{n} + \frac{0.7\, R_{tr}\, C_{int}\, L_{int}}{h} + R_{int}\, L_{int}\, C_L\, h + R_{tr}\, C_L\, n$$

# Case study

- For the case study of Figure 4, optimal h, n, and Dopt for each link of a 4x4 NoC at 45 nm technology are calculated.

- In our case study, 24 links will have (n,h) values set to (1,10) for variability-tolerant links, instead of (n,h) values set to (1,9) for nominal delay values.

- (n,h) can be (1,10), (10,1), (2,5),or (5, 2) as long as their product is 10.

$$P_{cost} = \frac{\sum_{links} n\,h_{statistical} - \sum_{links} n\,h_{nominal}}{\sum_{links} n\,h_{nominal}}$$

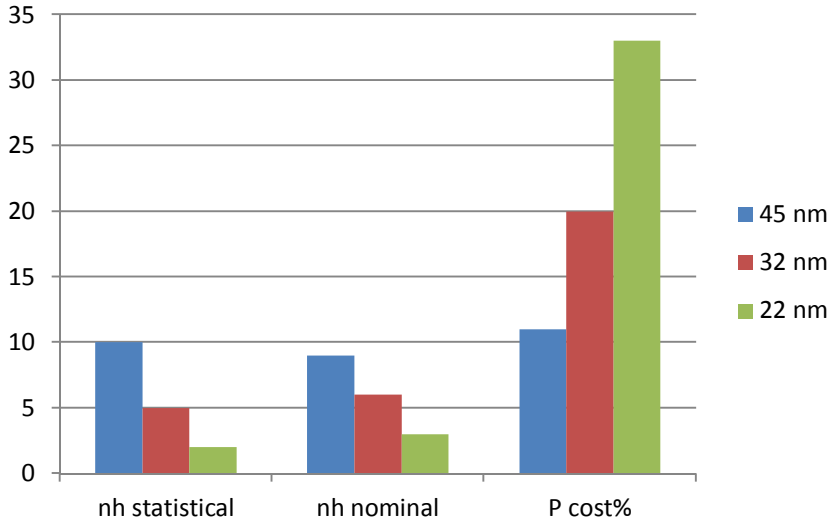
- The total power cost is 11 % of the total power consumption. while, worst-case values for (n,h) will be (2,7) to meet the worst-case delay.

- Thus, our statistical values save 28% of the power consumption compared to worst-case values.

# Results

- The power cost for a 4x4 NoC links at different technologies with a delay constraint of 0.2 ns is shown below:

| Technology | nh statistical | nh nominal | Pcost% |
|---|---|---|---|
| 45 nm | 10 | 9 | 11 |
| 32 nm | 5 | 6 | 20 |
| 22 nm | 2 | 3 | 33 |




- As technology scales down from 65 nm to 22 nm, the link delay variations increases from 6% to 9%.
- Links get faster (link delay is lower), and can meet the design constraints at lower nh nominal values.
- Increased variability, with lower link delay, will make variability more pronounced.

# Conclusion

- As technology scales down, both random and systematic delay variations increase, causing the total delay variations to approach 10% of the total delay.

- Using our proposed variability tolerant design methodology NoC links are tolerant to delay variations with total power cost up to 33%, as compared to nominal delay and power values.

- Proposed methodology achieves power saving up to 28 % of the total power consumption in the test case of 4x4 mesh at 45nm .

- Ignoring NoC links variability may cause circuits to fail to meet the design specifications, while predicting variations and using variability tolerant design enable us to tolerate delay variations at a defined power cost.

# *Thank You*

## *Questions?*