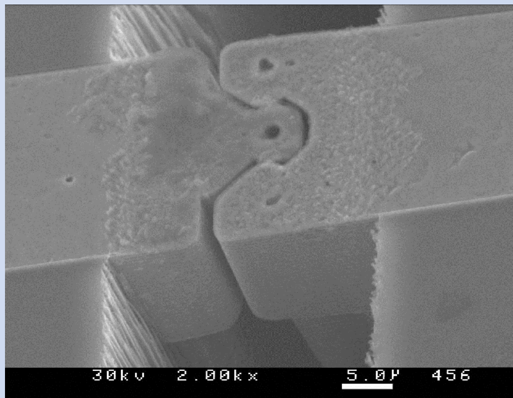
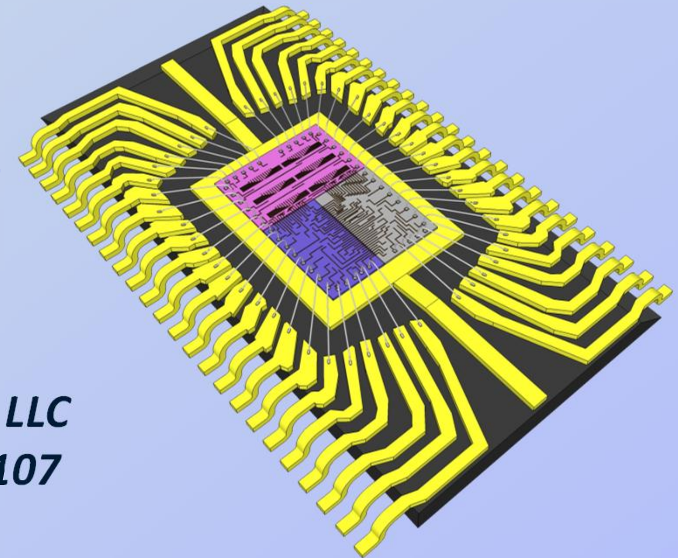
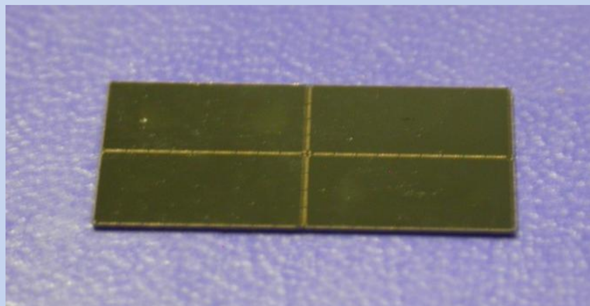
Network on Metachip Architectures

Ismo Hänninen*, Wayne Buckhanan, Michael Niemier, Gary Bernstein
Center for Nano Science and Technology
University of Notre Dame
Notre Dame, IN 46556
+1-574-631-0996
ismo.hanninen@nd.edu
** And Tampere University of Technology, Finland*





Jason Kulick
Indiana Integrated Circuits, LLC
1400 E. Angela Blvd., Unit 107
South Bend, IN 46617
+1-574-217-4612
jason.kulick@indianaic.com



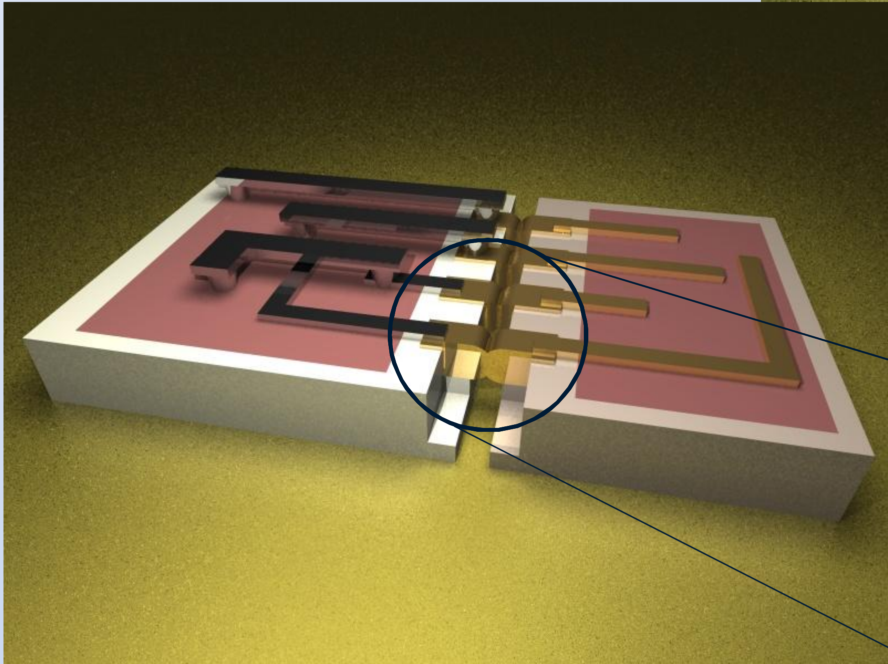
Outline

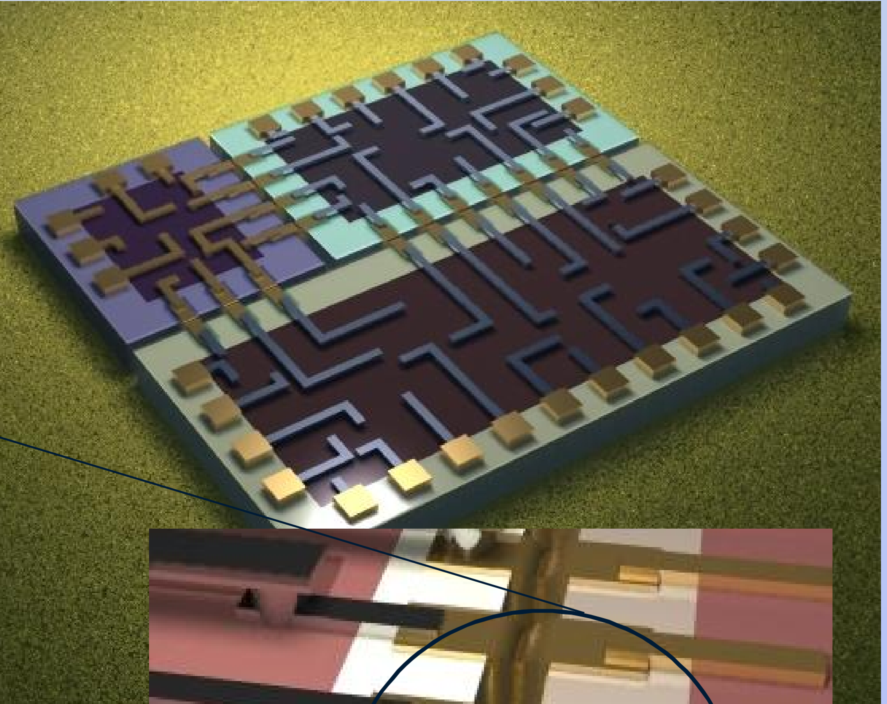
- Introduction: Metachips & Quilt Packaging®
- Signal Performance
- Interconnections and Quilt Size
- Memory Access on a Quilt
- Quilted Multiprocessor SoC
- Conclusion

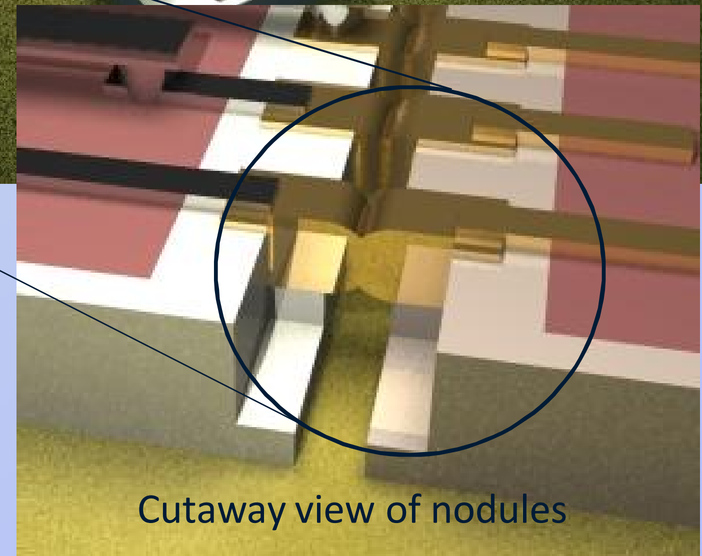
Introduction:

METACHIPS & QUILT PACKAGING®

Quilt Packaging Process - General

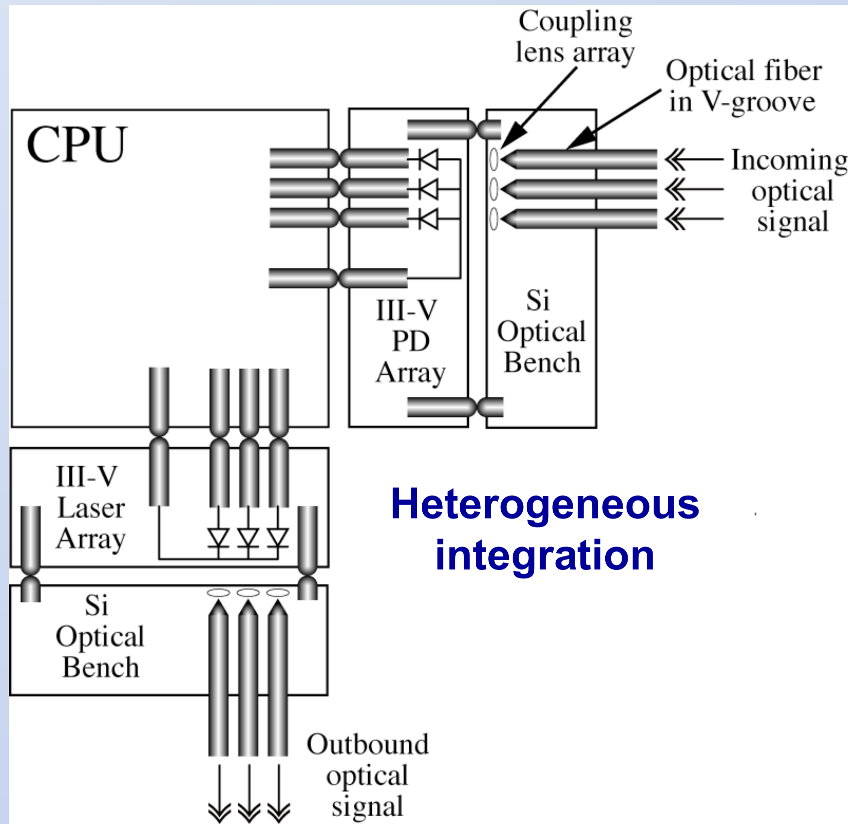






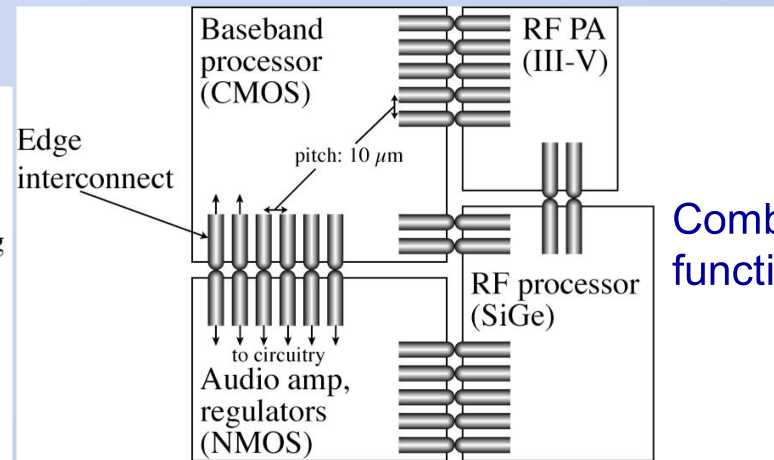
Bare die interconnect directly through edges

Some Applications of Quilt Packaging



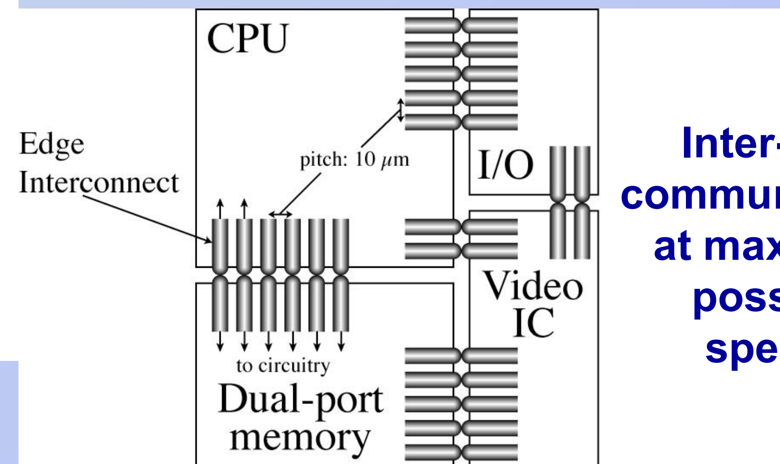
Heterogeneous integration

Optical networking



Combined functionalities

Wireless communication

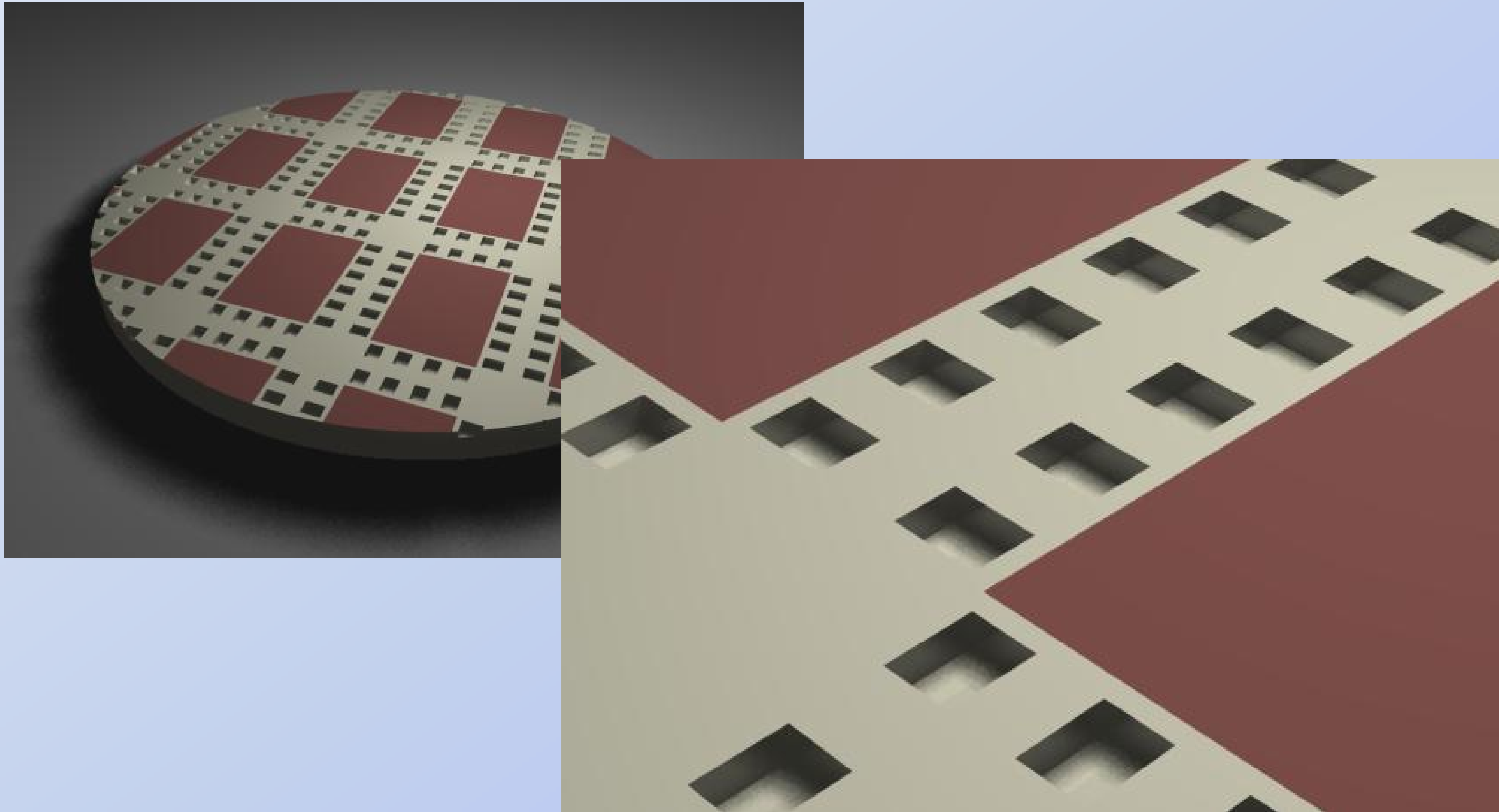


Inter-chip communication at maximum possible speeds

High speed digital processing

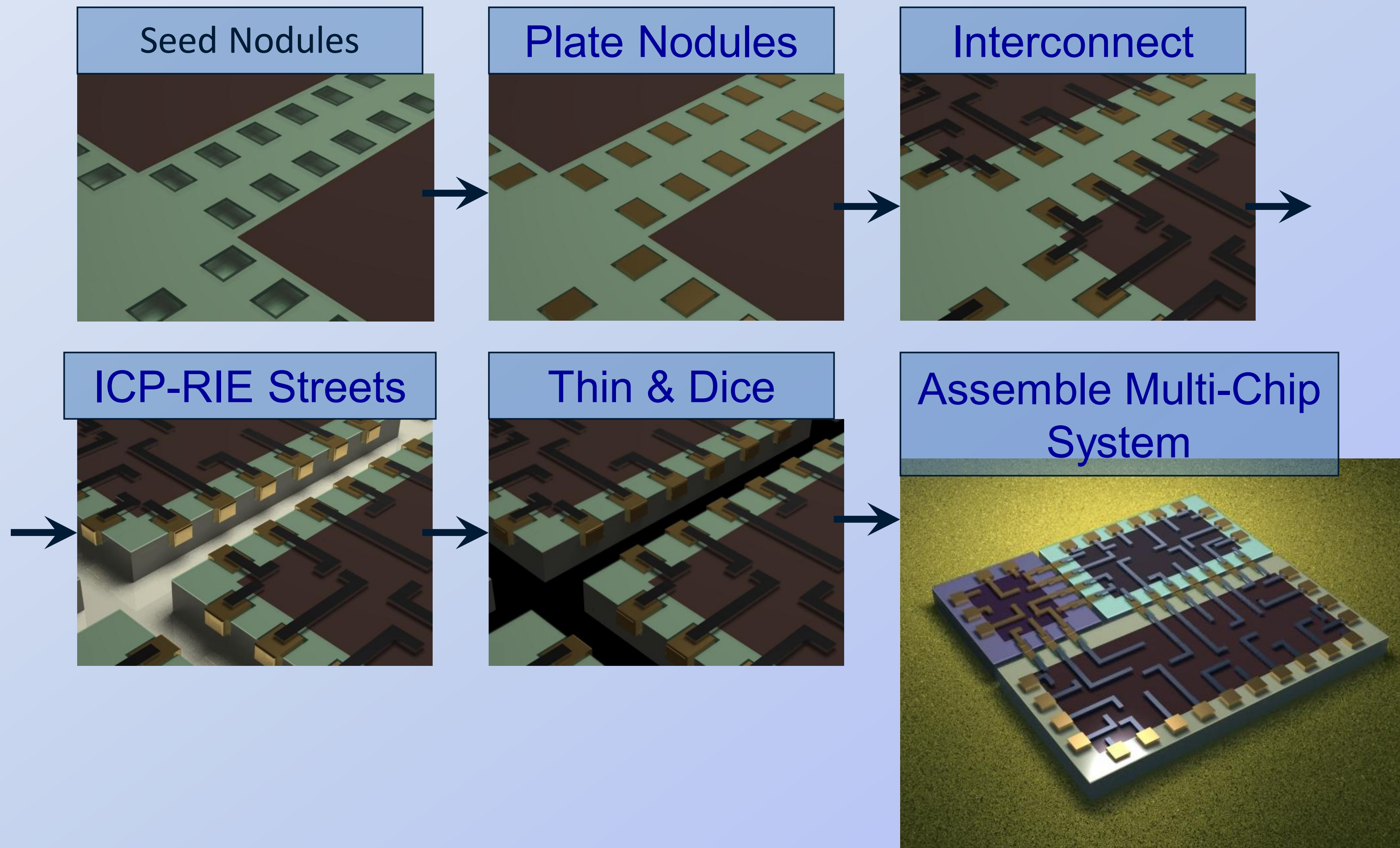
Quilt Packaging Fabrication

Etch Nodule Templates after IC front end fabrication

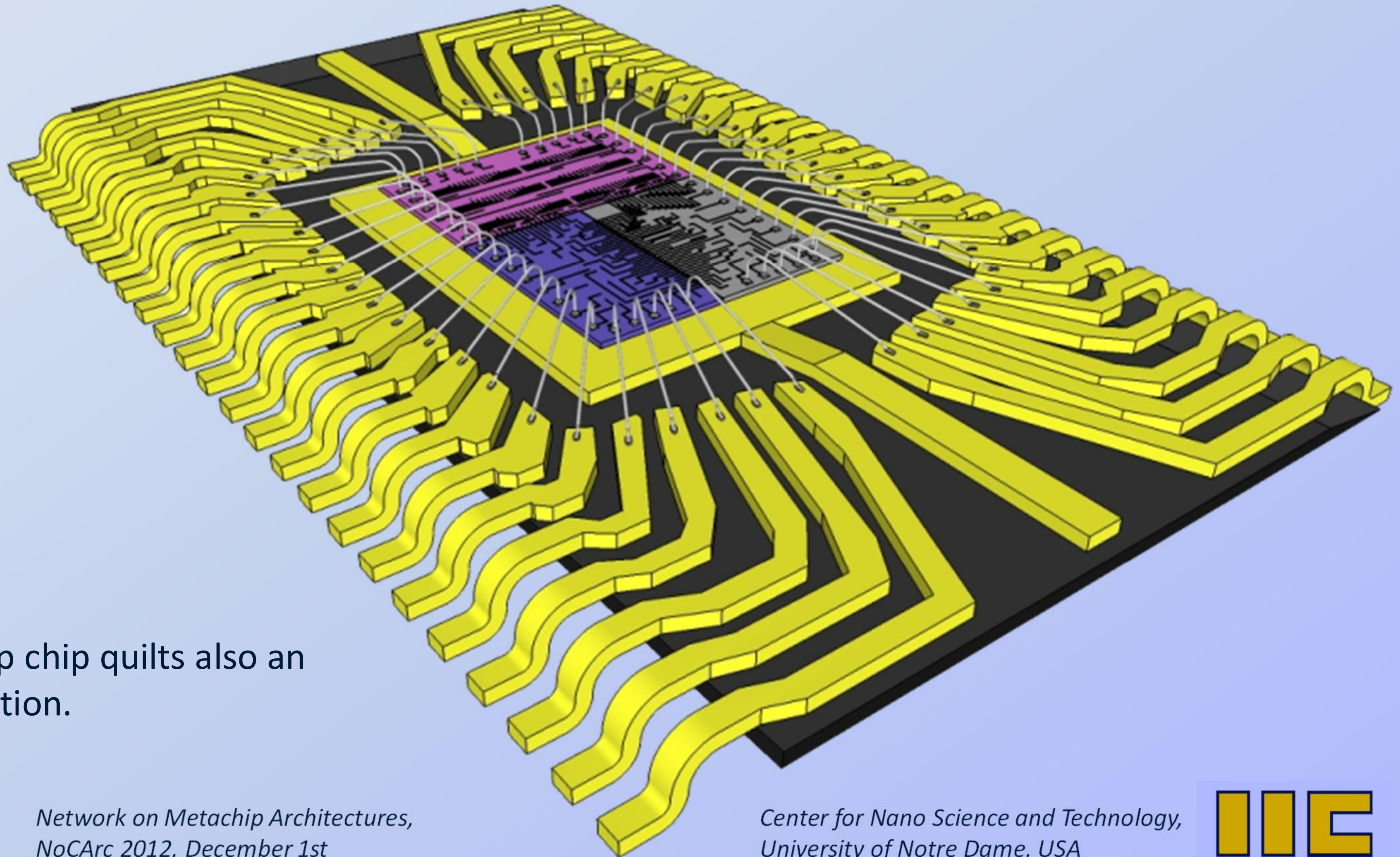


Indiana Integrated Circuits LLC

Quilt Packaging Fabrication



Quilted Chips are Packaged as if Monolithic



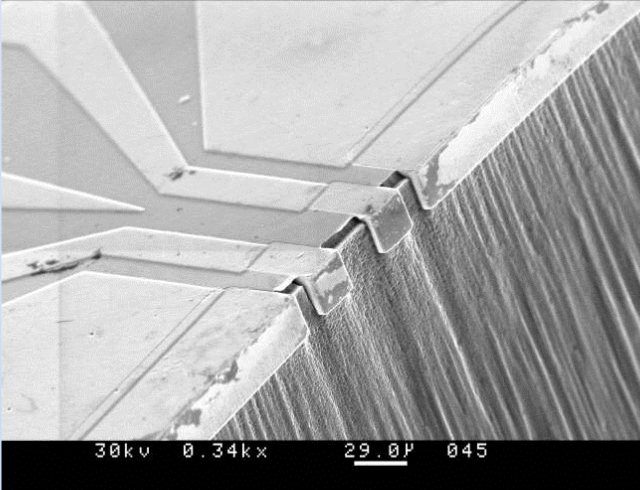
Flip chip quilts also an option.

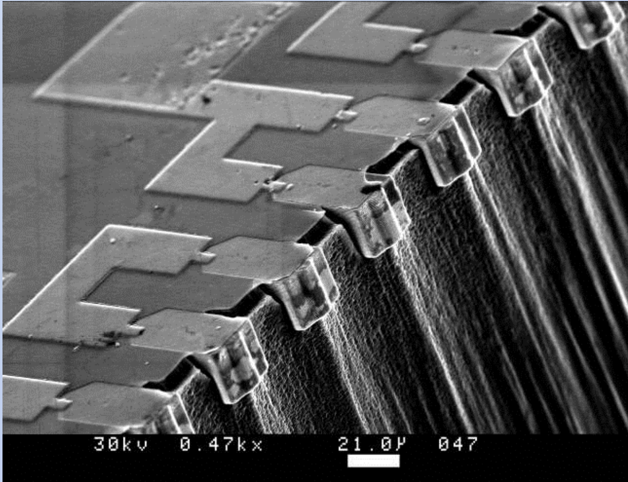
Advantages of Quilt Packaging

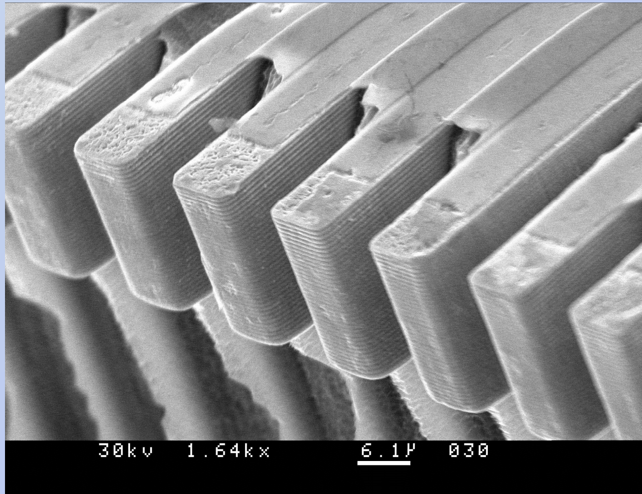
- **Heterogeneous integration** of ICs and components fabricated using different processes (e.g. nanotechnology and CMOS)
- **Better thermal control** due to all chips on heat sink
- **Simpler fabrication** than chip stacking
- **High signal bandwidth** with excellent signal integrity
- **Reduced power dissipation and die size** (up to 50%) through reduction of pin I/O drivers and package capacitances
- **Cost reduction** by eliminating some packages and reducing package and board complexities
- **Flexible use of IP and cores**– mix and match – not large development cost for new "quilt"
- **Decreased electrical noise**
- **Decreased need for passives**
- **Thinner profiles compared to chip stacking or PoP**
- **Variety of interconnect widths available simultaneously**

Can be used in combination with existing packaging strategies

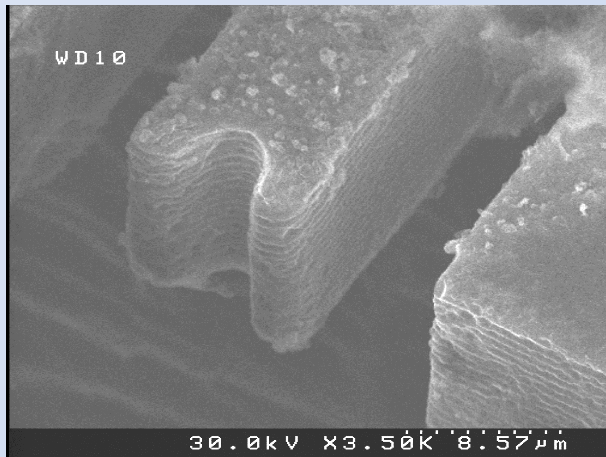
Various Nodule Geometries to 10 μm





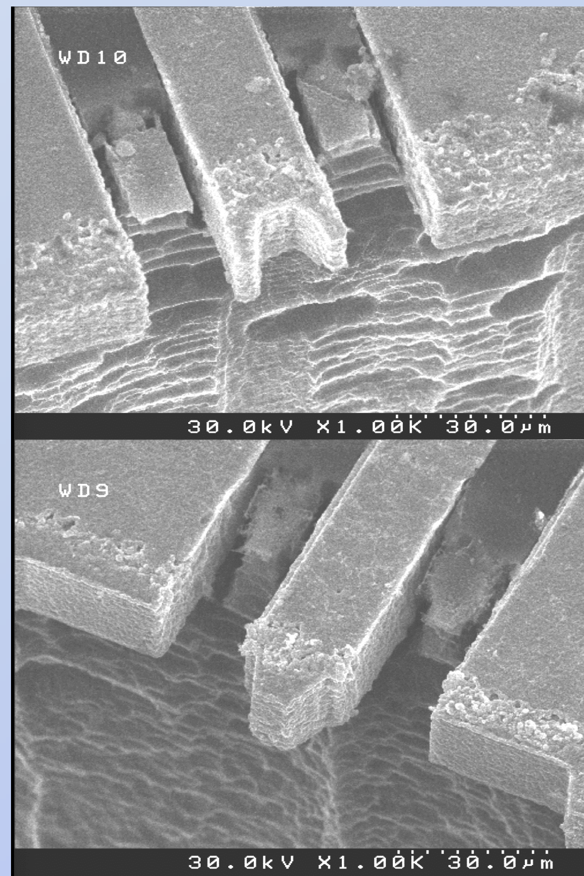


10- and 20-μm-wide Keyed Nodules



10-μm wide, 20-μm thick

10-mm chip would support 500 10-μm wide nodules on one side.

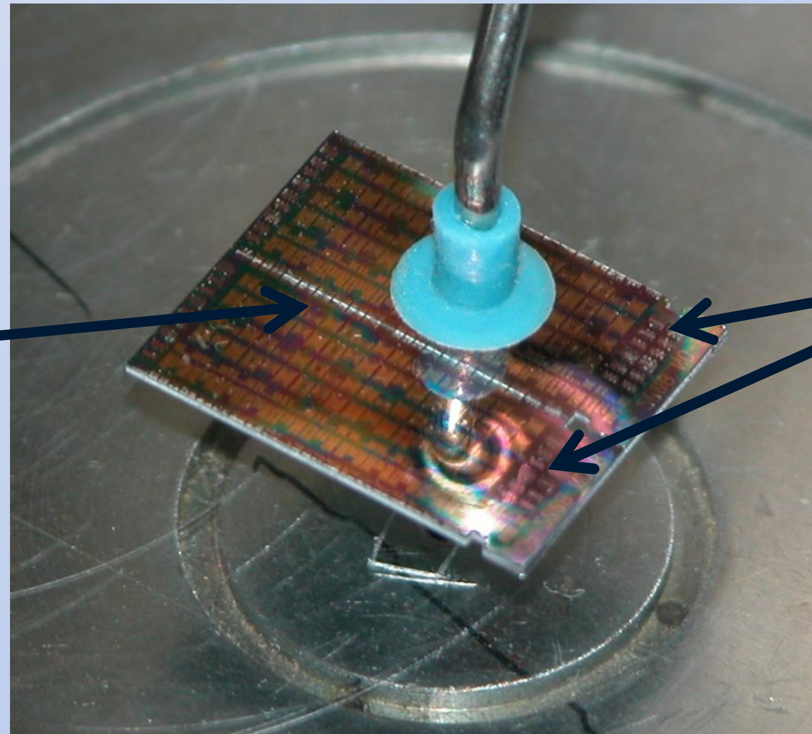


20-μm wide

- Interlocking nodules 10 μm to 400 μm fabricated
- Keys aid alignment
- Degree of protrusion, key shape, well controlled

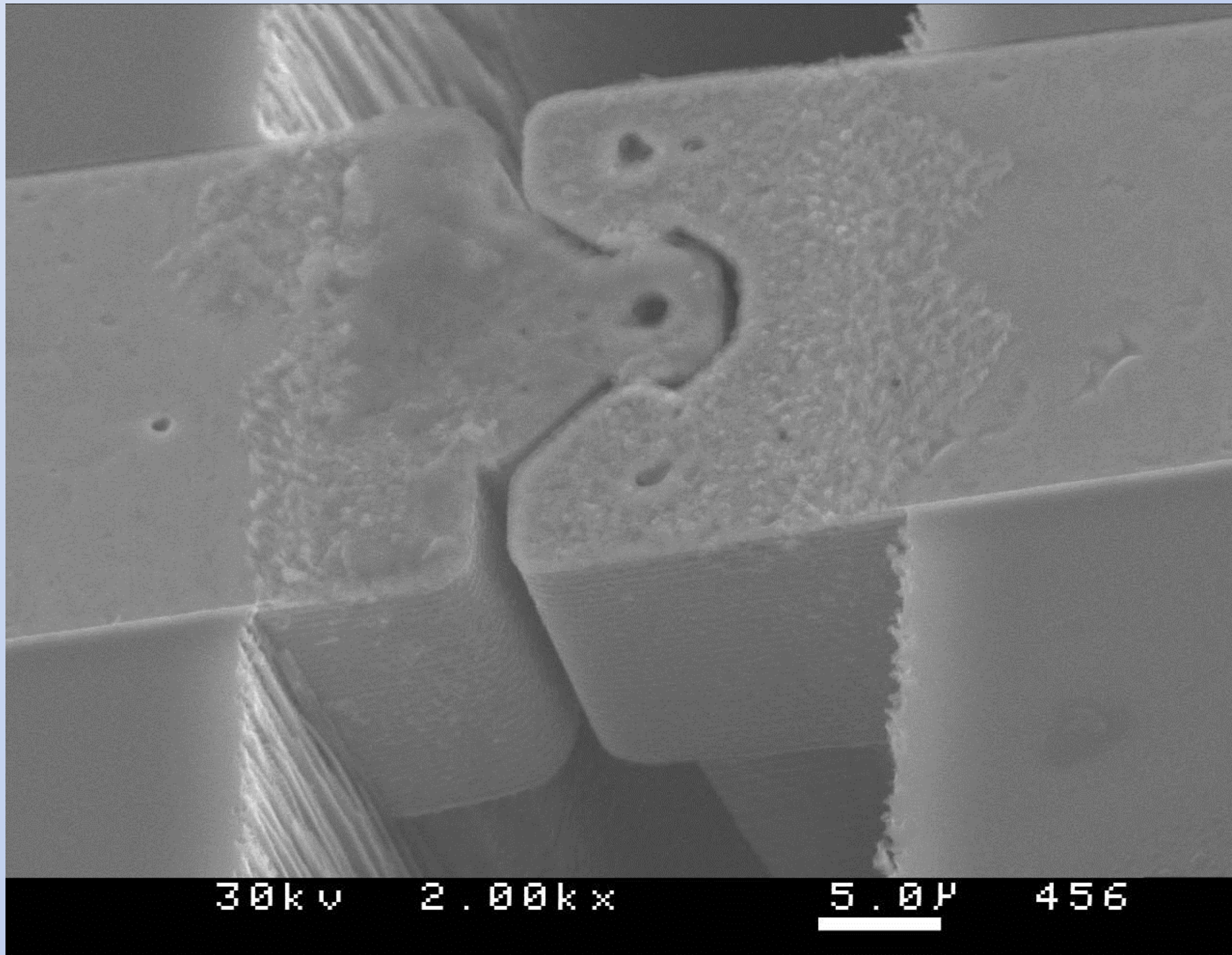
Nodules are Physically Strong – Chip Supported by Edge Only

Connected along edge

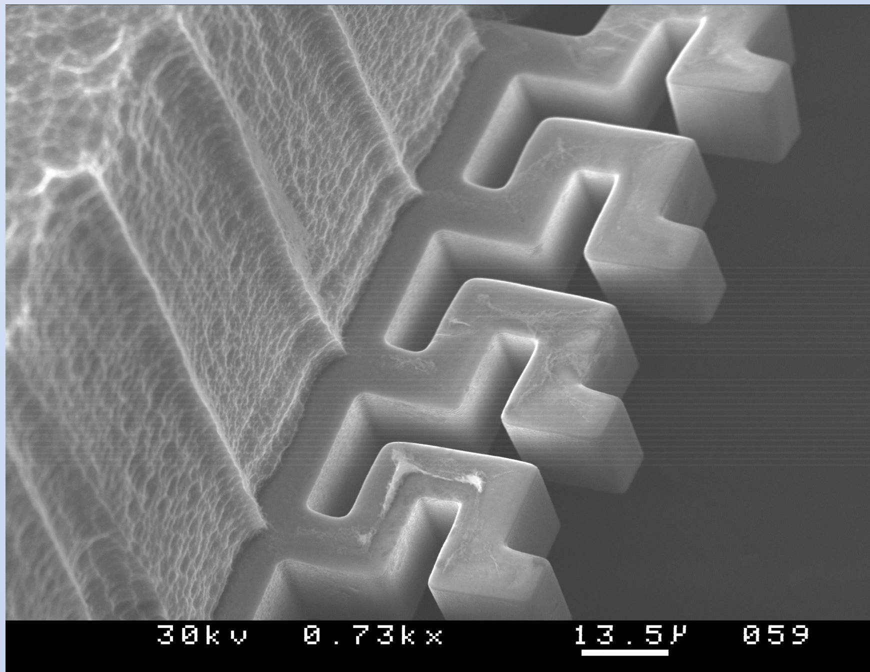


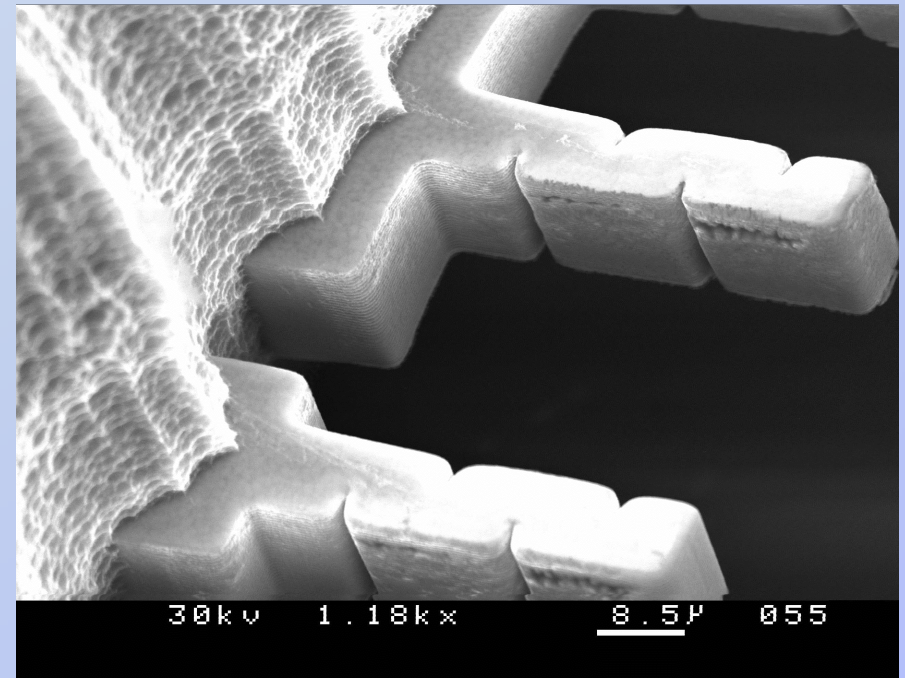
Two QP'd chips lifted off of surface

Interlocking Nodules

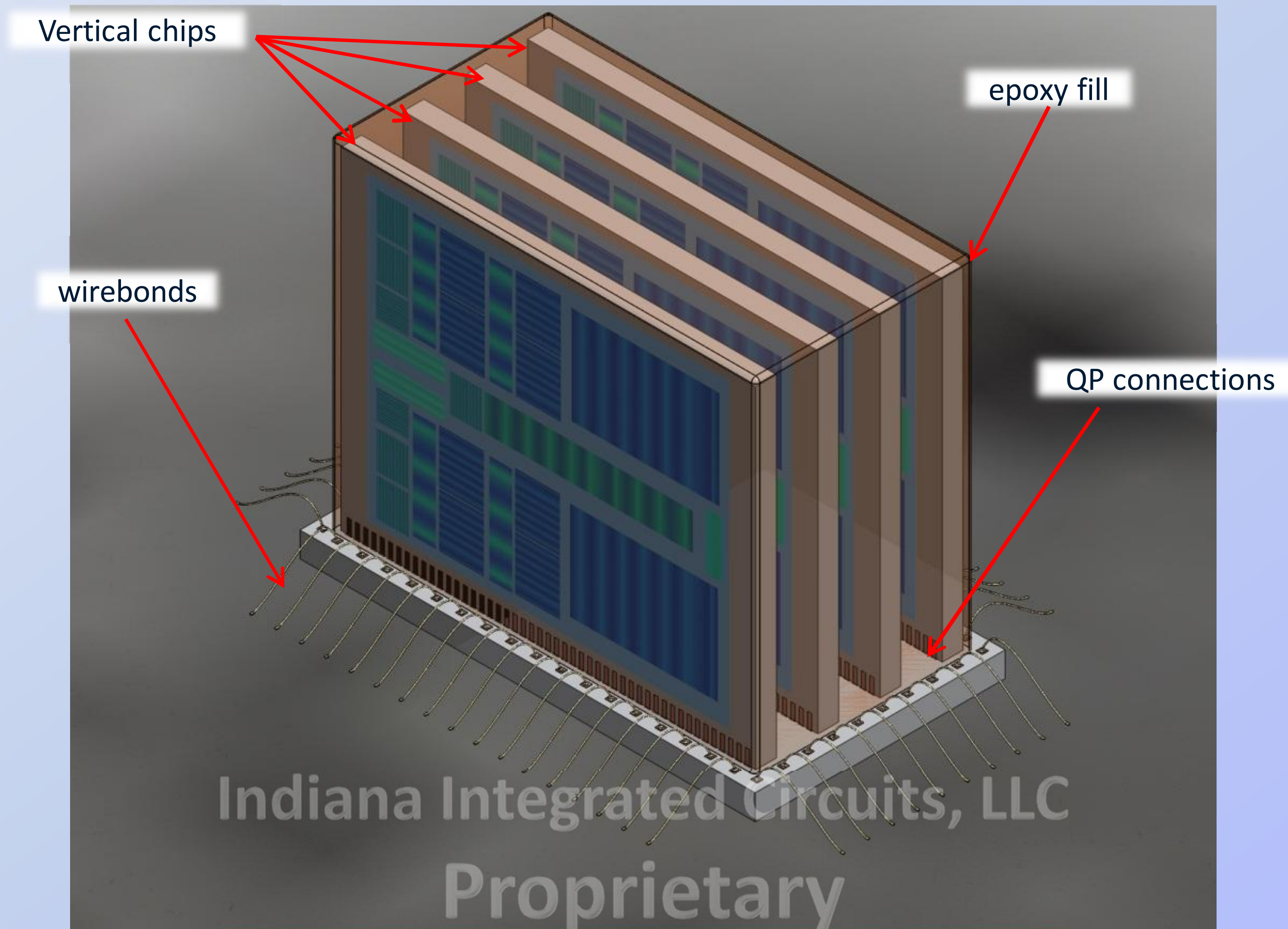


Compliant Nodules





3D QP Concept

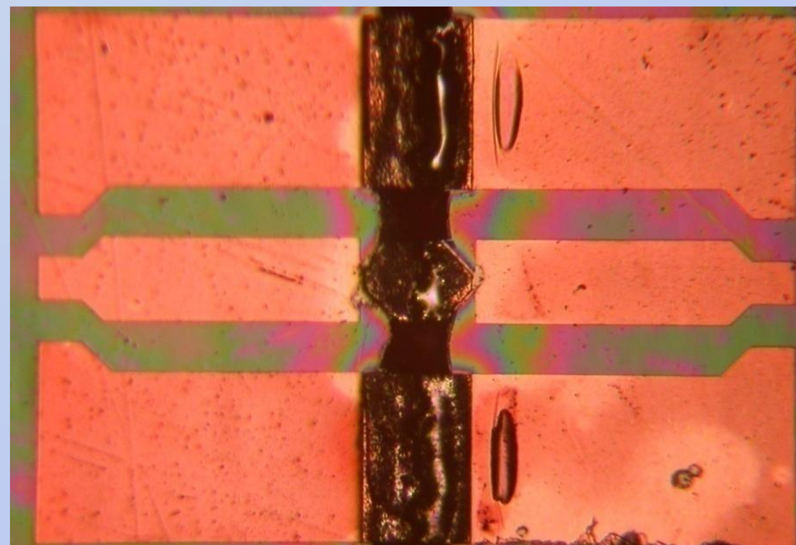


Measurements:

SIGNAL PERFORMANCE

Quilt Interconnect RF Performance

- Typical interconnect:
  - 100 µm nodule
  - Tapered signal line, straight CPW ground lines
  - 100 µm pitch GSG probe pads
- 8 kΩ-cm substrate resistivity
- 400 µm substrate thickness
- Cu interconnect, 1 µm Sn solder plating

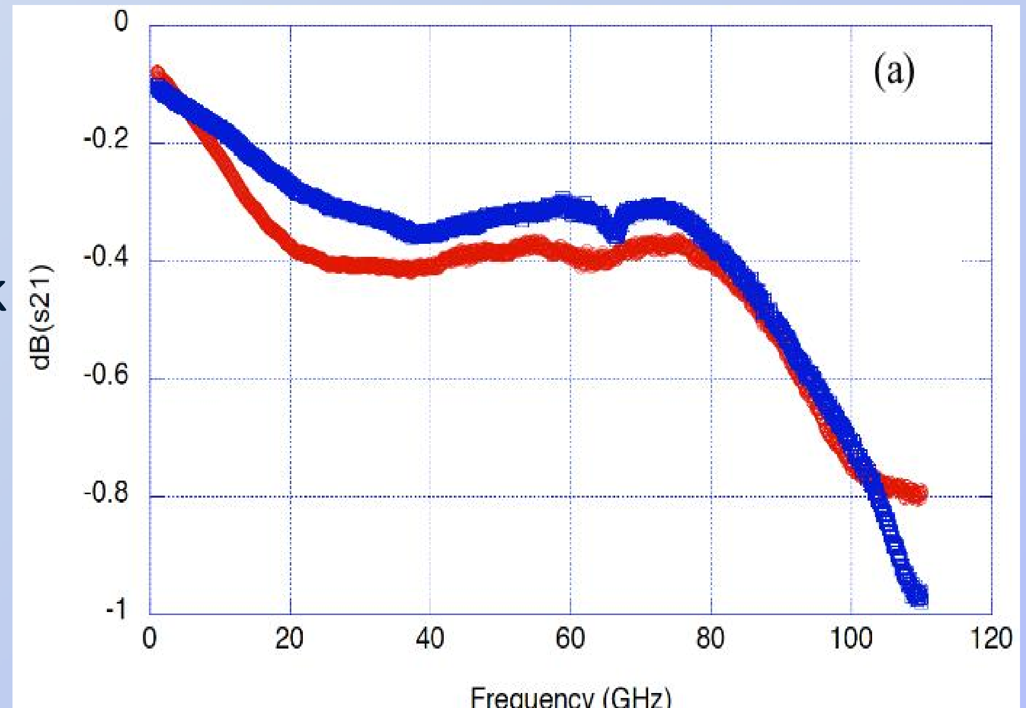


Center for Nano Science and Technology, University of Notre Dame, USA

Indiana Integrated Circuits LLC

RF Performance: Insertion loss

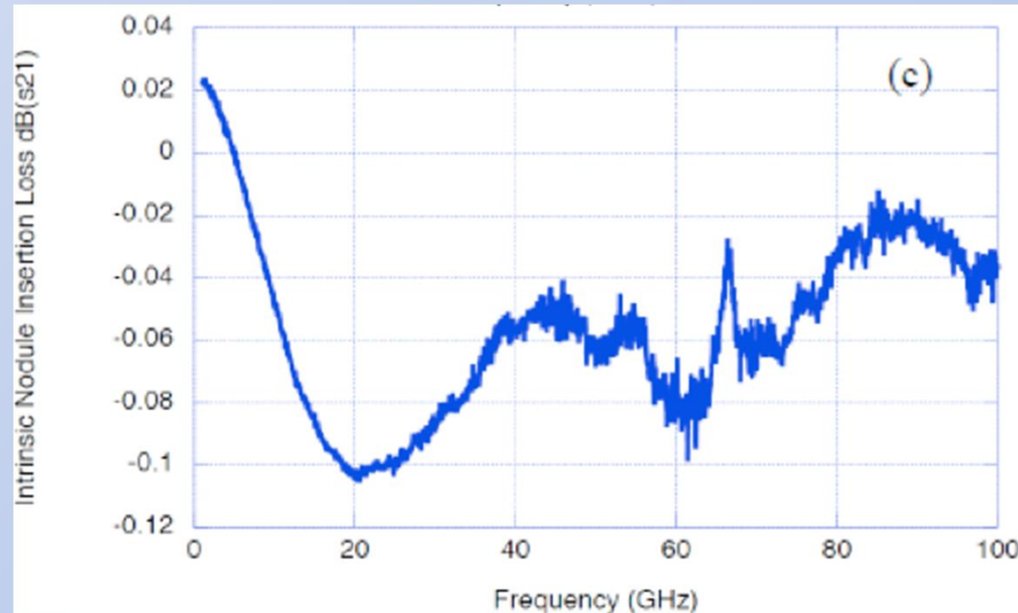
- S-parameters measured on-wafer,
  10 MHz – 110 GHz
- Nodule and test pad insertion loss curves track
- Loss attributable to nodules < 0.1dB to 110 GHz
- Loss including pads and launcher:
  - < 0.4 dB below 80 GHz
  - <1 dB to 110 GHz



Red: Nodules and test pads
Blue: Test pads alone

Intrinsic QP RF Performance

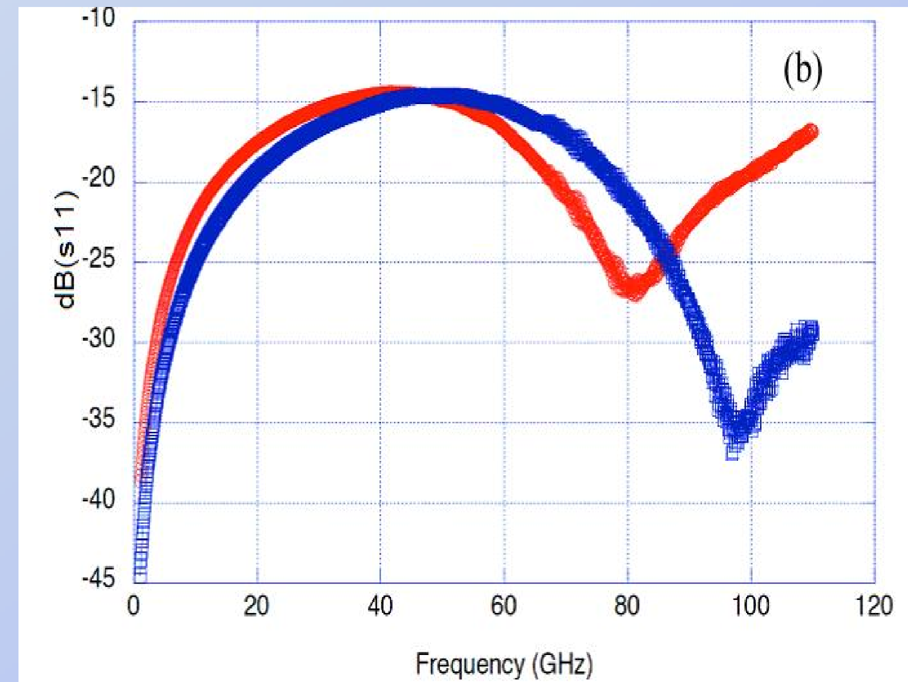
- De-embedding effects of pads, launcher:
  - Intrinsic QP nodule loss < 0.1 dB to 100 GHz
  - Nearly flat loss vs. frequency characteristic



- Promising for extremely wide bandwidth systems

RF Performance: Return loss

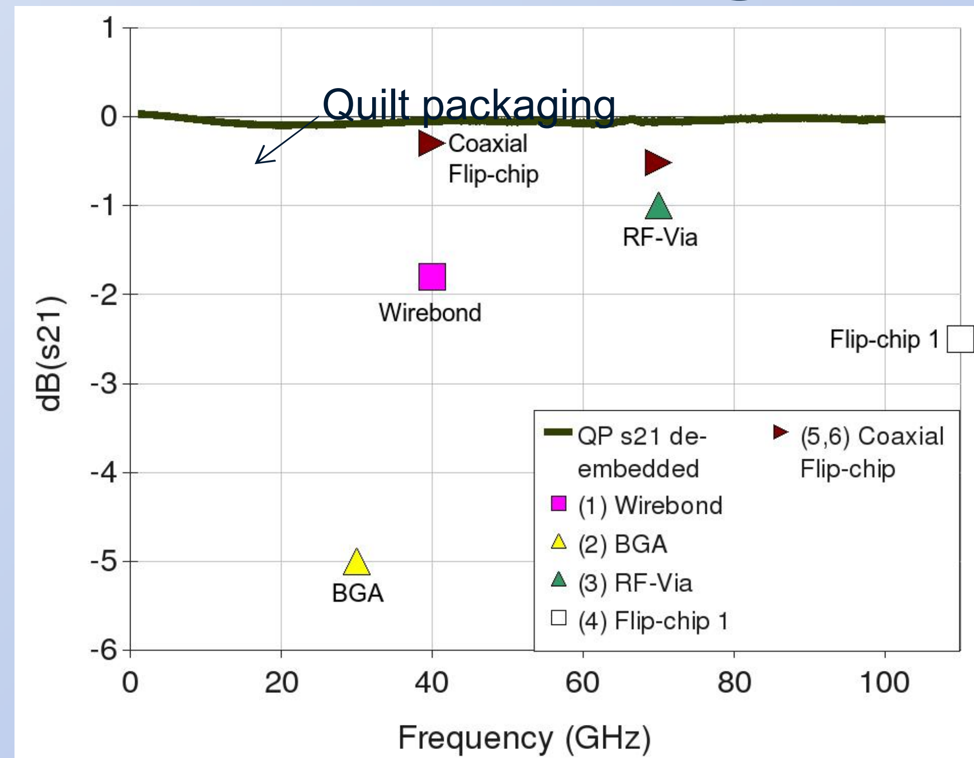
- Return loss shows a quarter-wavelength resonance
  - Unintended mismatch in the lines
  - Z_0 is 59.8 Ω, nominal 50 Ω.
- Characteristic of high quality transmission lines
- QP resonance at lower frequency
  - Consistent with increased transmission line length due to nodules



Red: Nodules and test pads
Blue: Test pads alone

Comparison to Other Technologies

- De-embedded insertion loss compared with recent papers on wirebonds, ball grid array, MS-to-CPW RF-via, flip chip.
- 0.25 dB lower than coaxial flip-chip via at 40GHz
- 1.7 dB lower than standard flip-chip at 110 GHz
- 0.8 dB lower than RF-via at 70 GHz



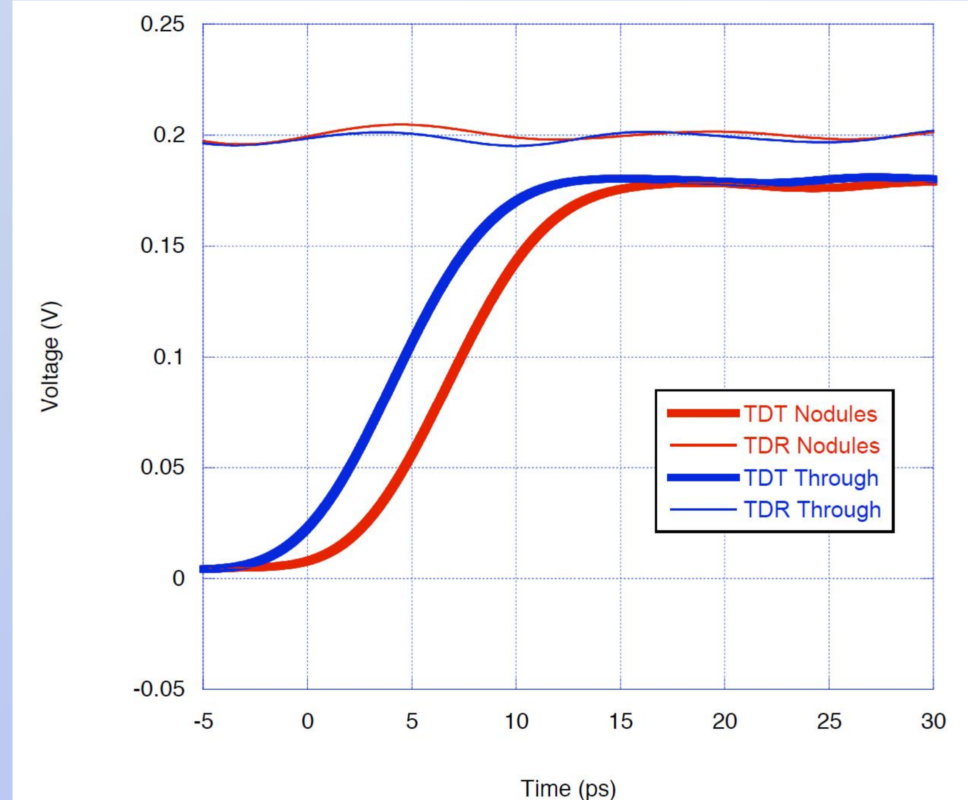
- 1. Sutano et al. IEEE Trans. Adv. Packaging, Vol 24, No. 4, Pg. 595. Nov. 2001.
- 2. Heyan, et. al. IEEE Trans. Microwave Theory and Tech., Vol. 51, No. 12, Pg. 2589. Dec 2003.
- 3. Hsu, et. al. CS-Mantech Conference, "Fabrication Process and 110GHz measurement result of MS-to-CPW RF-Via Transition for RF-MEMS Devices Packaging Applications" May 18-21 2009.
- 4. Cho, et. al. Microwave and Optical Technology Letters, Vol 51, No. 5, Pg. 1821. May 2009.
- 5. W. Wu, et al. IEEE Trans. Adv. Packaging, Vol 32, No. 2, Pg. 362, May 2009
- 6. W. Wu et al. IEEE Microwave and Component Letters, Vol. 17, No. 11, Nov. 2007

QP demonstrates a world record for low-loss chip-to-chip interconnect!

Time-Domain Performance

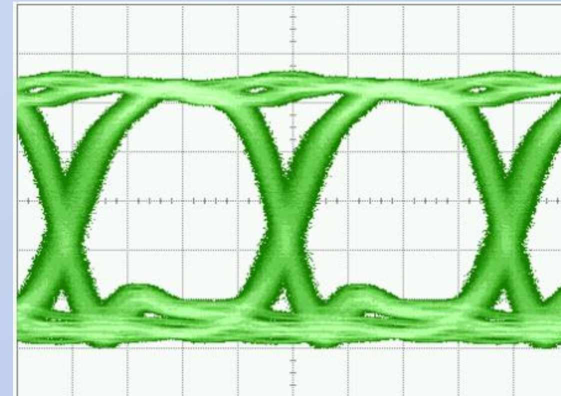
- Single-ended GSG CPW configuration
- Picosecond Pulse Labs 4022 TDR pulse enhancement module: < 9 ps risetime
- Total delay including probe pads, launcher: 7 ps (820 µm length)
- Delay due to QP nodules: 2.7 ps

100 µm nodule compared with pads/launcher, GSG

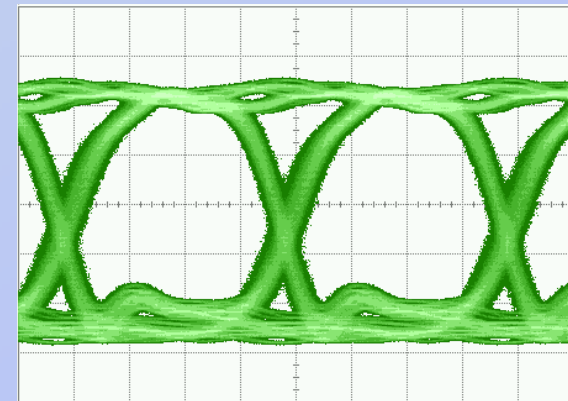


Eye diagrams

- Measurement of 12 Gb/s eye pattern (Anritsu MP1763B)
  - Horiz. 100 mV/div
  - Vert. 20 ps/div
- Data stream: 2^{31}-1 pseudo-random bit sequence
- Nearly ideal interconnect performance; indistinguishable from PG.
- Error-free operation
  - SNR (Q) = 12.9 for pattern generator alone, 12.4 after chip-to-chip interconnect



Raw pattern generator



50 µm GSG eye

What to expect of quilted metachips:

INTERCONNECTIONS AND QUILT SIZE

Chip Interconnects

- 50—200 homogeneous interconnection nodules per chip edge millimeter

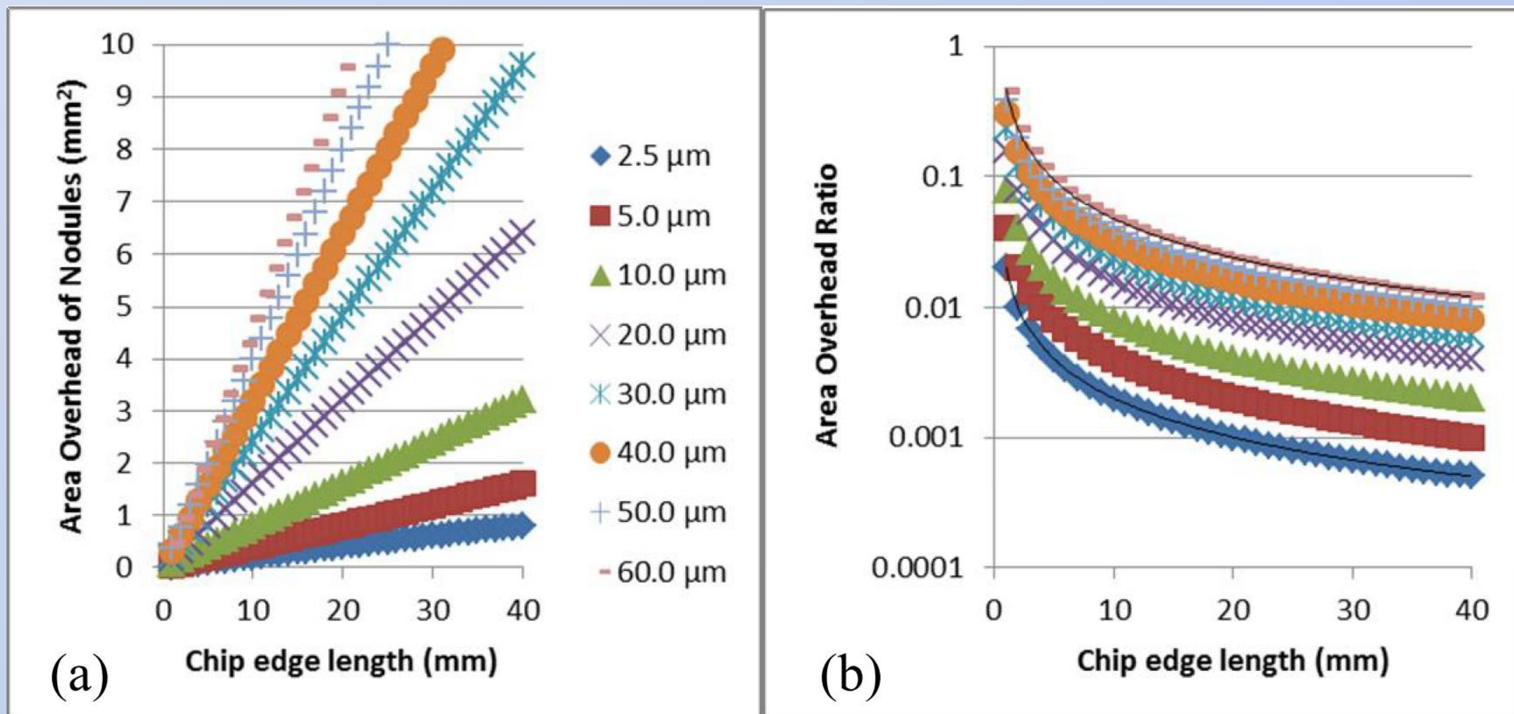
  $\Rightarrow$ thousands of wires per chip edge

Chip edge (mm)	Nodule/gap width (µm)		
	2.5	5	10
1.0	200	100	50
2.0	400	200	100
5.0	1000	500	250
10.0	2000	1000	500
20.0	4000	2000	1000
40.0	8000	4000	2000

- Various heterogeneous configurations possible

Silicon Area and Yield…

- Interconnection nodules consume very little silicon area, **typically << 1 %**

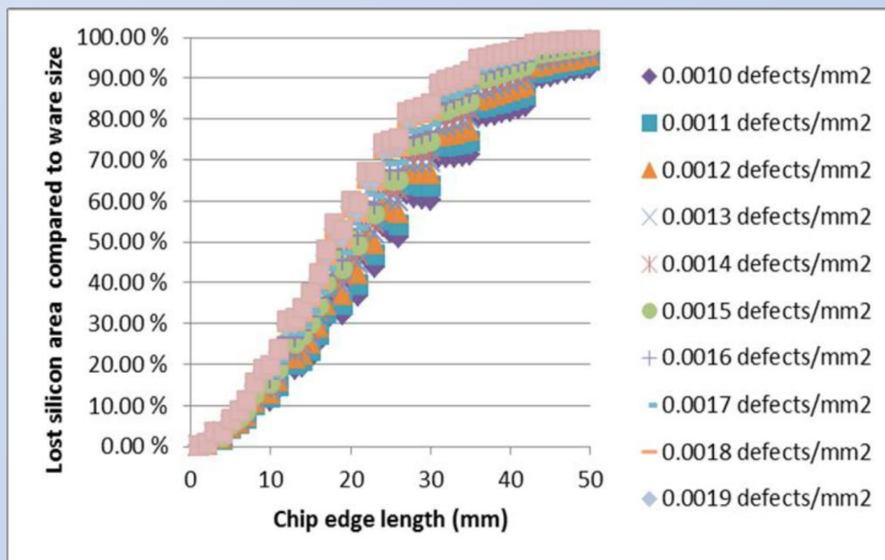


Indiana Integrated Circuits LLC

…Silicon Area and Yield

- Chip size affects IC fabrication yield, especially on deep-submicron technologies

  ⇒ **QP** offers **silicon savings** with high yield



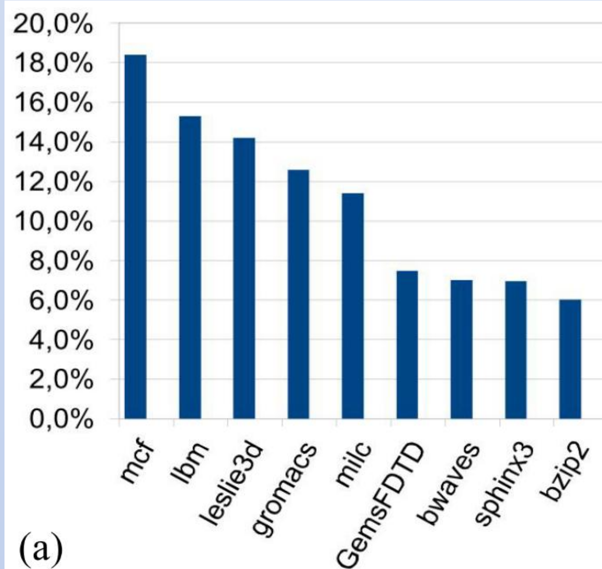
# chips, size (mm x mm)	Loss of silicon area due to…		
	yield, 0.0001 defects / mm^2	yield, 0.0010 defects / mm^2	nodules / dicing
1, 40 x 40	24.16 %	82.03 %	**0.00 %**
4, 20 x 20	6.26 %	40.34 %	**0.40 %**
16, 10 x 10	2.85 %	11.22 %	**0.80 %**
64, 5 x 5	2.12 %	4.30 %	**1.60 %**

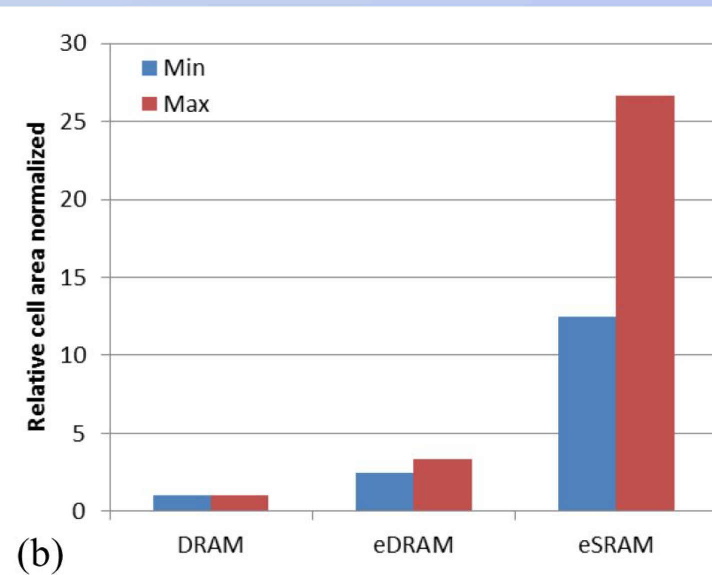
Removing the bottlenecks:

MEMORY ACCESS ON A QUILT

Quilted SoC Memory

- Quilted architecture alleviates memory system bottlenecks
  - Reduced physical distance vs. external memory chip
  - Improved memory density vs. single chip SoC
  - Wide bus access!



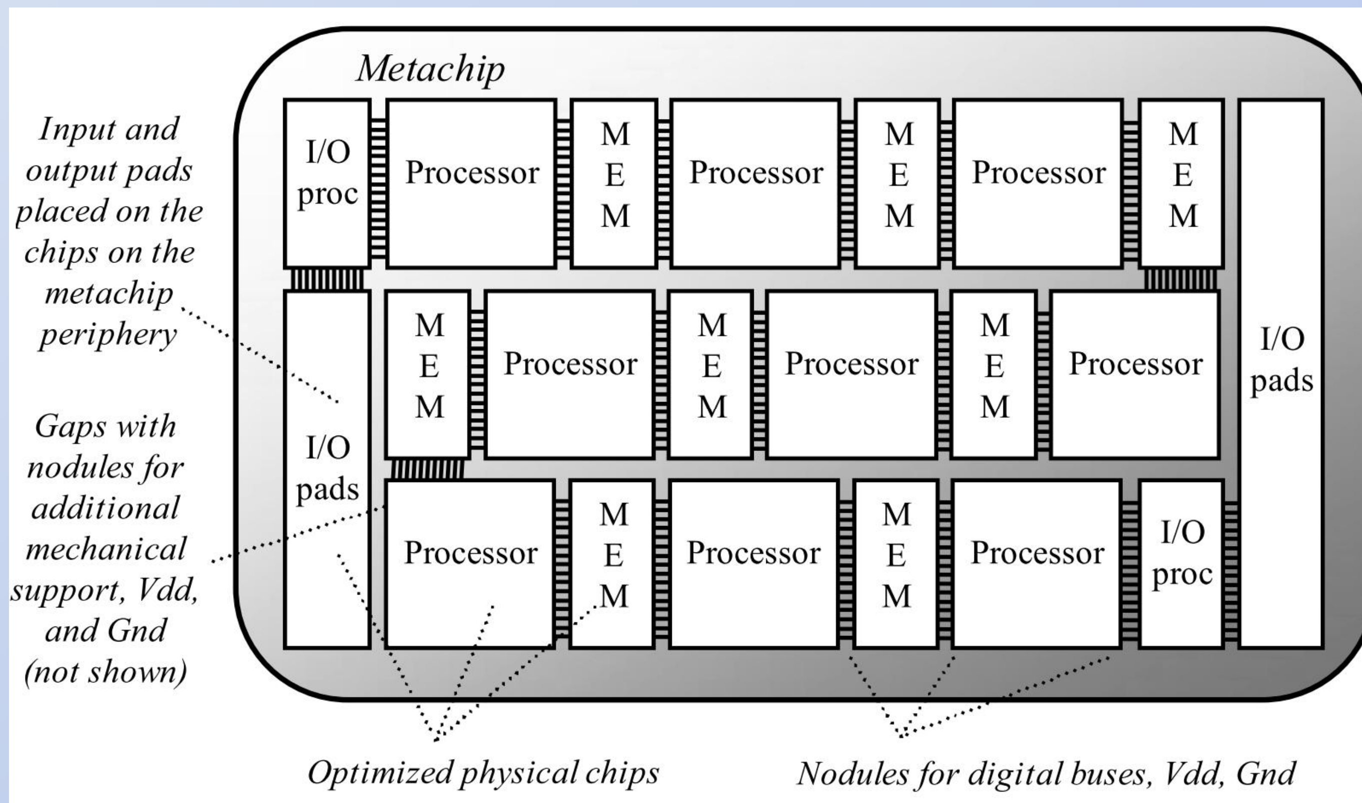


The dream:

QUILTED MULTIPROCESSOR SOC

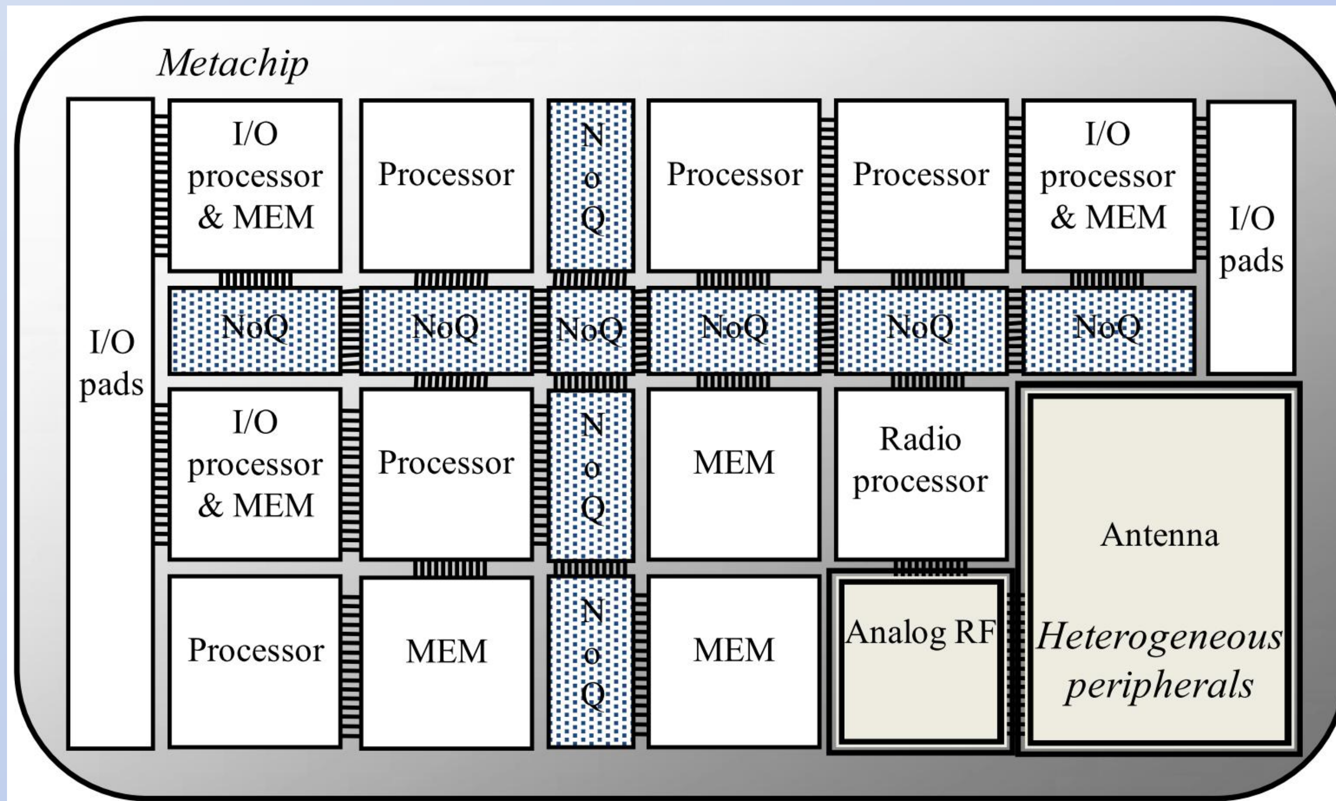
MPSoC with Local Memories

- System-on-a-Quilt (SoQ) for DSP applications



MPSoC with Network Quilts

- General, heterogeneous multiprocessor system based on **Network-on-Quilt (NoQ) tiles**



Quilted Metachips, SoQs, NoQs

CONCLUSION

Summary of QP Features…

- Provides enormous bandwidth potential for analog and digital systems
  - Direct-coupled millimeter-wave signals with extremely low loss
  - Resonance-free, dc-coupled channel for digital signaling; no equalization needed
- Savings in decreased chip area offsets the additional fabrication costs – more die per wafer
- Also provides benefits for RF, networking – extremely wide bandwidth, extremely low loss

…Summary of QP Features

- Quilt packaging is novel, unique and versatile
  - Applications to new system architectures
    - High speed, excellent signal integrity
    - Smaller form factor, reduced weight
  - Enables heterogeneous integration of dissimilar material systems, incompatible fabrication processes
  - Extremely wide bandwidths with good signal integrity
  - Intrinsic loss:
    - < 0.1 dB from 50 MHz - 100 GHz
    - Bandwidth > 200 GHz from simulations

Conclusions

- **Mapping SoC or NoC to the physical chips determines the IC fabrication economy**

  Economy improves significantly via a metachip

  Quilt nodule overhead << 1 % of silicon area

- **Quilted architectures (SoQ, NoQ)** enable efficient optimization and novel systems
  - SoCs with faster and larger memory
  - NoC with unprecedented size and complexity
  - Heterogeneous integration