Call for Papers

Fifth International Workshop on

Network on Chip Architectures

To be held in conjunction with the
45th Annual IEEE/ACM International Symposium on Microarchitecture
December 4, 2012
Vancouver, BC, Canada

http://nocarc.unikore.it/

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General Information

By entering into the ultra deep sub-micron (UDSM) era, the role played by the on-chip communication system is getting more and more relevance. In fact, as technology shrinks, gates become faster and more power efficient whereas wires become slower and more power hungry. Thus, the on-chip communication system represents one of the most important elements which determine the overall performance, cost, reliability, and energy consumption of a modern multi-processor system-on-chip (MPSoC). If the raw computation horsepower seems to be unlimited thanks to the ability of instancing more and more cores in a single silicon die, scalability issues, due to the need of making efficient and reliable the communication between the increasing number of cores, becomes the real problem. Several phenomena like communication errors (due to crosstalk, electromagnetic interference, inter-symbol interference, etc.), link latency, link power dissipation, etc., that were considered negligible in the previous technologies, are dominant in current and next generation MPSoC. The network-on-chip (NoC) paradigm is considered as the most viable solution for designing on-chip communication systems able to tackle with the above issues. The goal of the workshop is to provide a forum for researchers to present and discuss innovative ideas and solutions related to design and implementation of multi-core systems on chip.

Areas of Interest

This workshop focuses on issues related to design, analysis and testing of on-chip networks. The topics of specific interest for the workshop include, but are not limited to:

- Topologies selection and synthesis for NoCs and MPSoCs
- Routing algorithms and router micro-architectures
- QoS in on-chip communication
- Mapping of cores to NoC slots
- Power and energy issues
- Fault tolerance and reliability issues
- Memory architectures for NoC
- Dynamic on-chip network reconfiguration
- Modeling and evaluation of on-chip networks
- On-chip interconnection network simulators and emulators
- Analytical analysis methods for NoC performance and other properties
- Verification, debug and test of NoC
- 3D NoC architectures
- Emerging technologies and new design paradigms
- Industrial case studies of SoC designs using the NoC paradigm

Submission Guidelines

Both research and application-oriented papers are welcome. All papers should be submitted electronically by EasyChair. Submissions must be limited to 6 pages. Please, visit the workshop webpage for additional information about the submission process.

Important Dates

Abstract submission deadline	September 16, 2012
Full paper submission deadline	September 23, 2012
Author notification	October 22, 2012
Camera-ready version due	November 4, 2012
NoCArc Workshop	December 1, 2012