Call for Papers

NoCArc 2011

http://nocarc.unikore.it/

Fourth International Workshop on

Network on Chip Architectures

To be held in conjunction with the
44th Annual IEEE/ACM International Symposium on Microarchitecture
December 4, 2011
Porto Alegre, Brazil

Workshop Organizers

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General Information

The On-chip communication system represents one of the most important elements which determine the overall performance, cost, reliability, and energy consumption of a modern multi-processor system-on-chip (MPSoC). The role played by the communication infrastructure is predicted to become more and more important in the future technology nodes. Several phenomena like communication errors (due to crosstalk, electromagnetic interference, inter-symbol interference, etc.), link latency, link power dissipation, etc., that were considered negligible in the previous technologies, are dominant in current and next generation MPSoC. In addition, as approaching the many-cores era, in which hundreds or thousands of communicating on-chip cores represent the basic scenario, scalability issues must be properly addressed to meet performance, power and reliability requirements which characterize future ambient intelligent applications. The network-on-chip (NoC) paradigm is considered as the most viable solution for designing on-chip communication systems able to tackle with the above issues. The goal of the workshop is to provide a forum for researchers to present and discuss innovative ideas and solutions related to design and implementation of multi-core systems on chip. Besides regular papers, papers describing work in progress or incomplete but sound new innovative ideas related to the workshop theme are also encouraged.

Areas of Interest

This workshop focuses on issues related to design, analysis and testing of on-chip networks. The topics of specific interest for the workshop include, but are not limited to:

- Topologies selection and synthesis for NoCs and MPSoCs
- Routing algorithms and router micro-architectures
- QoS in on-chip communication
- Mapping of cores to NoC slots
- Power and energy issues
- Fault tolerance and reliability issues
- Memory architectures for NoC
- Dynamic on-chip network reconfiguration
- Modeling and evaluation of on-chip networks
- On-chip interconnection network simulators and emulators
- Analytical analysis methods for NoC performance and other properties
- Verification, debug and test of NoC
- 3D NoC architectures
- Emerging technologies and new design paradigms
- Industrial case studies of SoC designs using the NoC paradigm

Submission Guidelines

Both research and application-oriented papers are welcome. All papers should be submitted electronically by EasyChair (additional information in the website). Papers must be in PDF format and should include title, authors and affiliation, e-mail address of the contact author.

Papers must be formatted in accordance to the ACM style. ACM Word or LaTeX style templates are available in the website. In addition, Authors should apply ACM Computing Classification categories and terms. In order to be published, accepted papers must show a bibliographic strip containing the copyright statement (see web).

Submissions must be limited to 6 pages. Papers deviating significantly from these paper size and formatting rules may be rejected without review. If the authors wish a blind review to be performed, then the author's name and affiliation should be omitted in the submitted paper. In case of any questions please contact the workshop organizers.

Important Dates

Paper submission deadline	September 18, 2011
Author notification	October 18, 2011
Camera-ready version due	November 5, 2011
NoCArc Workshop	December 4, 2011