Third International Workshop on
Network on Chip Architectures

To be held in conjunction with the
43rd Annual IEEE/ACM International Symposium on Microarchitecture
December 4-8, 2010
Atlanta, Georgia, USA

http://nocarc.diit.unict.it/

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General Information

As the number of cores integrated into a System-on-Chip (SoC) increases, the role played by the interconnection system becomes more and more important. The International Technology Roadmap for Semiconductors depicts the on-chip communication issues as the limiting factors for performance and power consumption in current and next generation SoCs. Design in the era of ultra-deep submicron (UDSM) silicon is mainly dominated by issues concerning the communication infrastructure. While SoCs consisting of tens of cores were common in the last decade, common predictions foresee that the next generation of many-core SoCs will contain hundreds or thousands of cores. In the many-core era, as the number of cores residing on the same SoC increases significantly, the communication solutions also need to change drastically in order to support the new inter-core communication demands. It is nowadays widely recognized that Network-on-Chip (NoC) architectures represent the most viable solution to cope with scalability issues of future many-cores systems and to meet performance, power and reliability requirements which characterize future ambient intelligent applications.

Areas of Interest

The topics of specific interest for the workshop include, but are not limited to:

- NoC Performance Analysis
- Dynamic On-chip Network Reconfiguration
- Topology Selection and Synthesis for NoCs and MPSoCs
- Modeling and Evaluation of On-chip Networks
- Routing Algorithms and Router Micro-architectures
- Design Space Exploration and Tradeoff Analysis
- Guaranteed Throughput and Real Time On-chip Communication
- On-chip Interconnection Network Simulators and Emulators
- Mapping of Cores to NoCs
- Validation, Debug and Test of NoCs and MPSoCs
- Power and Energy Issues
- 3D NoC Architectures
- Fault Tolerance and Reliability Issues
- Emerging Technologies and New Design Paradigms
- Memory Architectures for NoC
- Industrial Case Studies of MPSoCs using the NoC Paradigm

The goal of the workshop is to provide a forum for researchers to present and discuss innovative ideas and solutions related to design and implementation of multi-core systems on chip. Besides regular papers, papers describing work in progress or incomplete but sound new innovative ideas related to the workshop theme are also encouraged.

Submission Guidelines

Both research and application-oriented papers are welcome. All papers should be submitted electronically by EasyChair (see the website for details). Papers must be in PDF format and should include title, authors and affiliation, e-mail address of the contact author. Papers must be formatted in accordance to the ACM style. ACM Word or LaTeX style templates are available in the web site. In addition, Authors should apply ACM Computing Classification categories and terms. Submissions must be limited to 6 pages. Papers deviating significantly from these paper size and formatting rules may be rejected without review. If the authors wish a blind review to be performed, then the author's name and affiliation should be omitted in the submitted paper. In case of any questions please contact the workshop organizers.

Important Dates

Final paper submission deadline	September 18, 2010
Author notification	October 18, 2010
Camera-ready version due	November 5, 2010
NoCArc Workshop	December 4 (or 5), 2010 (To be finalized)