Second International Workshop on

Network on Chip Architectures

Maurizio Palesi and Shashi Kumar

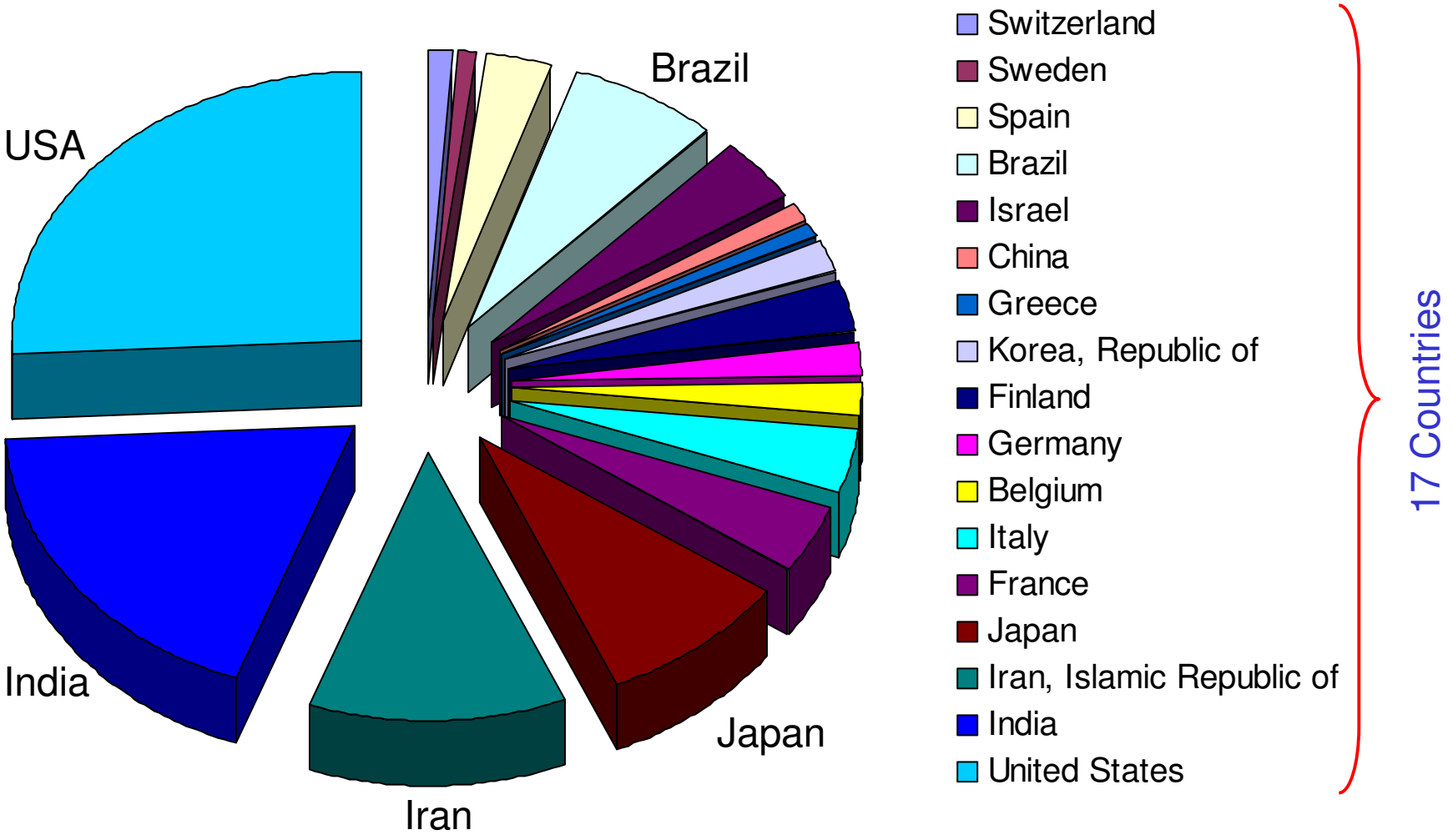
December 12, 2009

New York, New York, USA

About NoCArc

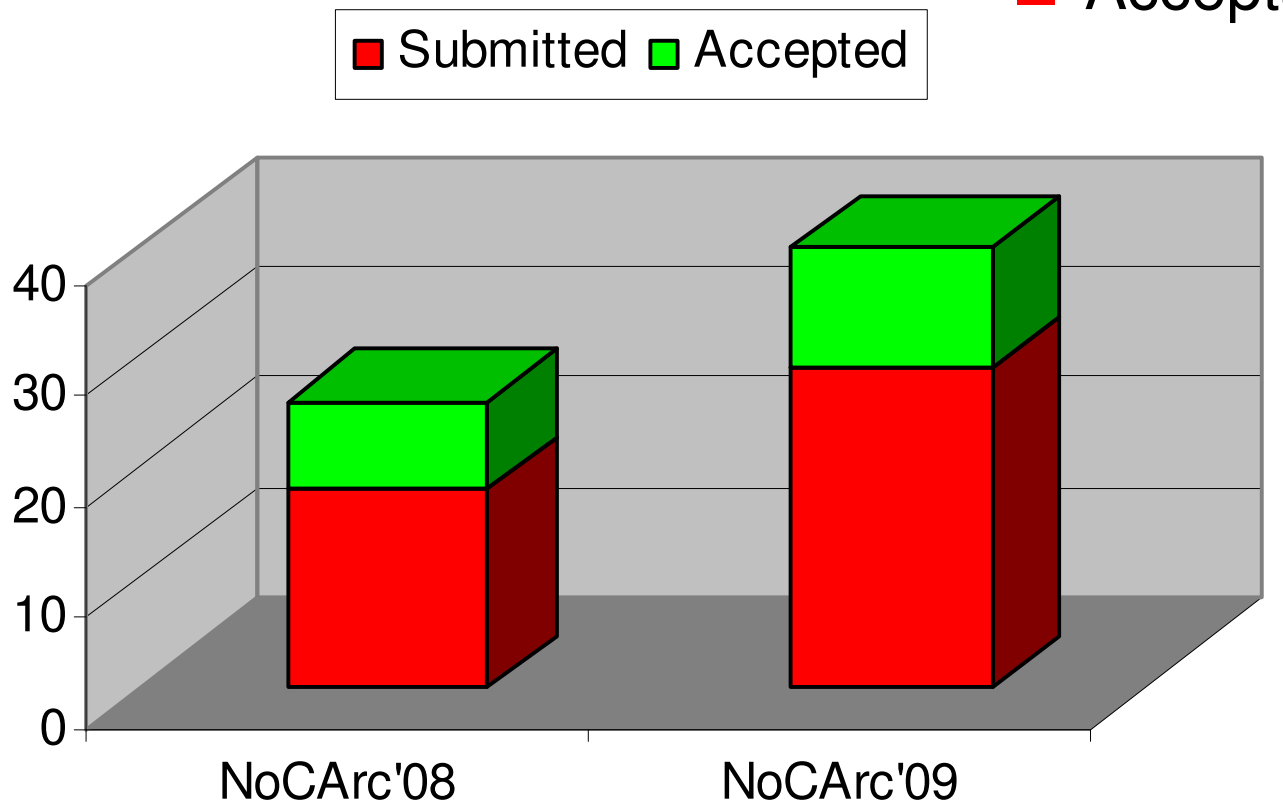
- Focus of the Workshop
  - Issues related to design, analysis and testing of on-chip networks
- Areas of Interest
  - Architectures and Topologies for NoCs and MPSoCs
  - Routing algorithms and Router Micro-architectures
  - Fault tolerance, reliability and testing issues
  - Dynamic on-chip network reconfiguration
  - Modeling and evaluation of on-chip networks
  - Design space exploration and tradeoff analysis
  - On-chip interconnection network simulators and emulators
  - Industrial case studies of SoC designs using the NoC paradigm
- Goal of the Workshop
  - To provide a forum for researchers to present and discuss innovative ideas and solutions related to design and implementation of multi-core systems on chip

Countries & Authors



Acceptance Rate

- **29** regular submissions
- **11** Accepted papers
- Acceptance rate of **38%**



Program

- Keynote talk
  - Radu Marculescu, *CMU*
    Toward a Science for Future NoC Design
- Two invited papers
  - Architecture Design Principles for the Integration of Synchronization Interfaces into Network-on-Chip Switches, by D. Ludovici, A. Strano, D. Bertozzi - TUDelft, Netherlands and University of Ferrara, Italy
  - Hybrid Wireless Network on Chip: A New Paradigm in Multi-Core Design, by P. Pande, A. Ganguly, K. Chang, C. Teuscher - Washington State University and Portland State University

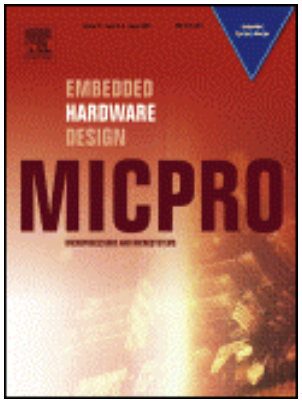
Program (*cnt.*)

- Four sessions
  - ➔ Router Arechitectures & Routing Algorithms (*4 papers*)
  - ➔ Design Methodologies & Mapping (*3 papers*)
  - ➔ Low Power Techniques & Performance Evaluation (3 papers)
  - ➔ Emerging Technologies & Novel Ideas (*3 papers*)

Proceedings

- Digital libraries

- Special Issue on ***Network-on-Chip Architectures and Design Methodologies*** in Microprocessors and Microsystems Journal, Elsevier
  - ➔ Guest Editors: *S. Kumar, R. Marculescu, M. Palesi*



Acknowledgments

Technical Program Committee

- Federico Angiolini
- Giuseppe Ascia
- Davide Bertozzi
- Giorgos Dimitrakopoulos
- Natalie Enright Jerger
- Manoj Singh Gaur
- José Flich Cardo
- Martti Forsell
- Ahmed Hemani
- Yuho Jin
- Anshul Kumar
- Shashi Kumar
- Marcello Lajolo
- Zhonghai Lu
- Radu Marculescu
- Juan Manuel Orduña Huertas
- Gianluca Palermo
- Maurizio Palesi
- Davide Patti
- Partha P. Pande
- Carlo Pistritto
- Alberto Scandurra
- Virendra Singh
- Tor Skeie
- Christof Teuscher
- Mei Yang
- Vittorio Zaccaria

Why NoCArC?

- Yet Another NoC Conference?
  - ➔ Only one conference dedicated to NoC
    - ✓ Network on Chip Symposium (NoCS): Annual Event
  - ➔ Related Workshops
    - ✓ Interconnection Network Architectures: On chip Multi-chip (INA-OCMC)
    - ✓ Communication Architecture Conference (CAC)
  - ➔ Special Track, Special sessions on NoC in almost all VLSI and DA conferences
    - ✓ VLSI Design, DATE, DAC, ICCAD, Euro-micro DSD

What can NoCArC Provide?

- Focus on all issues related to NoC Architectures
  - ➔ Collect and highlight important contibutions for industry and education
  - ➔ Identify the gaps and address those gaps
    - ✓ Memory architectures for NoC based systems
    - ✓ Fault tolerance, testing and reliability issues
    - ✓ Mathematical foundations and Science for NoC design
- Opportunity to large research community
  - ➔ Research community has really grown over the last five years and needs more publication opportunities
- NoCArc can slowly expand and provide a platform for growth of this area.

Keynote Talk

- **Title: Toward a Science for Future NoC Design**
- **Speaker: Radu Marculescu**