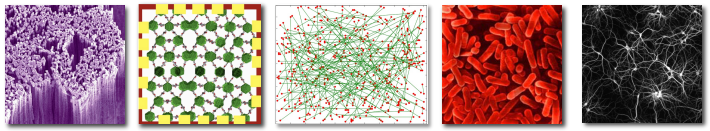
Christof Teuscher, Neha Parashar, Mrugesh Mote, Nolan Hergert, Jonathan Aherne

Wire Cost and Communication Analysis of Self-Assembled Interconnect Models for Networks-on-Chip

Portland State University
Department of Electrical and Computer Engineering (ECE)
www.teuscher-lab.com | www.teuscher-lab.com/christof
teuscher@pdx.edu

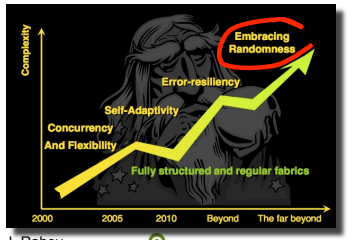


Emerging Interconnects

- The top-down way we fabricate electronic chips is not sustainable at the current pace of progress.
- Bottom-up self-assembled computers are the holy grail of molecular and nanotechnology.
- We lack control over such techniques, thus, interconnects will be partly or largely unstructured and imperfect.
- Such interconnects would be easier and cheaper to build in massive scale.

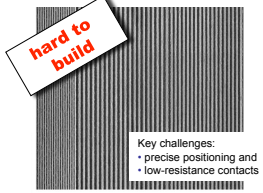
"It is unclear whether it is necessary or even possible to control the precise regular placement and interconnection of these diminutive molecular systems." (Tour, 2002)

"Self-assembly makes it relatively easy to form a random array of wires with randomly attached switches." (Zhirnov & Herr, 2001)

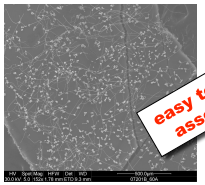


J. Rabey

Fabricating Unstructured Nanowire Assemblies

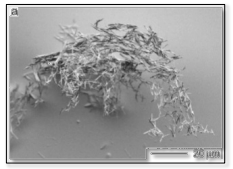


Melosh et al., Science, 2003

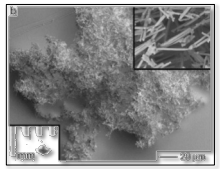


Polyaniline (PANI) conductive polymer, LANL, Wang et al.

- Prototypes of randomly assembled nanowire assemblies for novel interconnects are currently being built by collaborators at Los Alamos National Laboratory (LANL).

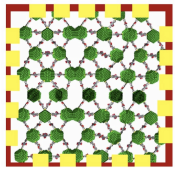


Gracias team, John Hopkins University

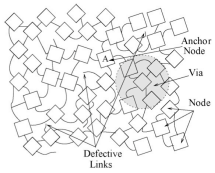


Gu et al., Three-Dimensional Electrically Interconnected Nanowire Networks Formed by Diffusion Bonding, *Langmuir 2007, 23, 979-982.*

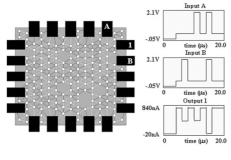
Examples of Unstructured Devices



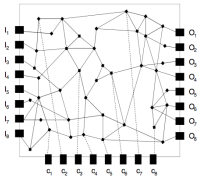
→ J. M. Seminario et al. **The Nanocell: A Chemically Assembled Molecular Electronic Circuit**. IEEE Sensors Journal, 6(6):1614-1626, 2006.



→ Pathwardhan, Dwyer, Lebeck. **A Self-Organizing Defect Tolerant SIMD Architecture**, ACM J. Emerg. Technol. Comput. Syst. 3, 2, Article 10 (July 2007)



→ J. Tour et al. **Nanocell Logic Gates for Molecular Computing**. IEEE Transactions on Nanotechnology, 1 (2):100-109, 2002.



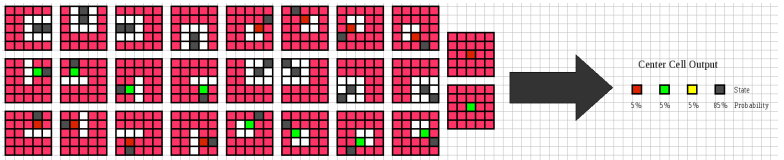
→ J. Lawson, D. H. Wolpert. **Adaptive Programming of Unconventional Nano-Architectures**. Journal of Computational and Theoretical Nanoscience, 3, 272-279 (2006).

Contributions of this Paper

- Two physically-plausible models for generating unstructured NoC interconnects:
  - wire deposition
  - direct wire growth
- Consider the wiring cost
- Investigate NoC design trade-offs of these models.
- Compare with other non-classical NoC models
- Use of evolutionary algorithms to validate assumptions.

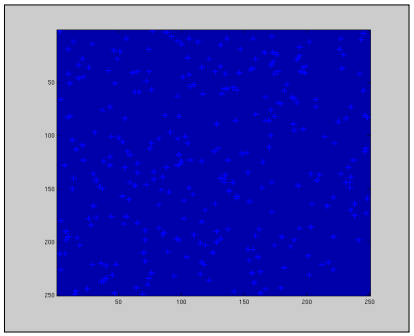
Wire Growth Model

- Probabilistic cellular automata (CA)
- Grid of cells
  - Each cell can be in one of multiple states
  - Cell states are updated depending on the neighbor cells
- Wires start growing from seed points in a random direction
- Wires turn with a certain probability *t*
- Wires stop growing with a certain probability *s*

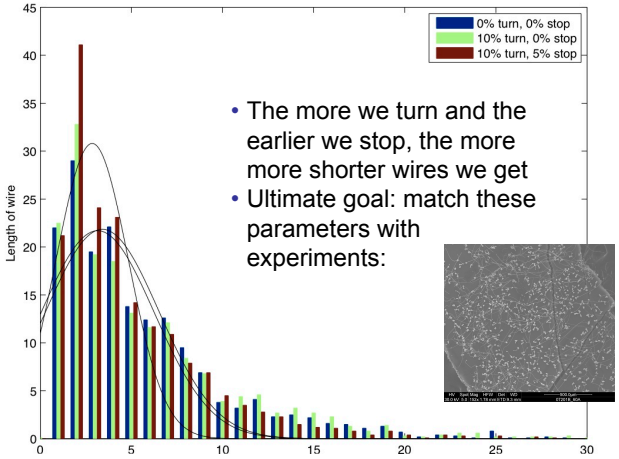


Wire Growth Model

- Model parameters: (1) number of seed points *N*, (2) turn probability *t*, (2) stop probability *s*



Results: Wire-length Distribution



- The more we turn and the earlier we stop, the more more shorter wires we get
- Ultimate goal: match these parameters with experiments:

Levitan's Model

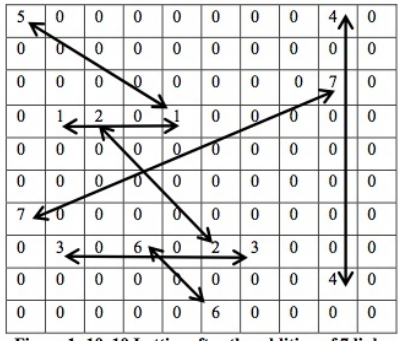
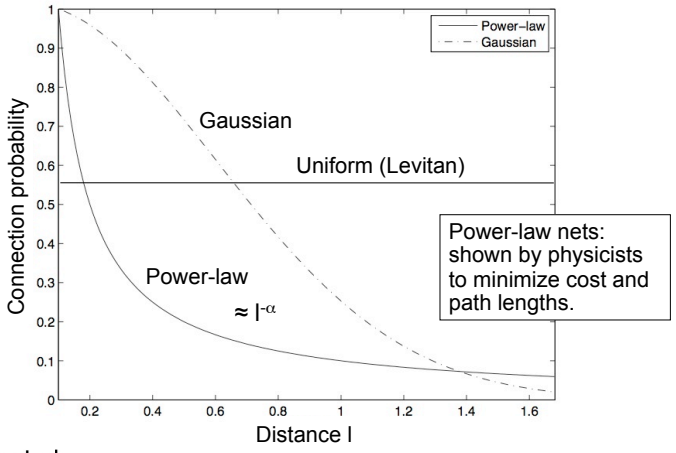


Figure 1: 10x10 Lattice after the addition of 7 links

- Drop wires with uniform length distribution on a surface
- They form a network
- On a √Nx√N grid, 80% of the cells can be connected into a single spanning tree with only N wires
- Example: 100 wires

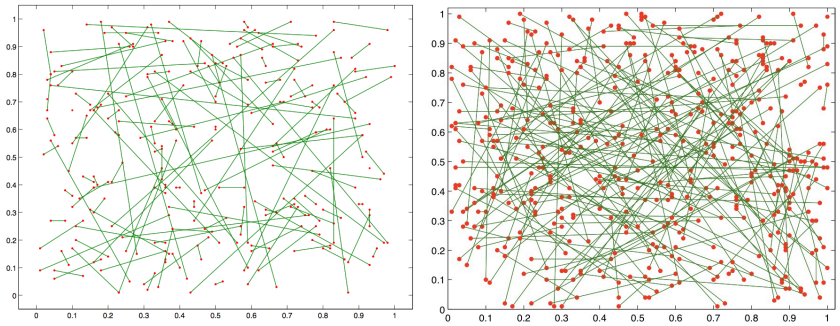
S. P. Levitan. **You can get there from here: Connectivity of random graphs on grids**. In Proceedings of the *Design Automation Conference* (DAC 2007), pages 272–273, San Diego, CA, Jun 4–7 2007. ACM.

Power-law Wire Length Distribution

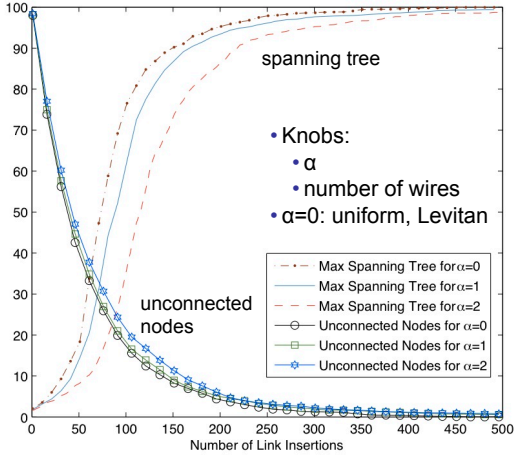


Our Wire Drop Model

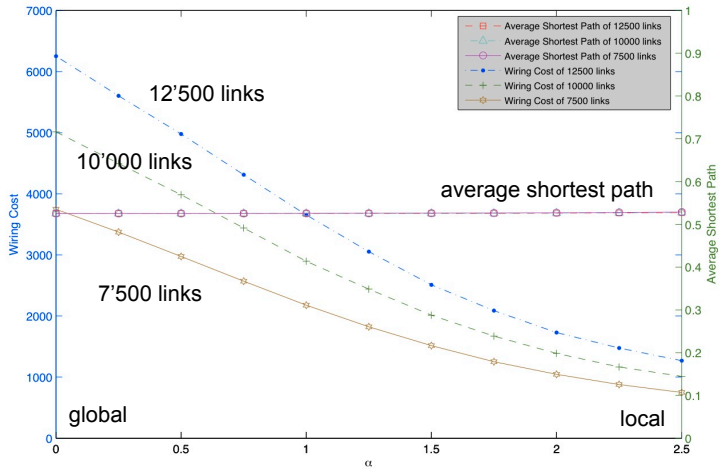
- Drop wires with power-law length distribution on a surface: $l^{-\alpha}$
- Decreases the total number of additional wires required and thus the wiring cost.



Results: Spanning Tree and Unconnected Nodes



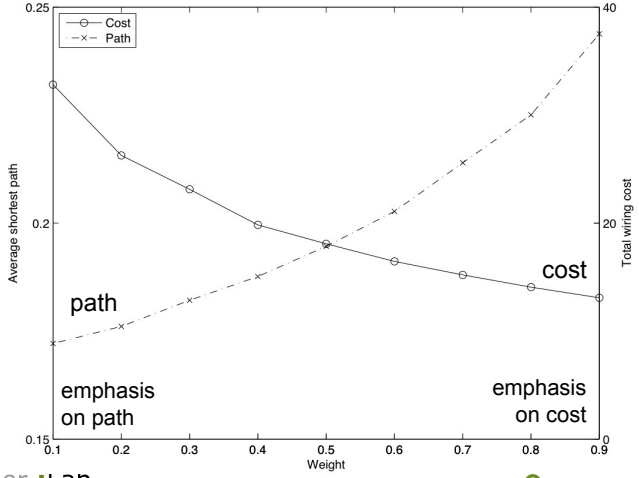
Results: Wiring Cost



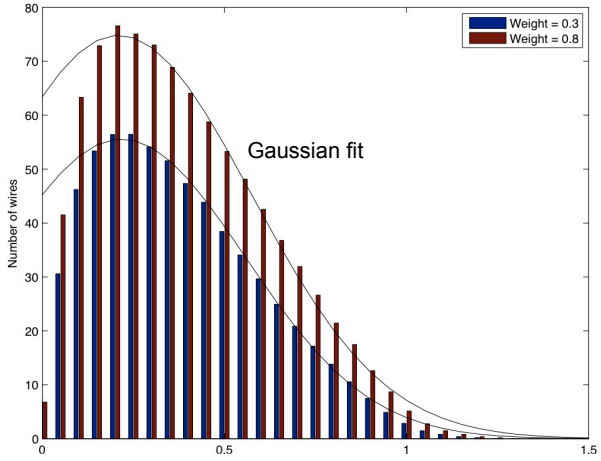
Network Optimization by Evolutionary Algorithms

- Evolutionary algorithms (EA) are a metaheuristic optimization technique inspired by natural evolution.
- **Given**: *N* nodes
- **Questions**:
  - how to interconnect these nodes to maximize performance (average shortest path) and minimize cost (wire length)
  - what wire-length distribution evolves?
- Model parameter:
  - weight factor *a*
  - f= *a* x average shortest path + (1 - *a*) x cost

Results: Cost versus Average Path Length



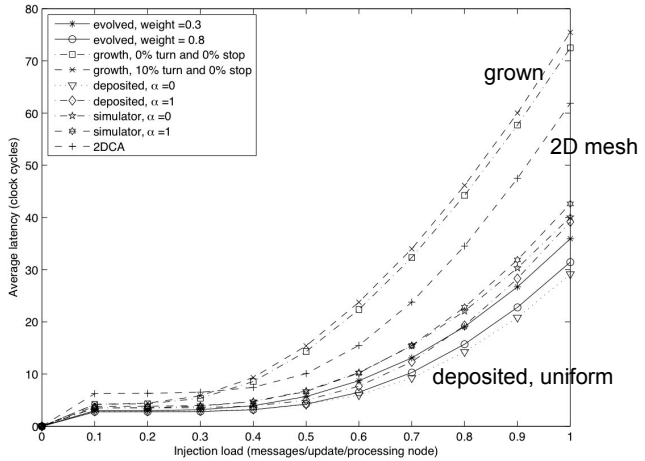
Results: Wire Length Distribution



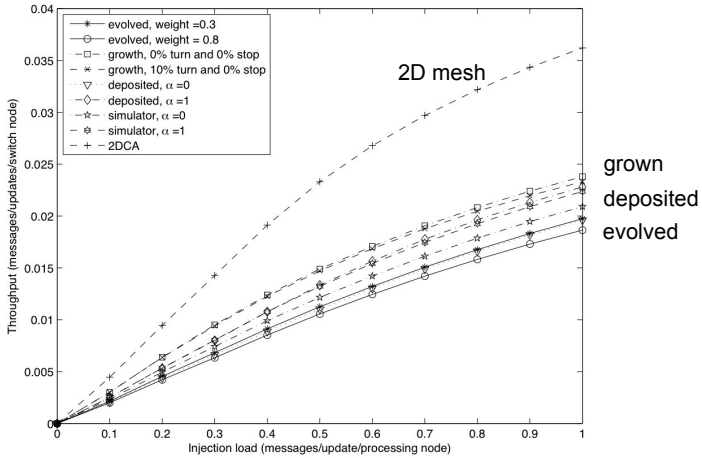
Evaluation in NoC Framework

- Evaluate the networks from the two models and the evolutionary algorithm in a more realistic framework.
- Processing and switch nodes
- Virtual channels
- Shortest path routing
- Random traffic model
- 64 nodes
- 2D mesh for a baseline comparison

Results: Average Latency



Results: Throughput



Results: Average Path and Wiring Cost

Network	Average shortest path [dist. units]	Total wire cost [dist. units]
Evolved, Weight = 0.3	0.54	226.52
Evolved, Weight = 0.8	0.53	326.43
Deposited, $\alpha = 0$	0.60	292.07
Deposited, $\alpha = 1$	0.57	95.679
Growth, 0%turn, 0%stop	0.54	58.374
Growth, 10%turn, 0%stop	0.56	57.403
2D CA mesh, simulator,	0.76	16.905
2D random, $\alpha = 0$, simulator	0.87	186.6
2D random, $\alpha = 1$, simulator	0.61	94.697

Conclusions

- Self-assembled NoCs will be largely unstructured.
- This is much better than it sounds: with the right paradigms, they are beneficial in terms of **performance**, **wiring cost**, **robustness,** and **scalability** against failures.
- Reason: bottom-up fabrication results in wire-length distributions that are driven by resource constraints (volume, area, time). We are in a "**physical sweet spot**"
- Specific wire-length distributions allow to reduce the total wiring cost (and thus the energy consumption).

References

- **Abstract NoC framework, unstructured NoC, benefits of randomness**
  - C. Teuscher. Nature-inspired interconnects for emerging large-scale network-on-chip designs. *Chaos*, 17(2):026106, 2007. arXiv:0704.2852
  - C. Teuscher and A. A. Hansson. Non-Traditional Irregular Interconnects for Massive Scale SoC. *IEEE International Symposium on Circuits and Systems, ISCAS 2008*, Seattle, May 18-21, 2008, pages 2785-2788
- **Damage spreading and robustness in random dynamical networks:**
  - T. Rohlf, N. Gulbahce, and C. Teuscher. Damage spreading and criticality in finite random dynamical networks. *Physical Review Letters*, 99(24):248701, 2007. arXiv:cond-mat/0701601
  - Q. Lu, C. Teuscher. Damage Spreading in Spatial and Small-world Random Boolean Networks. In revision. arxiv:cond-mat/0904.4052
- **Architectural and computing considerations:**
  - C. Teuscher, N. Gulbahce, and T. Rohlf. Assessing Random Dynamical Network Architectures for Nanoelectronics. Proceedings of the *IEEE/ACM Symposium on Nanoscale Architectures, NANOARCH 2008*, Anaheim, CA, USA, Jun 12-13, 2008. arXiv:0805.2684
  - C. Teuscher, N. Gulbahce, and T. Rohlf. An Assessment of Random Dynamical Network Automata for Nanoelectronics. In press.

Check it out!

www.teuscher-lab.com

LinkedIn myspace facebook twitter