First International Workshop on

Network on Chip Architectures

November 8th, 2008

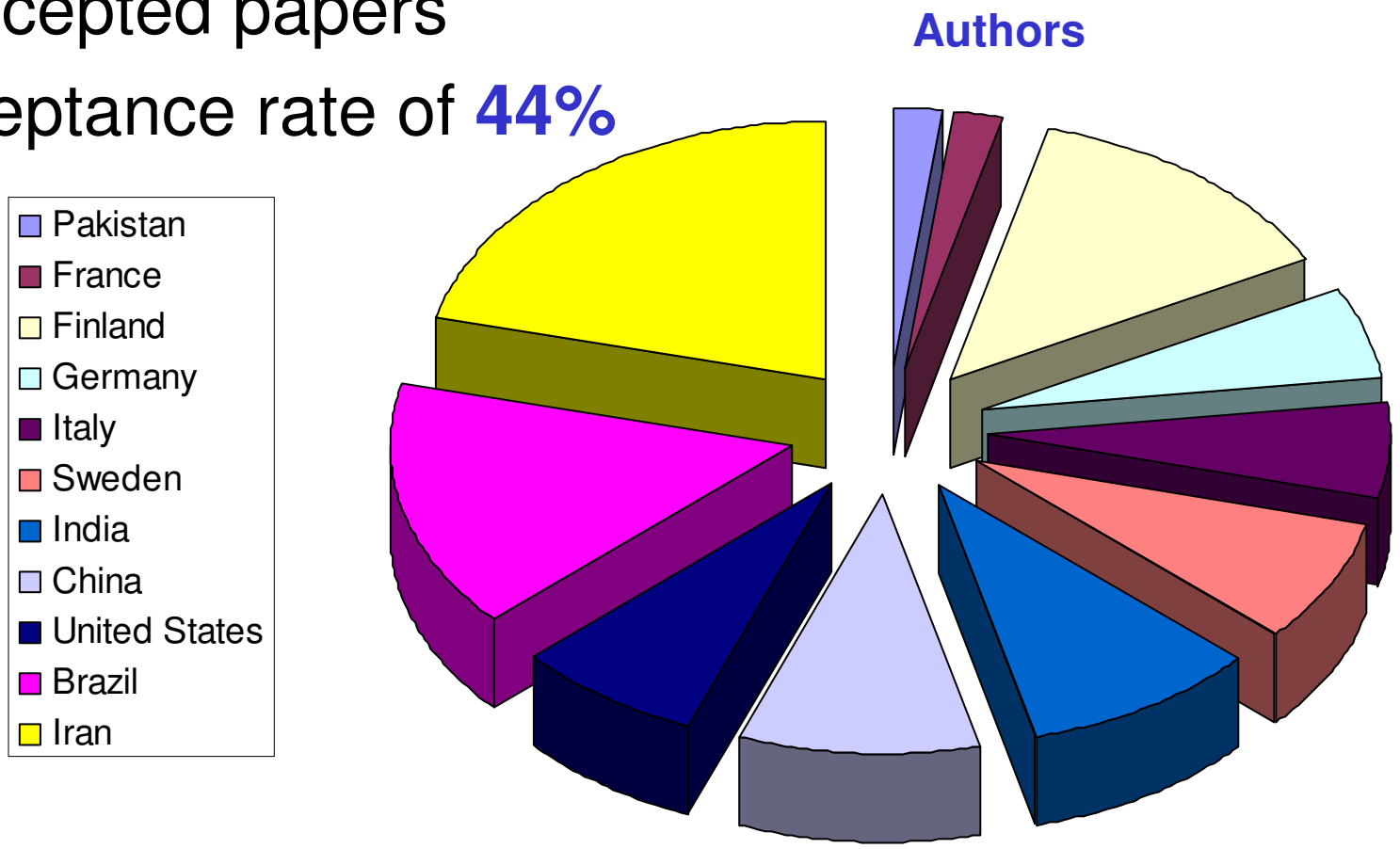
Lake Como, Italy

About NoCArc

- Focus of the Workshop
  - Issues related to design, analysis and testing of on-chip networks
- Areas of Interest
  - Architectures and Topologies for NoCs and MPSoCs
  - Routing algorithms and Router Micro-architectures
  - Fault tolerance, reliability and testing issues
  - Dynamic on-chip network reconfiguration
  - Modeling and evaluation of on-chip networks
  - Design space exploration and tradeoff analysis
  - On-chip interconnection network simulators and emulators
  - Industrial case studies of SoC designs using the NoC paradigm
- Goal of the Workshop
  - To provide a forum for researchers to present and discuss innovative ideas and solutions related to design and implementation of multi-core systems on chip

Submissions

- 18 submissions
- 8 accepted papers
- Acceptance rate of 44%



Program

- Three sessions + 1 Keynote talk
  - Router Microarchitecture (*2 papers*)
  - Performance Evaluation (*3 papers*)
  - Prospective Architectural Proposals (*3 papers*)

- Keynote talk by ***José Duato***
  - Managing Heterogeneity in Future NoCs

Proceedings

- Only informal proceedings in this edition
- Dissemination of the papers
  - ➔ Papers and slides will be published to the NoCArc web page
  - ➔ An invitation to download the proceedings will be sent to ML in this area

Acknowledgments

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