

Special Issue on

Network-on-Chip Architectures and Design Methodologies in

Microprocessors and Microsystems - Embedded Hardware Design

The Elsevier Embedded Hardware Design (MICPRO) Journal seeks original manuscripts for a Special Issue on Networks-on-Chip (NoCs) scheduled to appear in the second half of 2010.

Continuous reduction in the time-to-market required by the telecommunications, multimedia and consumer electronics market makes full-custom design inappropriate and has led to the definition of design methodologies based on the reuse of Intellectual Properties (IPs, or cores). In turn, this has caused an increase in the complexity and heterogeneity of single chip based implementations of embedded applications. While systems-on-chip (SoCs) consisting of tens of cores were common in the last decade, common predictions foresee that the next generation of many-cores SoC will contain hundred or thousands of cores. In the many core era, as the number of cores residing on the same SoC increases significantly, the communication solutions also need to change drastically in order to support the new inter-core communication demands. Indeed, nowadays, it is widely recognized that traditional bus-based interconnect architectures are no longer adequate for deep-sub-micron (DSM) technologies. Instead, the network-on-Chip (NoC) is generally viewed as the ultimate solution for the design of modular and scalable communication architectures, able to provide inherent support to the integration of heterogeneous cores through the standardization of the network boundary.

This Special Issue is focused on issues related to architectures and design methodologies of on-chip interconnection networks based on the NoC paradigm. The goal of the Special Issue is to provide a forum for researchers to present and discuss innovative ideas and solutions related to design and implementation of multi-core systems on chip.

All authors who presented papers at NoCArc 2009 are encouraged to submit an extended version of their paper to MICPRO for possible inclusion in this special issue. However, besides submissions based on NoCArc 2009 papers, other high quality submissions within the scope of the special issue are also welcome. Each submission will be reviewed by at least three reviewers to ensure very high quality of selected papers for the special issue.

Areas of Interest

The topics of specific interest for this Special Issue include, but are not limited to:

- Topologies selection and architecture synthesis for NoCs
- Routing algorithms and router micro-architectures
- Guaranteed throughput and real-time on-chip communication
- Mapping of cores to NoC nodes
- Power and energy issues
- Fault tolerance and reliability issues
- Memory architectures for NoCs

- Programming and OS support for NoCs
- Dynamic on-chip network reconfiguration
- Modeling and evaluation of on-chip networks
- Design space exploration and tradeoff analysis
- On-chip interconnection network simulators and emulators
- Verification, debug and test of NoC
- Metrics and benchmarks for NoCs
- Performance and power estimation techniques
- Emerging technologies and new communication paradigms
- Case studies of SoC designs using the NoC paradigm

Submission Guidelines

The submitted papers must be written in English and describe original research which is neither published, nor currently under review by other journals or conferences. The author guidelines for preparation of manuscript can be found at <http://www.elsevier.com/locate/micpro>. All manuscripts and any supplementary material should be submitted through the Elsevier Editorial System (EES) at the following location <http://ees.elsevier.com/micpro/>. The authors must select "NoCArc 2009" when they reach the "Article Type" step in the submission process.

Note the following important dates.

Important Dates

Submission deadline:	March 12, 2010
Reviews completed by:	April 23, 2010
Revisions due by:	May 21, 2010
Reviews of revisions completed by:	June 18, 2010
Final decision:	July 1, 2010

Guest Editors

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