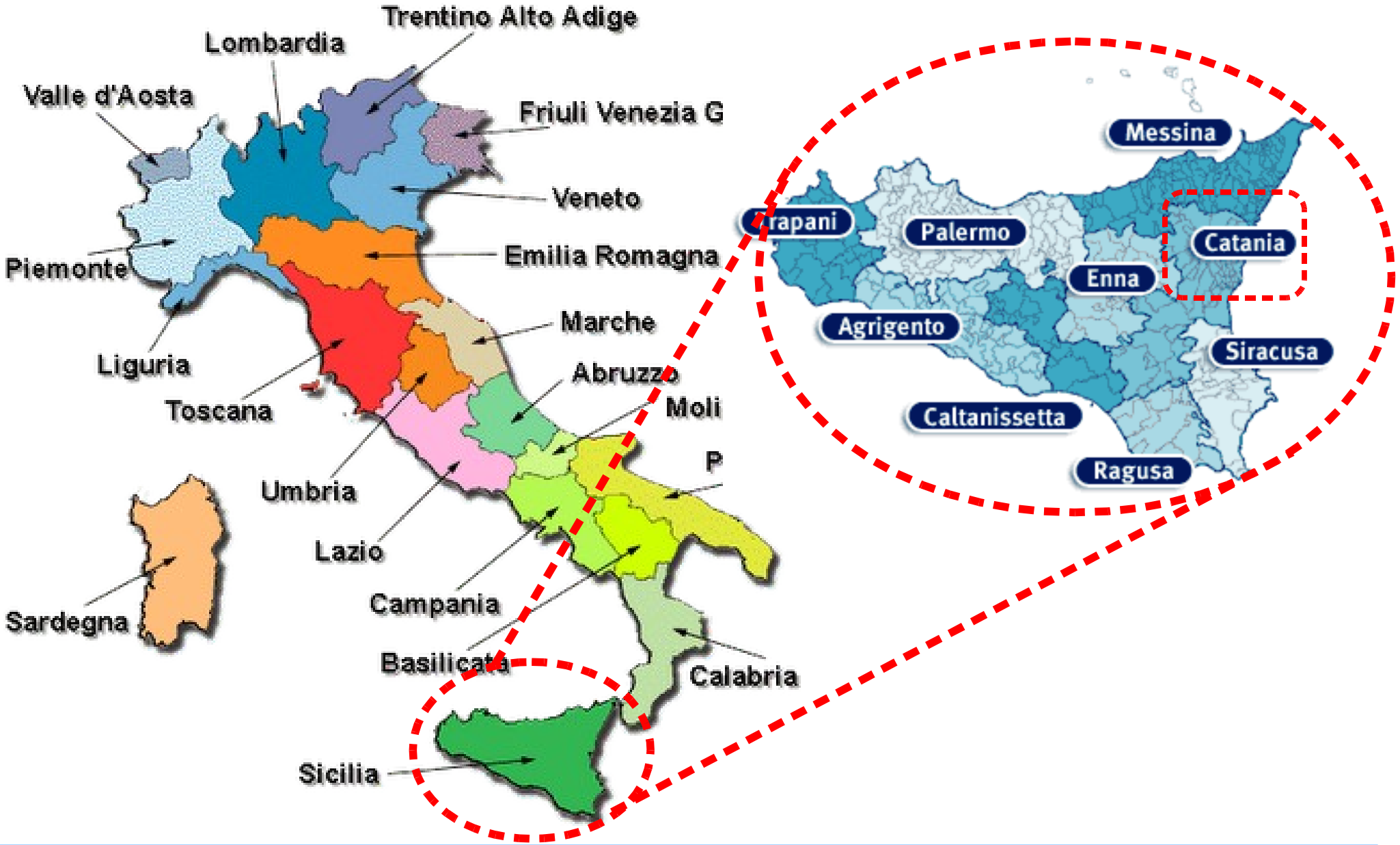
NoC Research Summary

Catania


Trentino Alto Adige
Lombardia
Valle d'Aosta
Friuli Venezia Giulia
Veneto
Piemonte
Emilia Romagna
Marche
Liguria
Abruzzo
Toscana
Molise
Puglia
Umbria
Lazio
Sardegna
Campania
Basilicata
Calabria
Sicilia

Catania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Toscana
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Umbria
Lazio
Campania
Basilicata
Calabria
Sardegna
Sicilia
Messina
Trapani
Palermo
Catania
Enna
Agrigento
Siracusa
Caltanissetta
Ragusa

UniCT

- 12 Faculties
- ~65,000 students
- Faculty of Engineering (6,000 students)
  - ➔ 7 Departments
    - ✔DAU: Architecture and Urban design
    - ✔DIEES: Electrical, Electronic and Systemics
    - ✔DICA: Civil
    - ✔DIIM: Industrial and Mechanics
    - ✔***DIIT: Informatics and Telecommunications***
    - ✔DM: Mathematic
    - ✔DMFCI: Physics and Chemistry

DIIT

- Department of Computer Science and Telecommunications Engineering (*DIIT*)
- ~50 people
- Research groups
  - ➔Computer Sciences
  - ➔Telecommunications
  - ➔Electromagnetic Fields

Research Areas of Interest

Computer Sciences

- Computer architectures
- Embedded systems
- Hardware/software codesign
- Operating systems
- Real time systems
- Peer to peer systems and applications
- Trust and reputation systems
- E-Learning technologies
- Sensor networks

- Self-organizing and self-adaptive systems
- Mobile agents
- Ubiquitous computing
- Human computer interaction

Research Areas of Interest

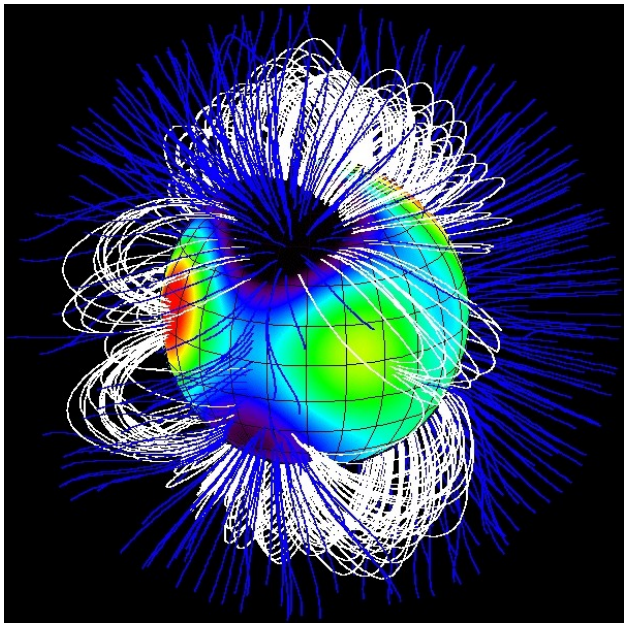
Telecommunications

- Speech signal classification and recognition
- Speech coding for mobile communications
- Digital signal processing in communications
- Distributed multimedia applications
- Multimedia traffic modeling and analysis
- Wireless and satellite networks
- Mobile systems
- Next generation internet
- Wireless sensor networks

Research Areas of Interest

Electromagnetic Fields

- Development of ultra-wideband antennas
- Interaction of microwaves with anisotropic media
- Single-mode solid-state waveguide lasers and amplifiers
- Computational electromagnetism



Industrial Cooperations

Academic Cooperations

- Austrian Academy of Sciences, Austria
- Institute for Industrial IT, Germany
- Institutfür Automation und Kommunikation, Germany
- University of Aveiro, Portugal
- University of York, UK
- University of Lund, Sweden
- University of Porto, Portugal
- Universitat Politècnica de Catalunya, Spain
- Malardalen Universuty, Sweden
- University of Illinois at Urbana Champain, USA
- Technical University of Vienna, Austria
- Halmstad University, Sweden
- Jönköping University, Sweden
- Universidad de Valencia, Spain
- Universidad Politecnica de Valencia, Spain
- Concordia University
- Columbia University, New York, USA
- Rice University, Houston, USA
- Dartmouth College, Dartmouth, USA
- German Aerospace Center (DLR), Munich, Germany
- University of California, Riverside, USA
- University of California, Irvine, USA
- Florida Institute of Technology
- Exeter University
- Centre for Research on Embedded Systems, University of Halmstad, Sweden
- Institute fur Automation und Kommunikation, Magdeburg, Germany
- State University of Aerospace instrumentation, San Pietroburgo, Russia
- Università of Craiova - Romania
- University of Helsinki, Finland
- Technical University of Cluj
- University Politehnica of Budapest
- University of Thessaloniki
- University of Edinburgh
- National Center for High-performance Computing (NCHC) - Taiwan
- CoSBi - The Microsoft Research - University of Trento Centre for
- Computational and Systems Biology
- Georgia Institute of Technology, Atlanta, USA
- University of Cyprus, Cyprus

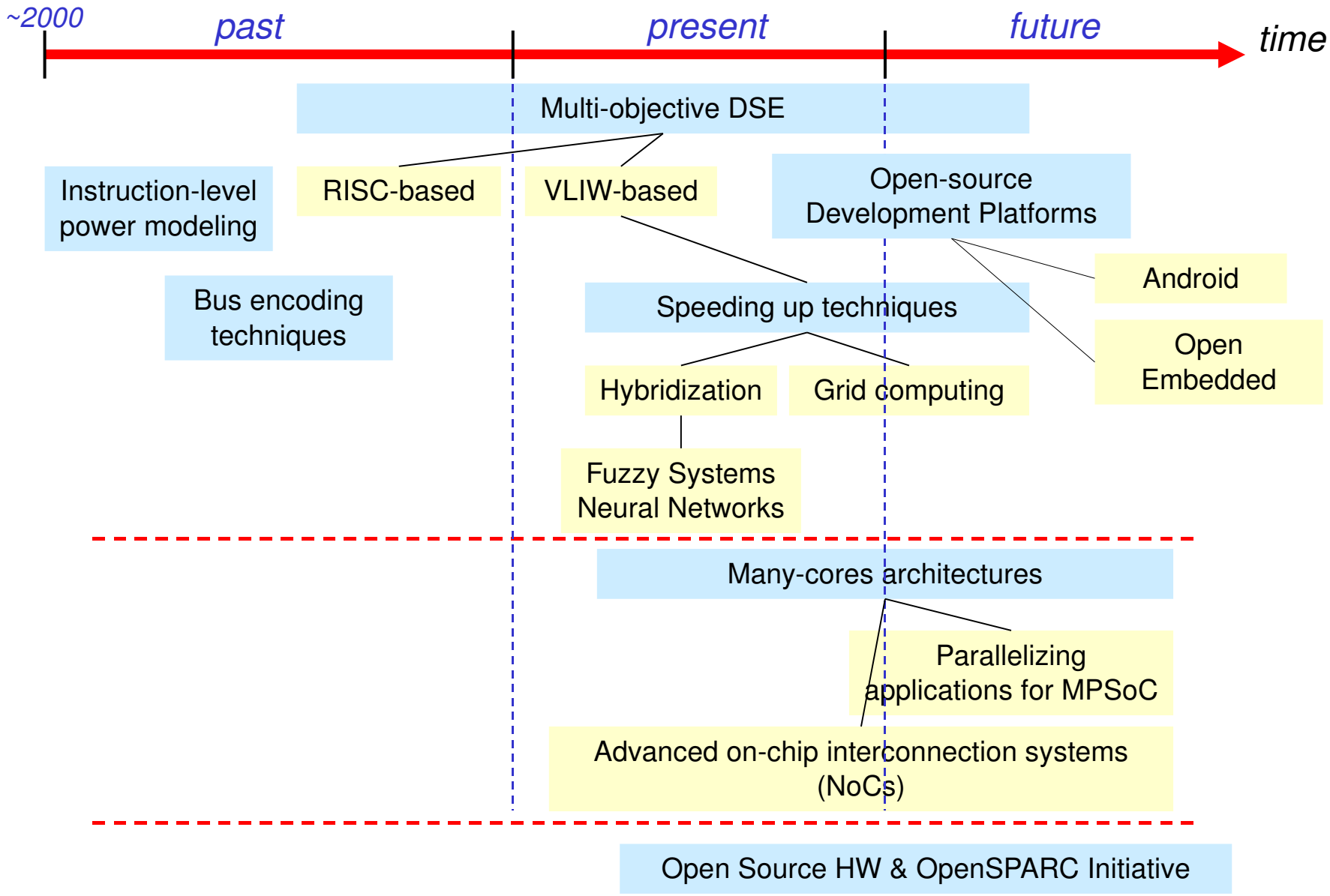
European Projects

- **NEWCOM** - Network of Eecellence in Wireless Communications
- **CRUISE** - Creating Ubiquitous Intelligent Sensing Environments
- **I-TRACE** - Interactive Tracing and Graphical Annotation in Pen-based e-learning
- **flexWARE** - Flexible Wireless Automation in Real-Time Enviroments
- **P2P-PROVIDEO** - P2P middleware for deployment of an innovative business model for the provision of a QoS-aware video multicast transport service over the Internet

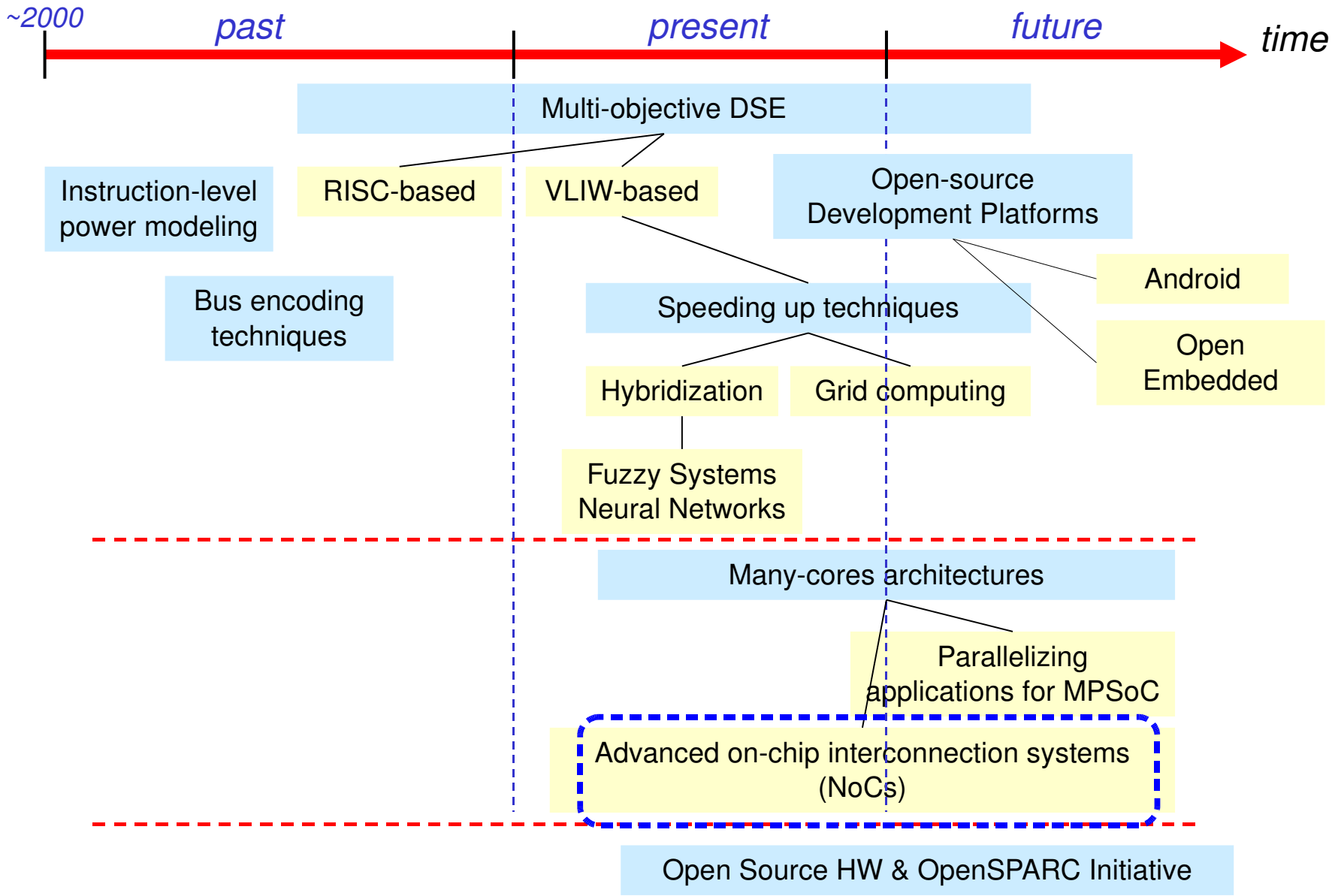
Team

- Vincenzo Catania, *Full Professor*
- Giuseppe Ascia, *Associate Professor*
- Daniela Panno, *Associate Professor*
- Maurizio Palesi, *Contract Researcher*
- Davide Patti, *Contract Researcher*
- Alessandro G. Di Nuovo, *Contract Researcher*
- Fabrizio Fazzino, *PhD Student*
- Master thesis students
- Undergraduate students

Research Topics in ES Area



Research Topics in ES Area



Outline

- Application Specific Routing Algorithms
- Concurrent Mapping and Routing
- Dealing with Manufacturing Defects
- Encoding Scheme for Low Power

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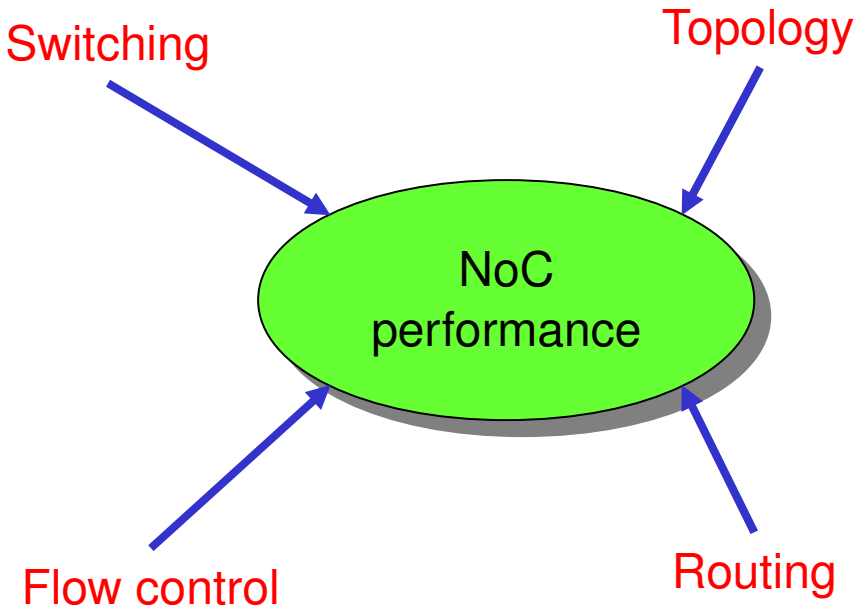
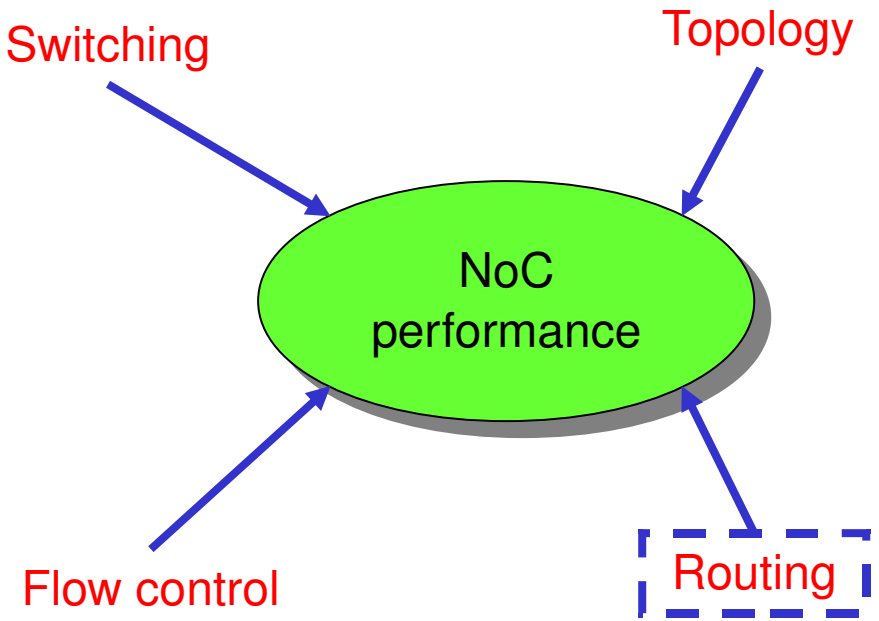
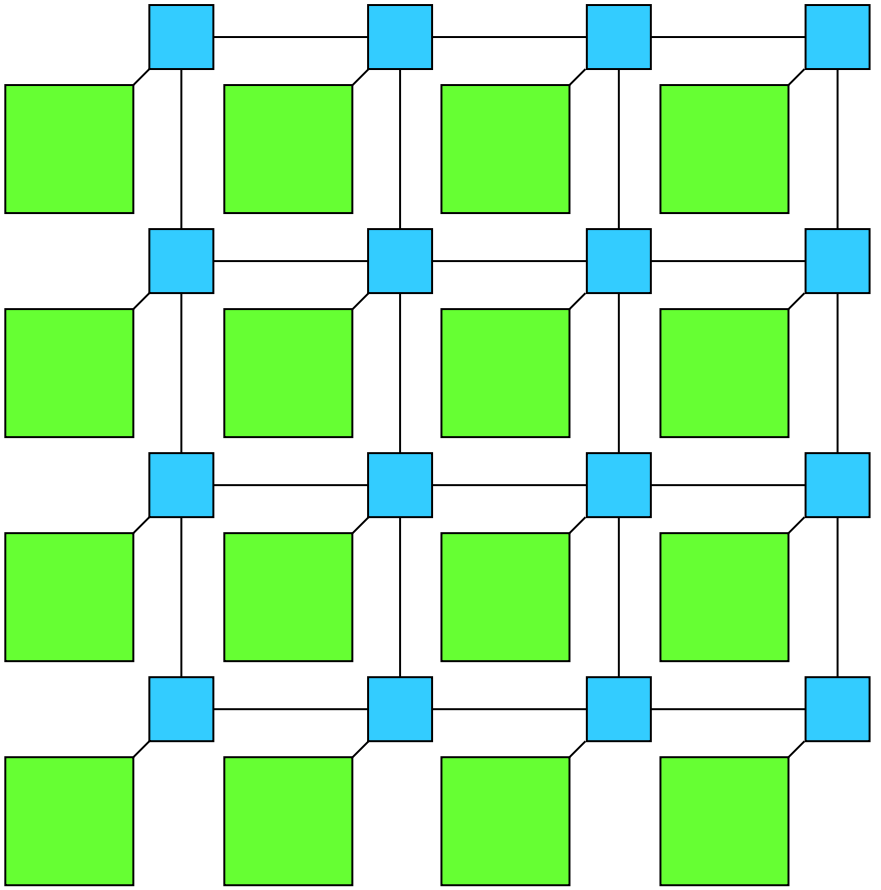
Routing Algorithms



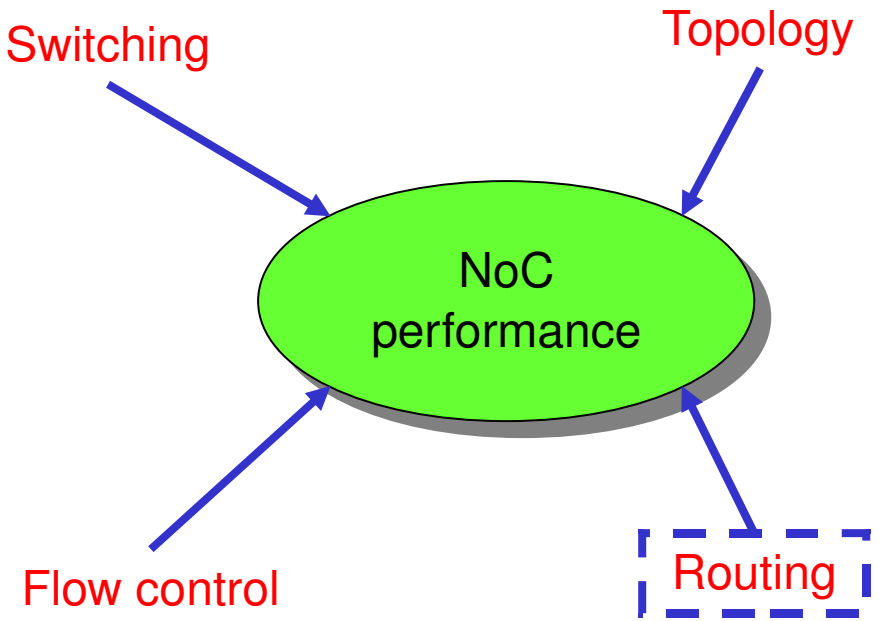
Routing Algorithms

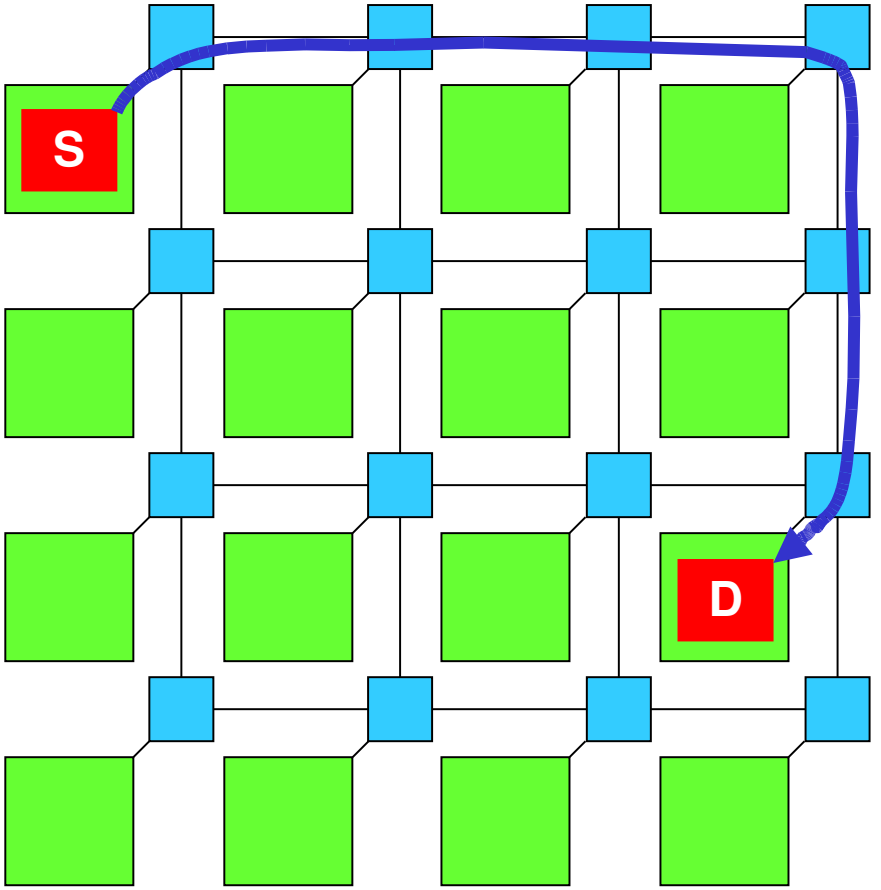




- Routing determines the path selected by a packet to reach its destination
  - ➔ Deterministic
  - ➔ Adaptive

Routing Algorithms





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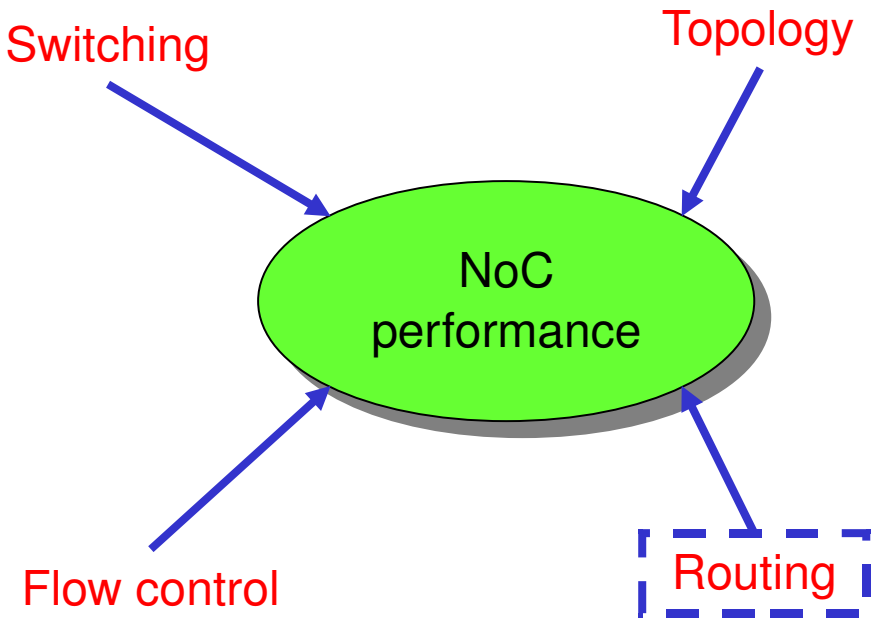
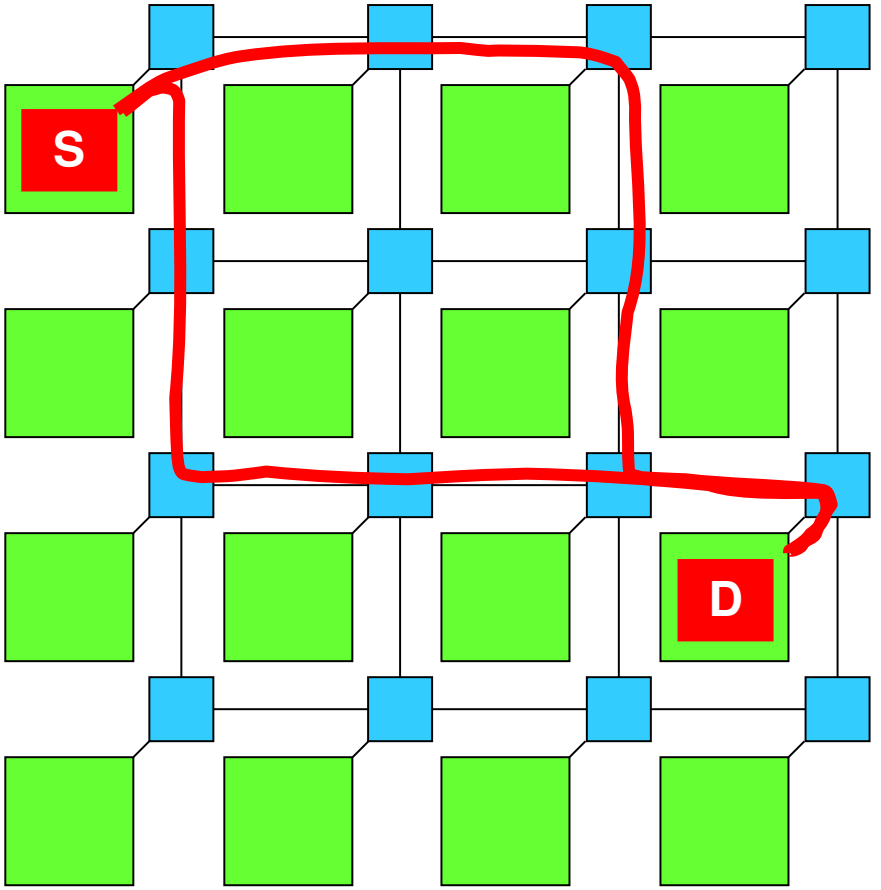
Routing Algorithms





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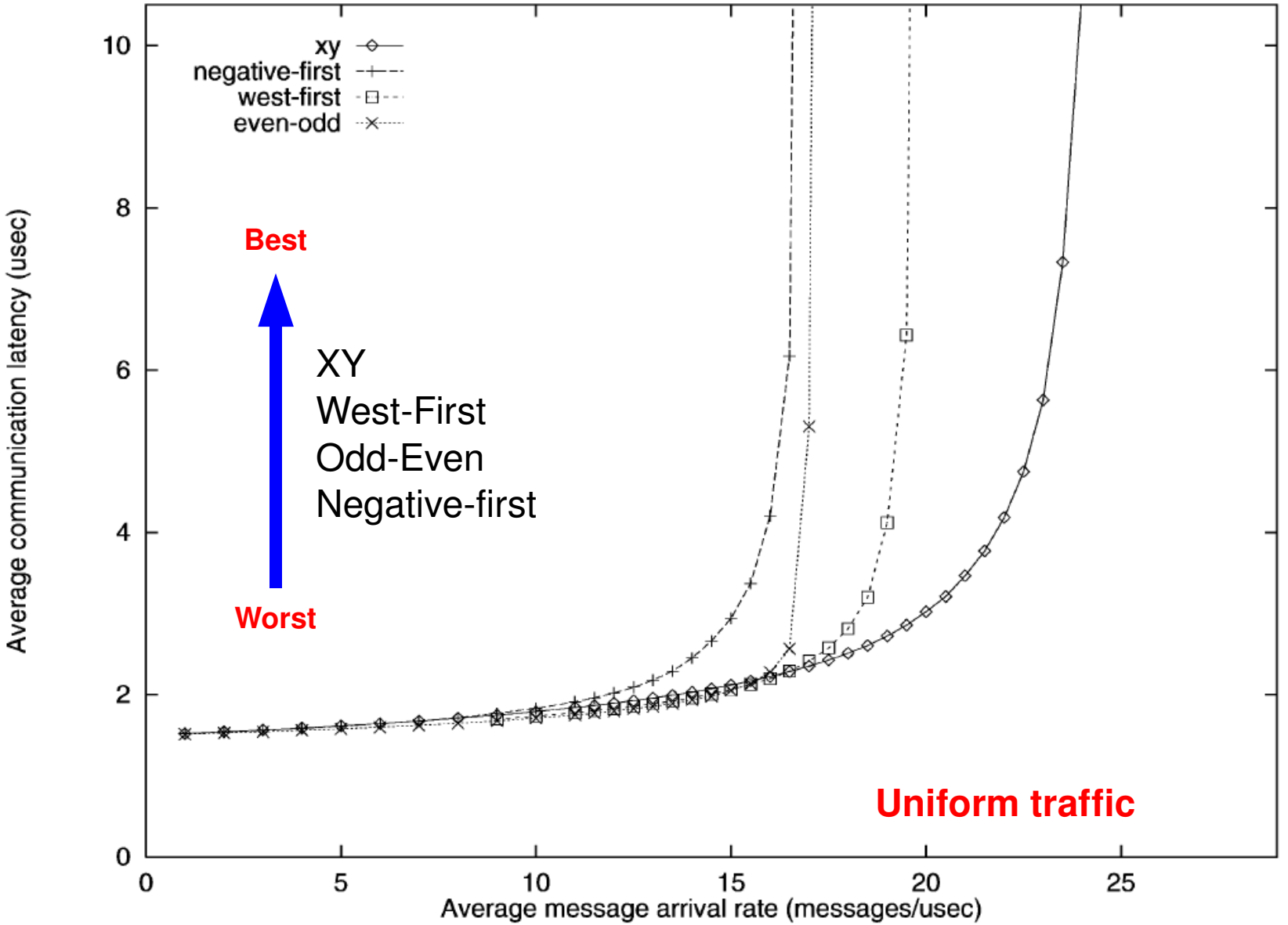
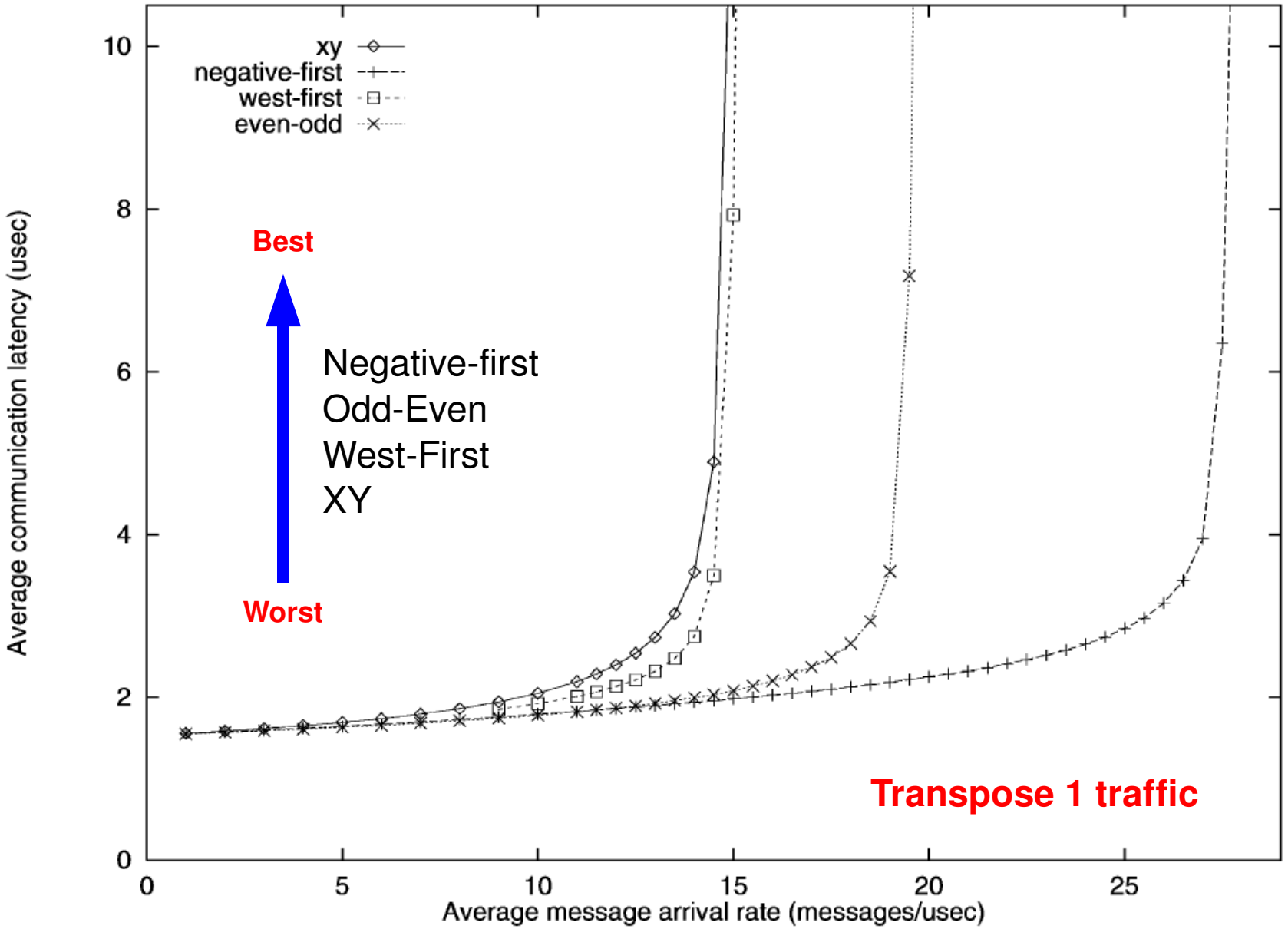
  - ➔ Deterministic
  - ➔ **Adaptive**

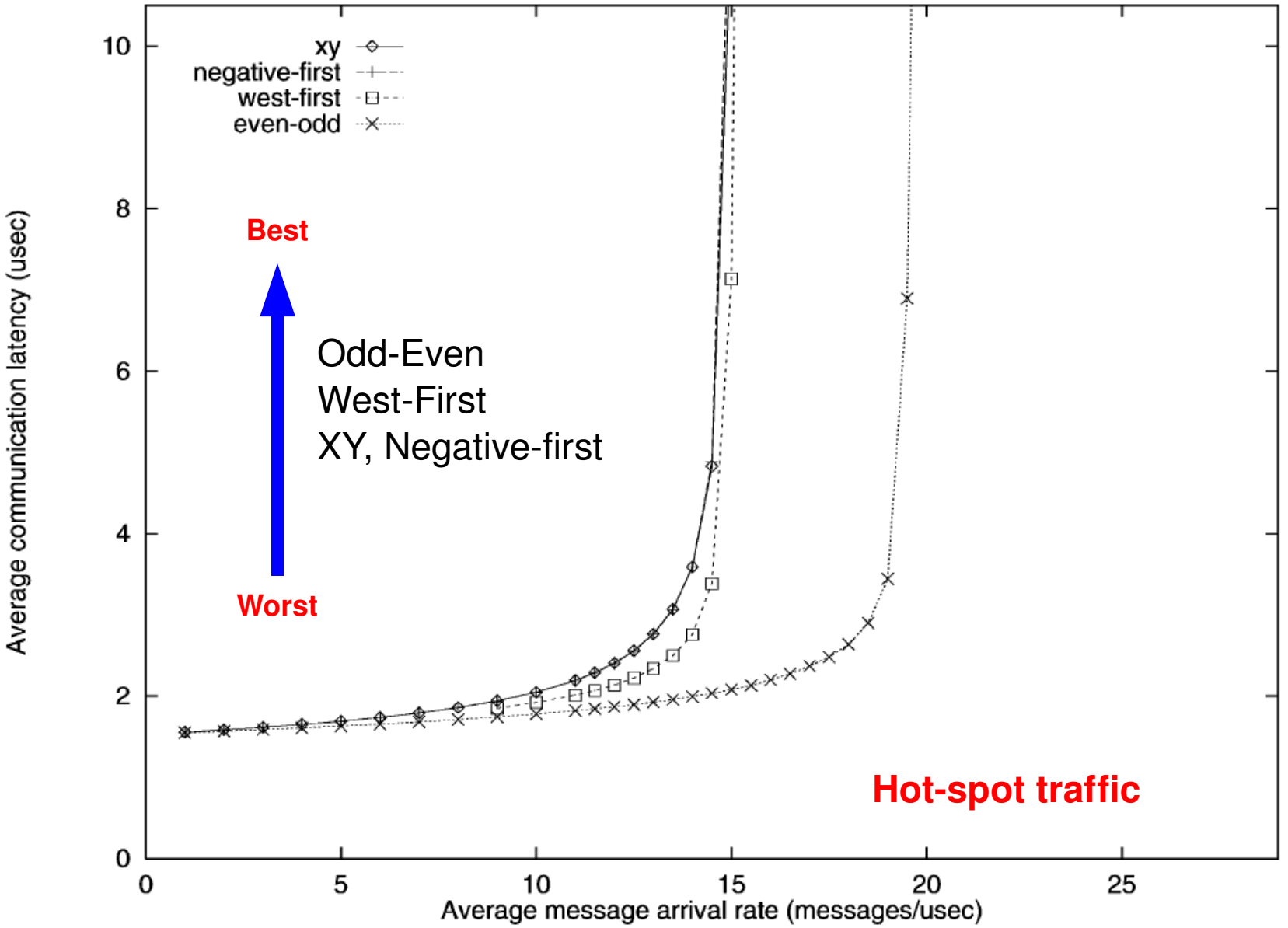
Performance of Routing Algorithms



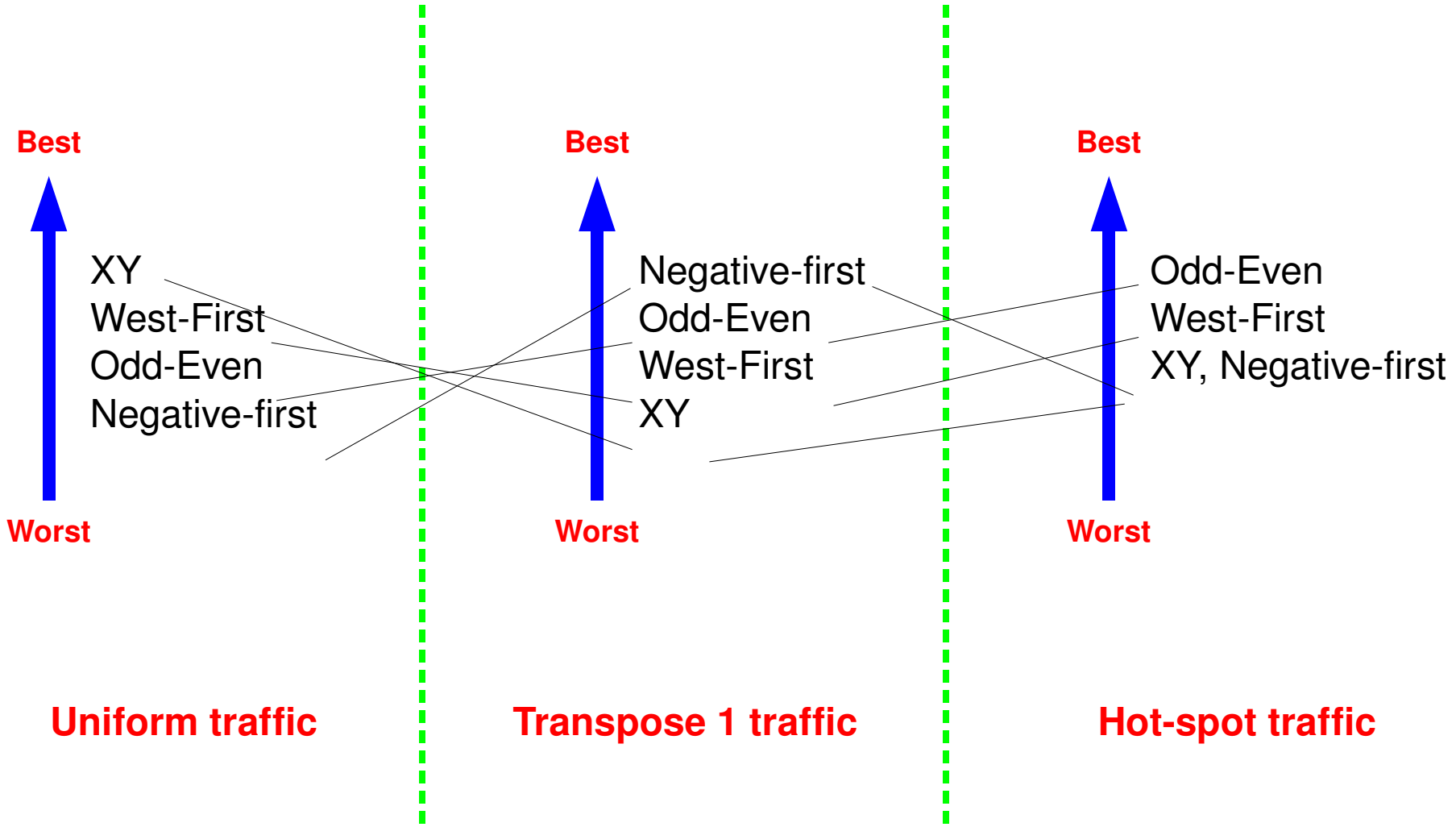
Performance of Routing Algorithms



Performance of Routing Algorithms

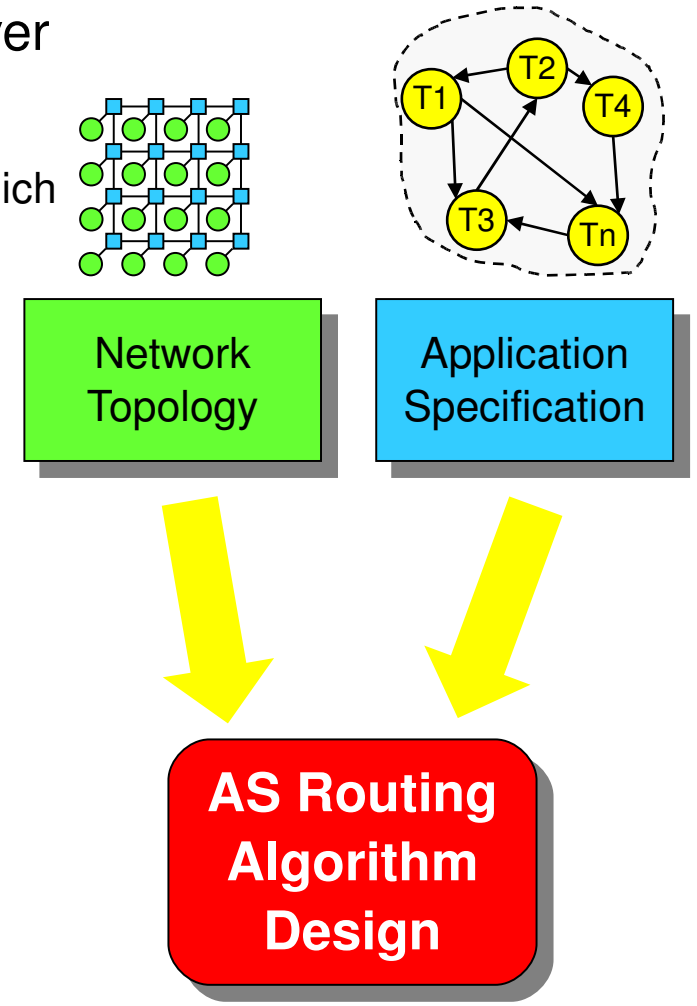


No Winner Routing Algorithm



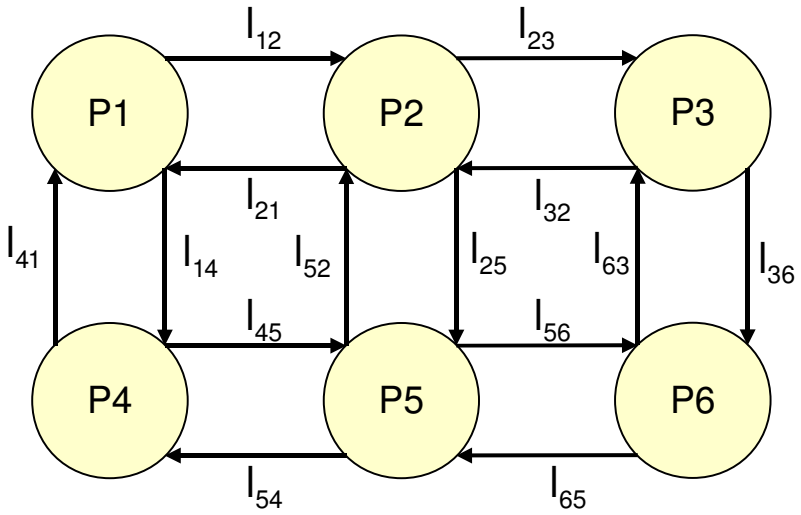
Application Specific Routing Algorithm

- Information about
  - ➔ Tasks which communicate and tasks which do never communicate
    - ✔ After task mapping ➔ Information about network nodes which communicate
  - ➔ Cuncurrent/non cuncurrent communications
  - ➔ Communications bandwidth requirements
- Many opportunities
  - ➔ Improving performance (e.g., maximize routing adaptivity)
  - ➔ Simplify the estimation/control of congestion
  - ➔ Design more effective selection policies

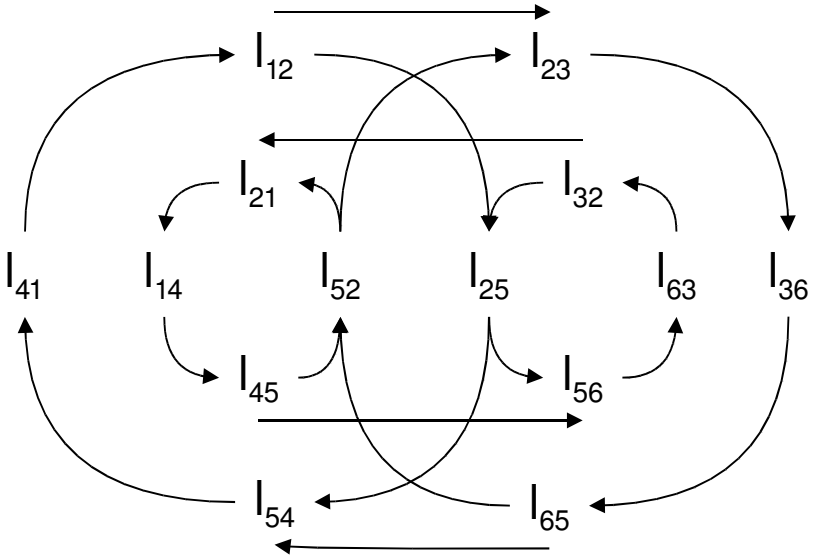


APSRA Example

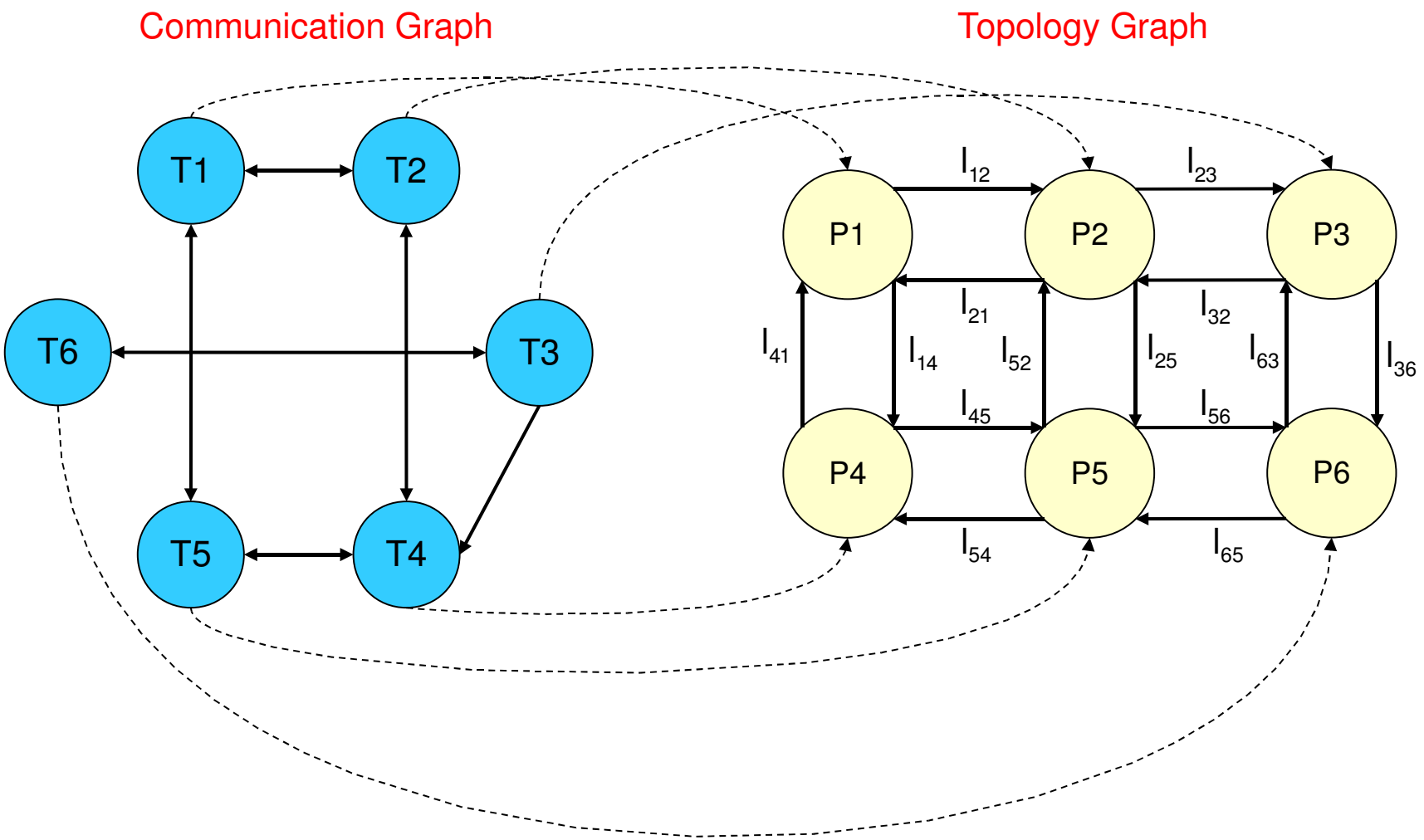
Topology Graph



Channel Dependency Graph



APSRA Example (cnt'd)



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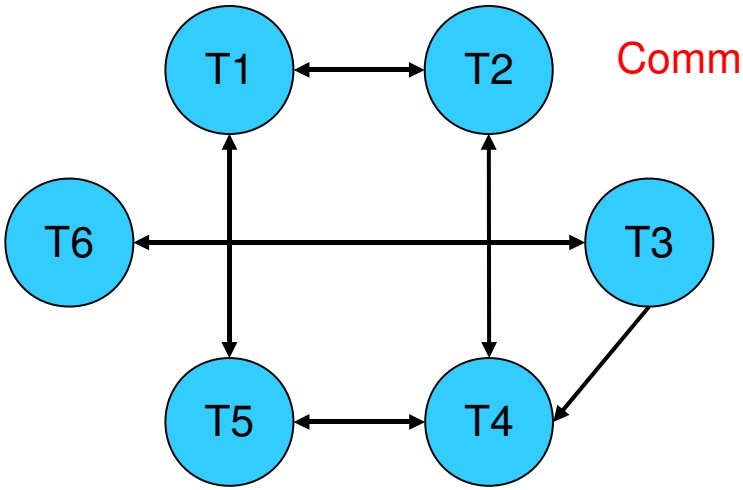
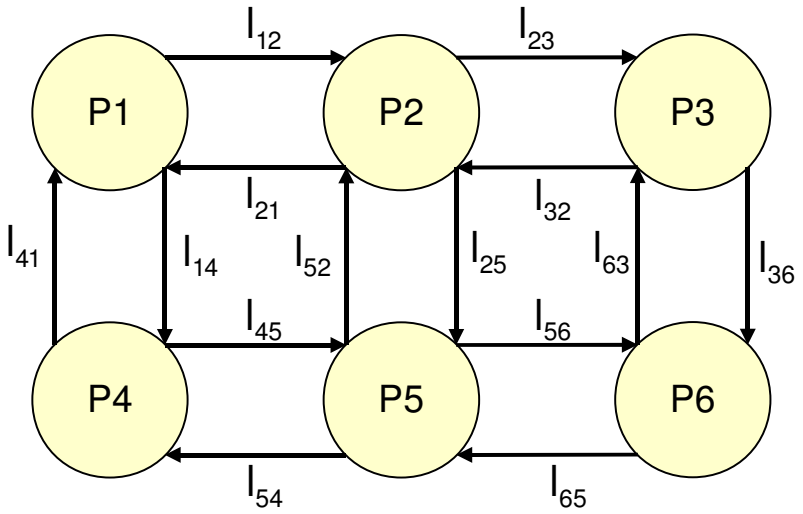
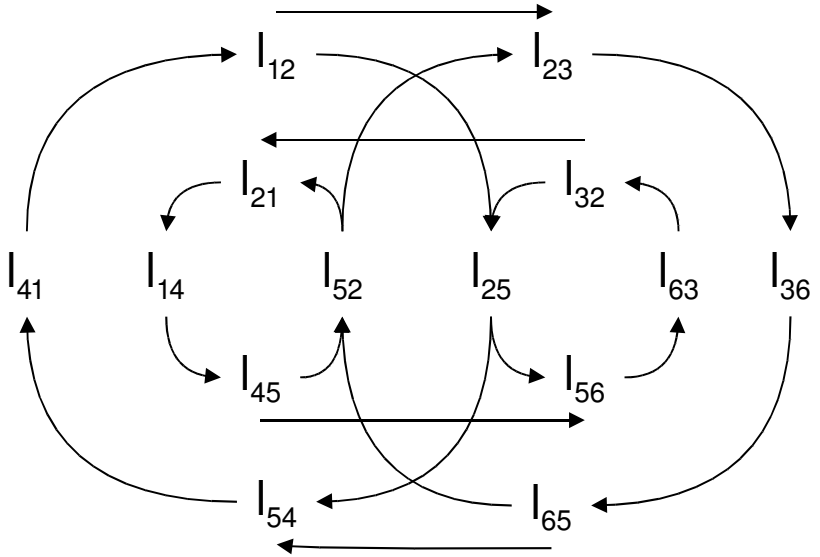


Communication Graph

Topology Graph





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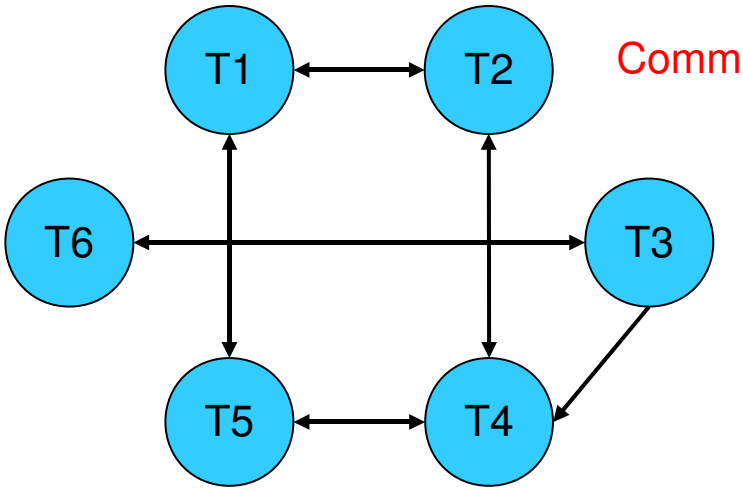
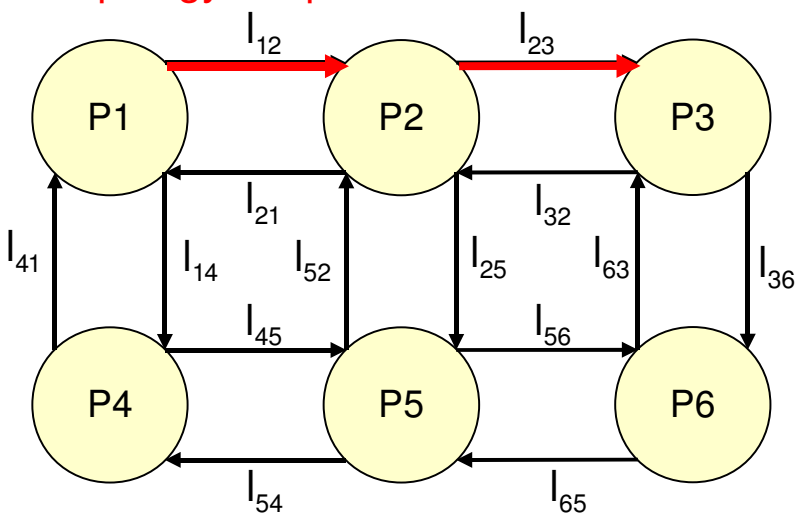
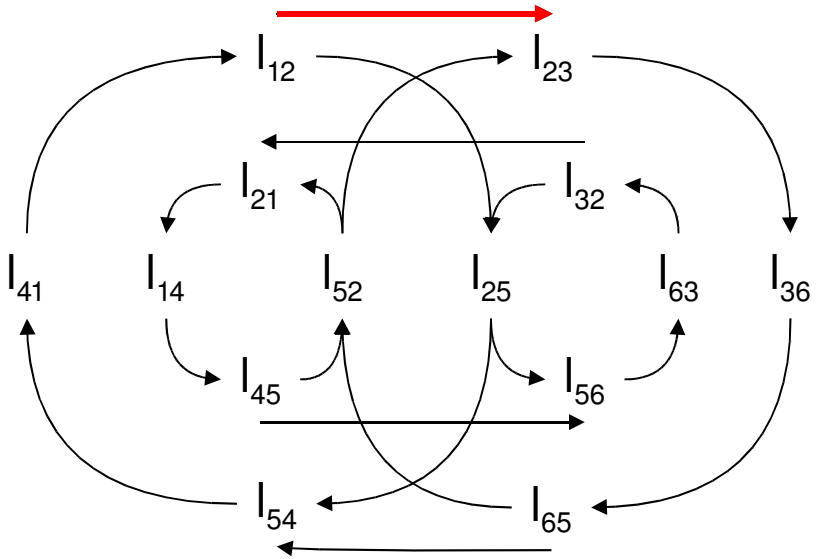


Communication Graph

Topology Graph





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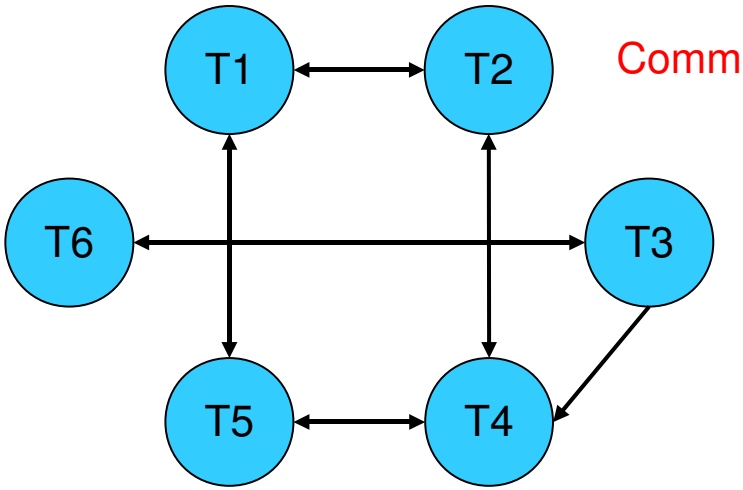
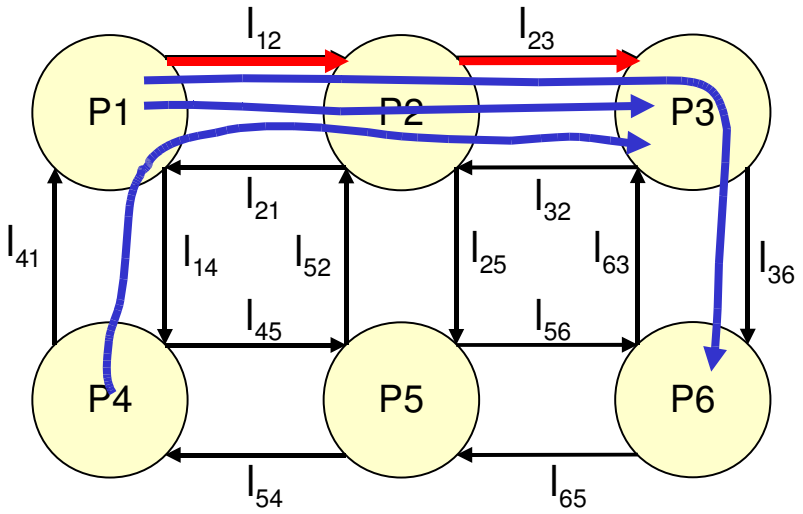
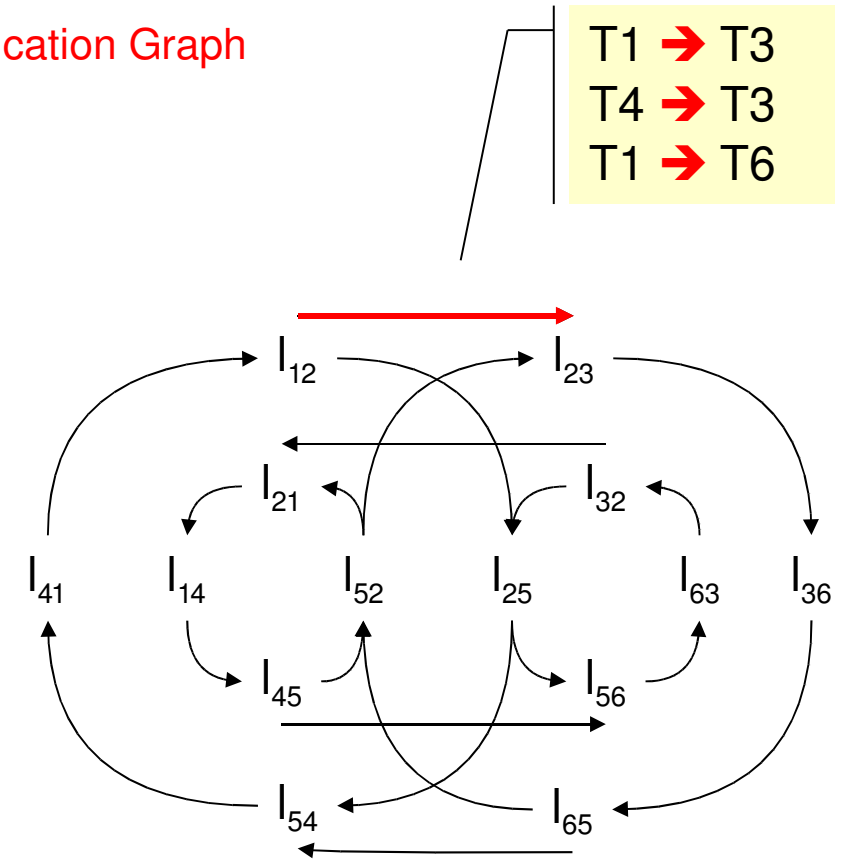


Communication Graph

T1 ➔ T3
T4 ➔ T3
T1 ➔ T6

Topology Graph





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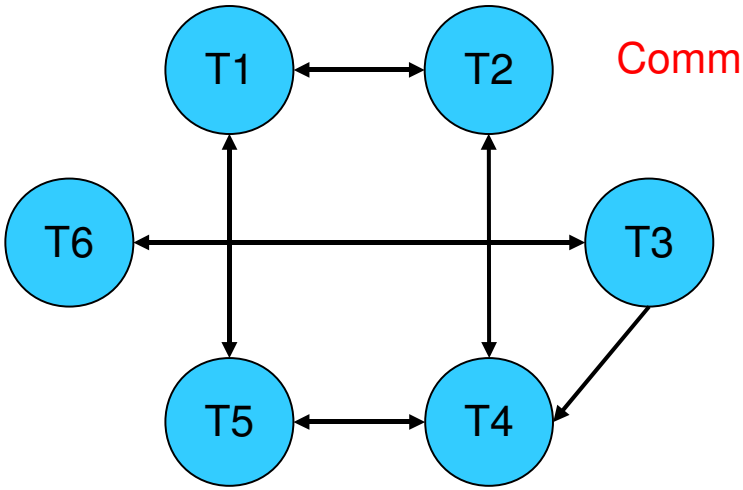

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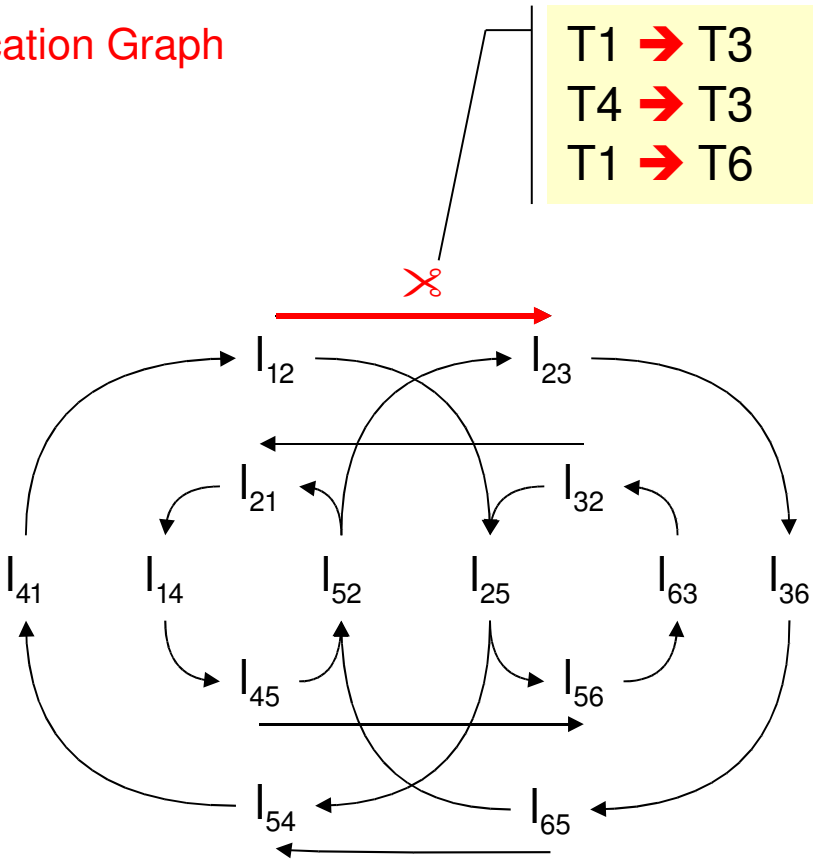
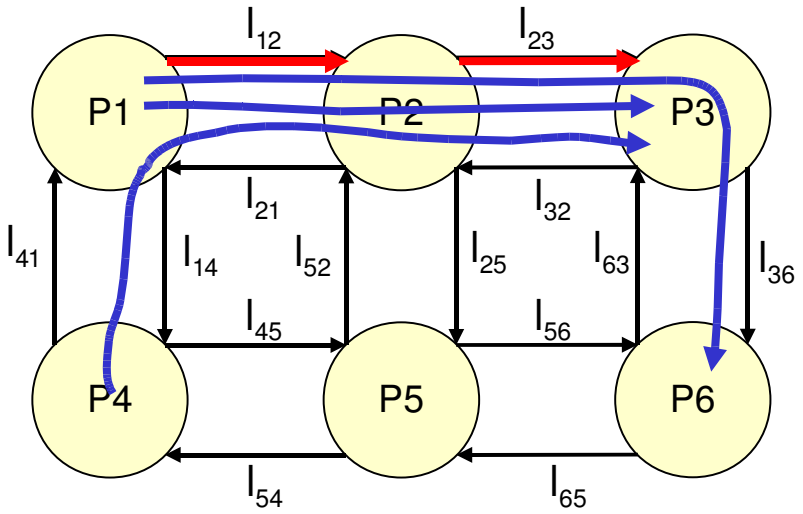


Channel Dependency Graph

Topology Graph



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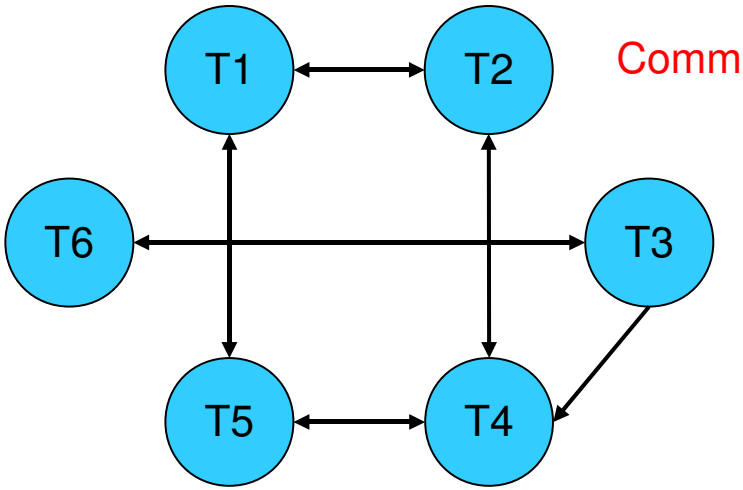

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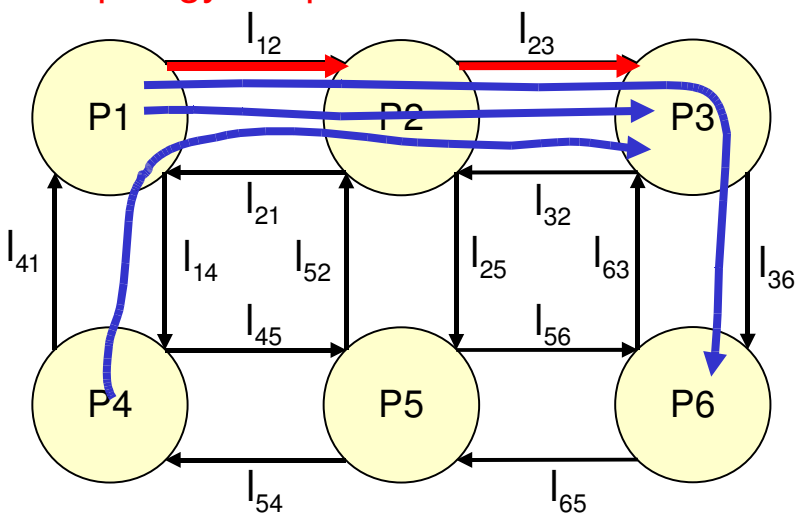

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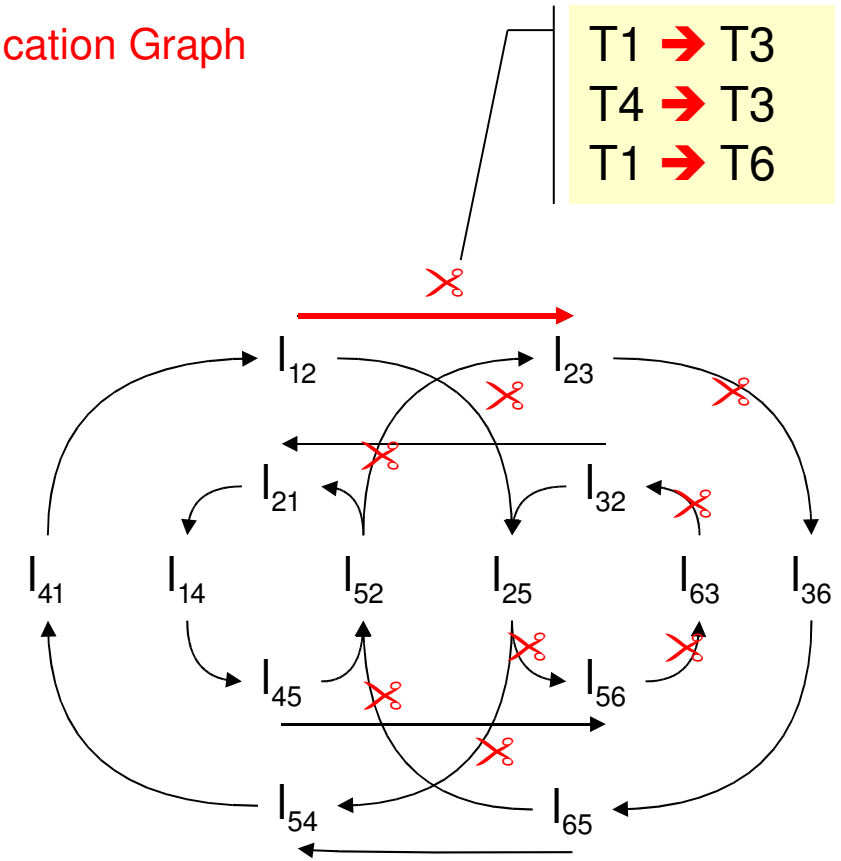

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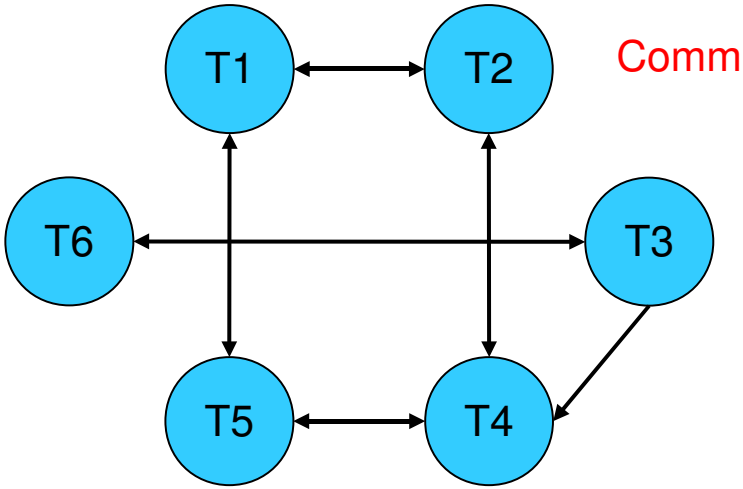
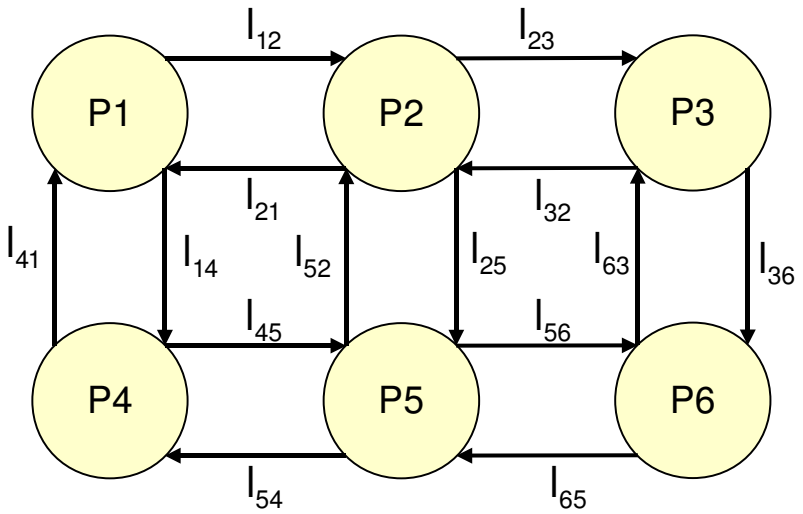
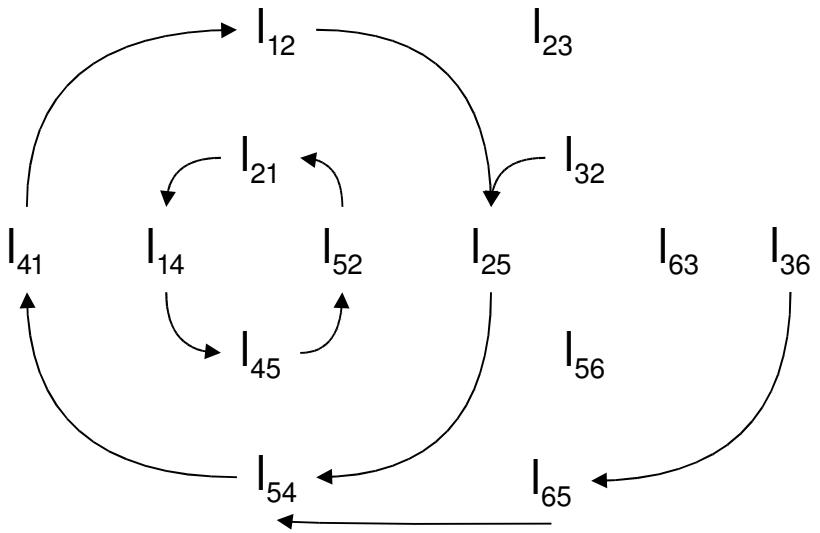


Communication Graph

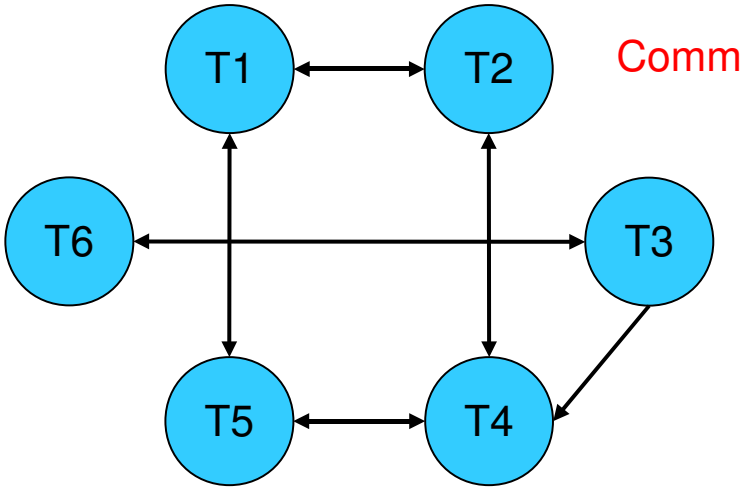
Topology Graph





Application Specific
Channel Dependency Graph

APSRA Example (cnt'd)



Communication Graph

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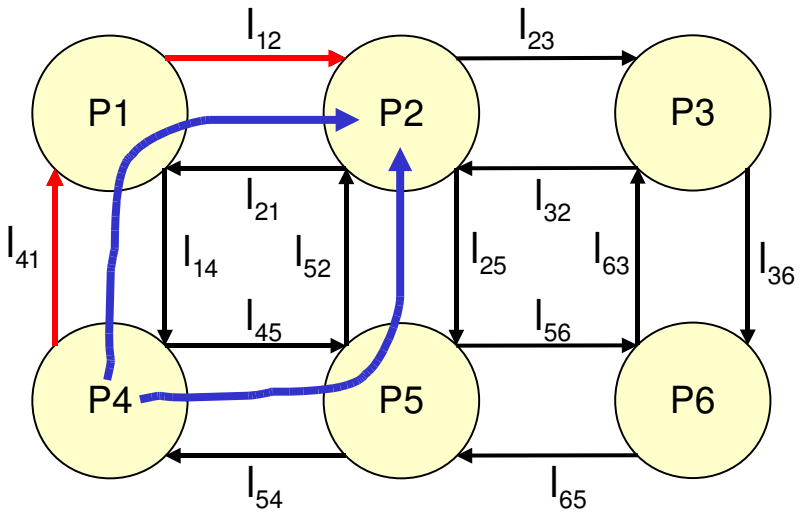

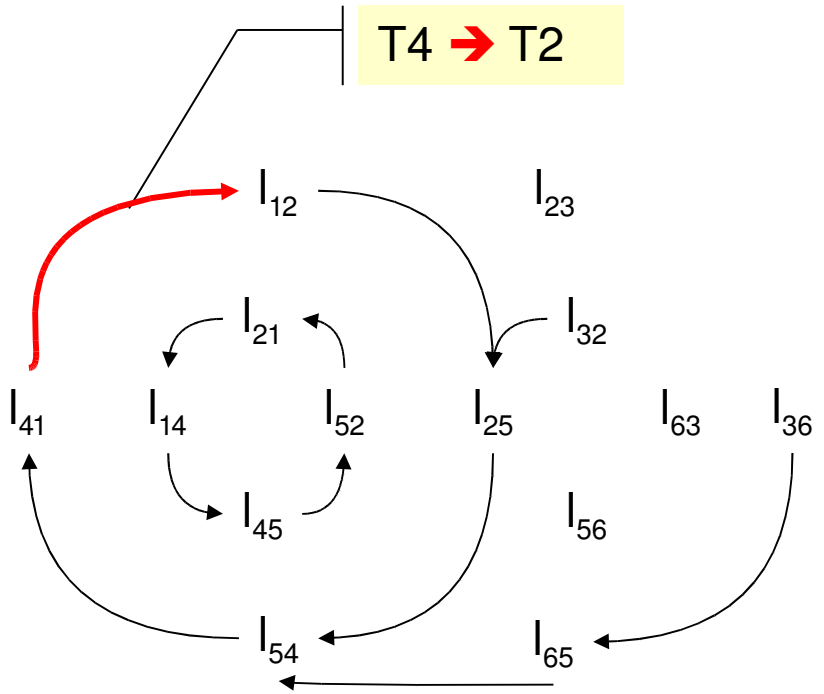

Application Specific
Channel Dependency Graph

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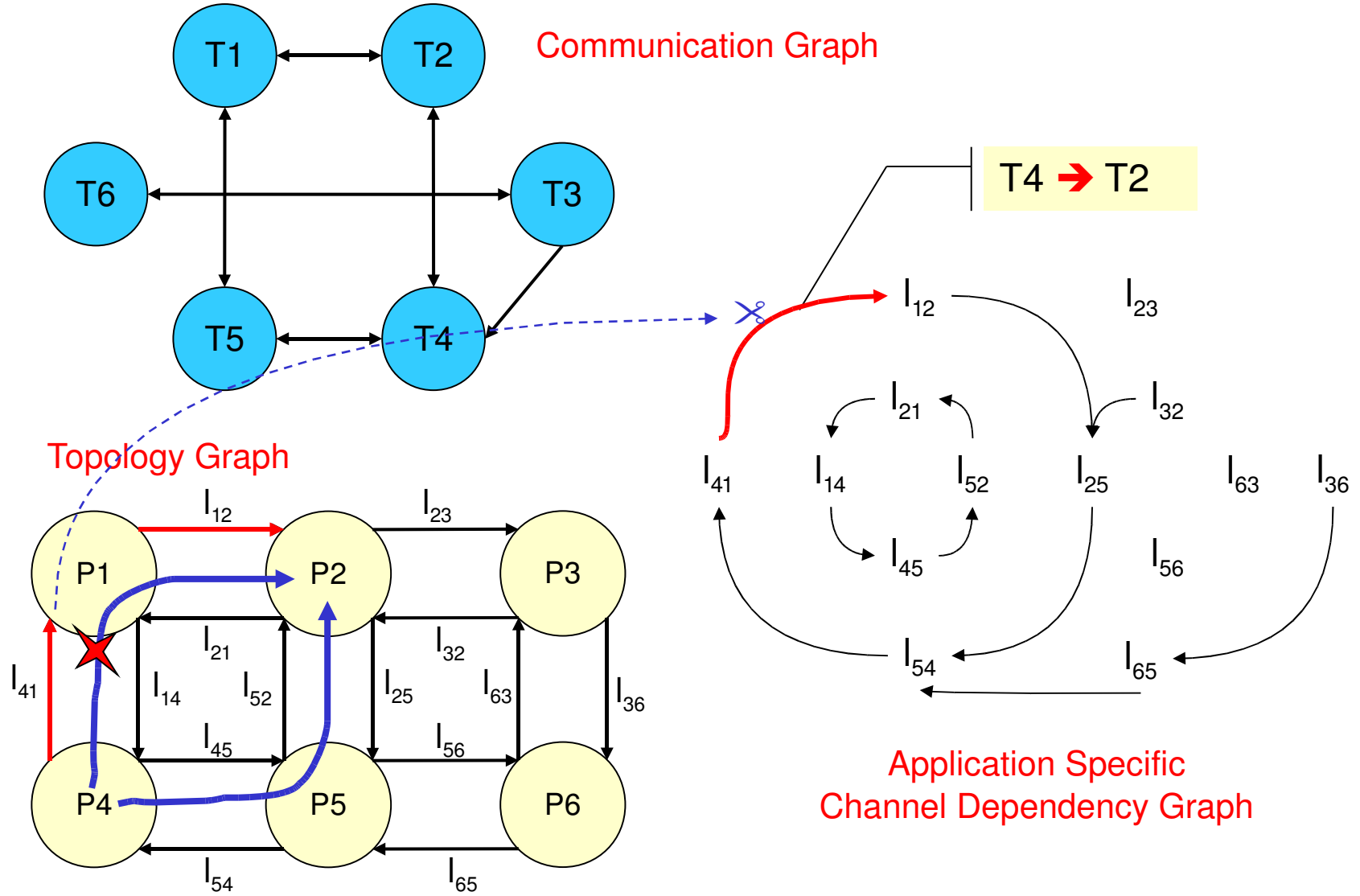
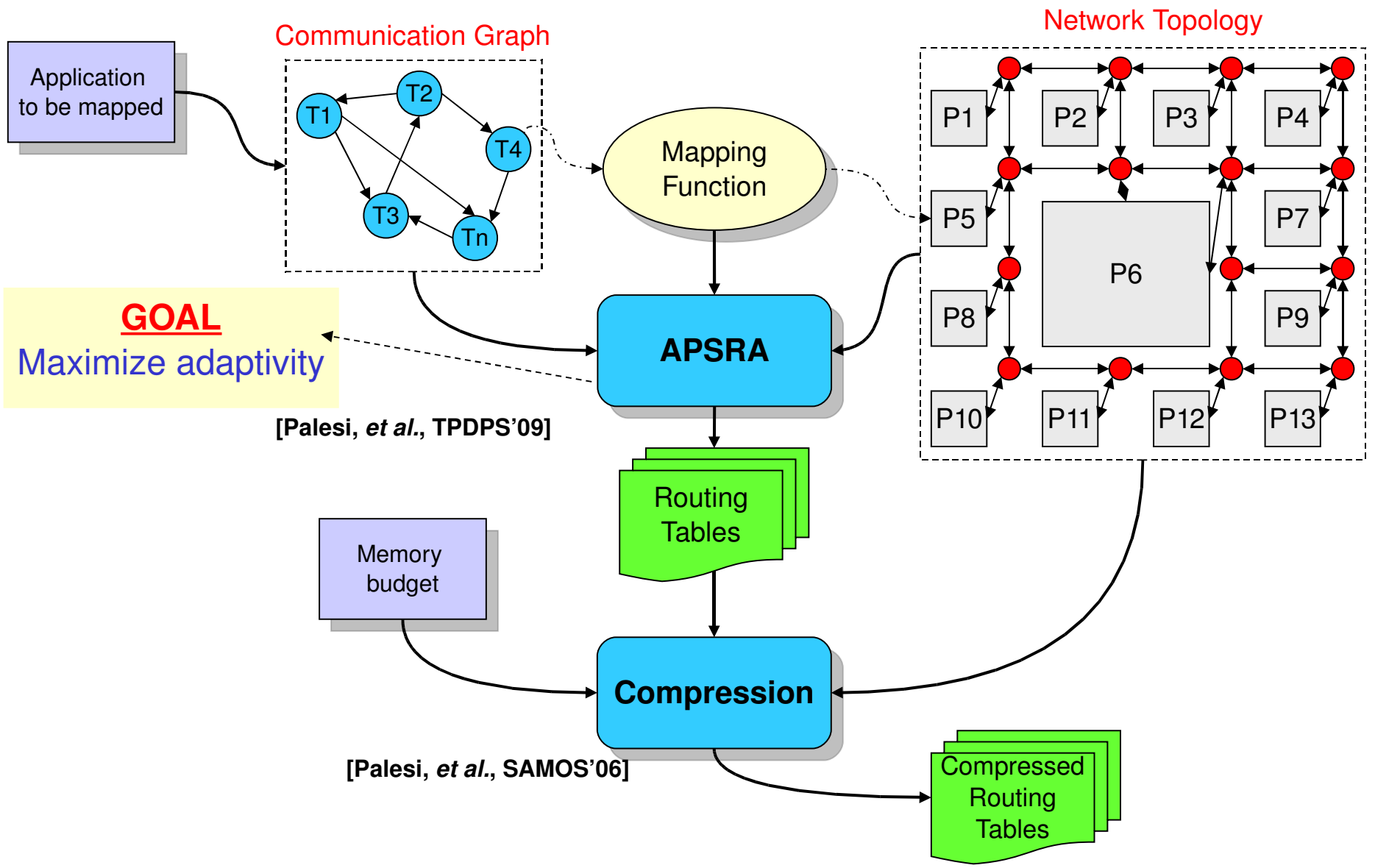
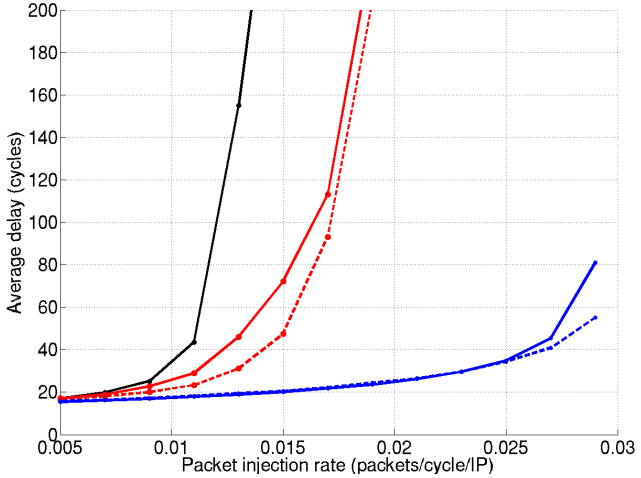


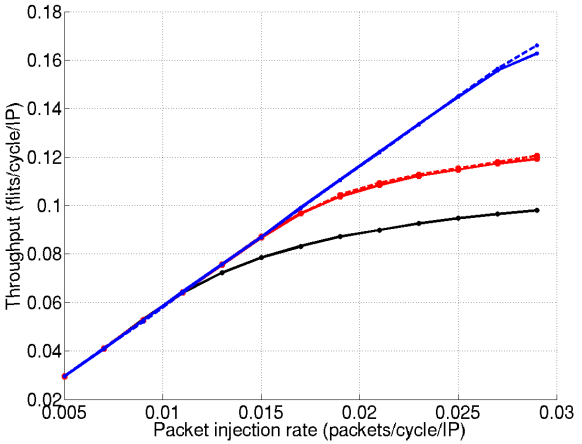
APSRA Methodology



APSRA Performance (1/2)

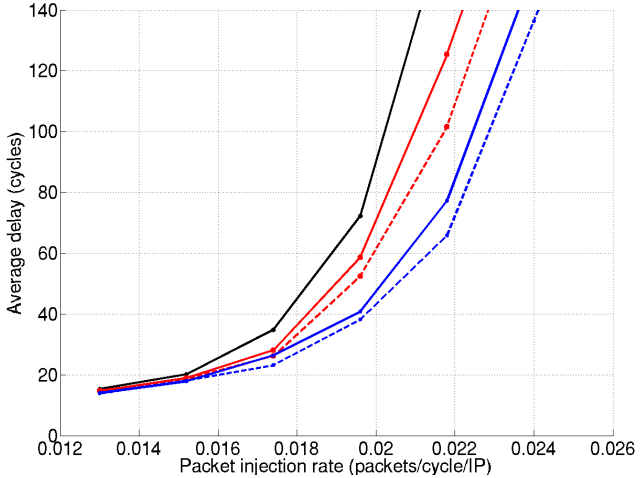
Transpose 1

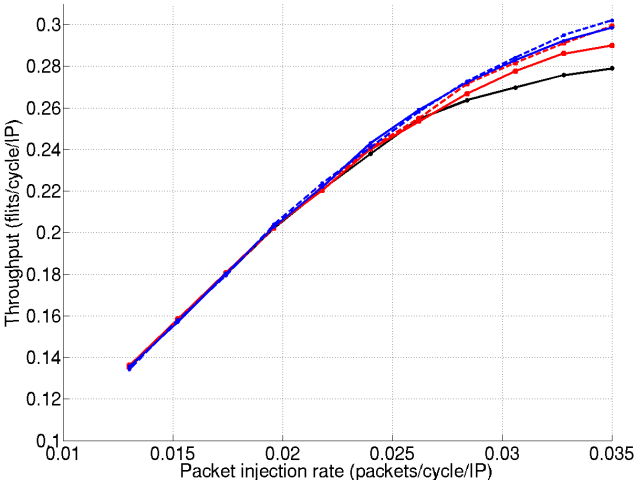


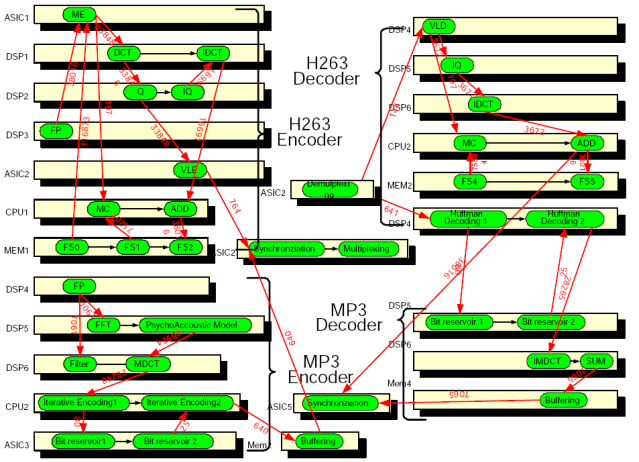


XY
Odd-Even (sel=random)
APSRA (sel=random)
Odd-Even (sel=buffer level)
APSRA (sel=buffer level)

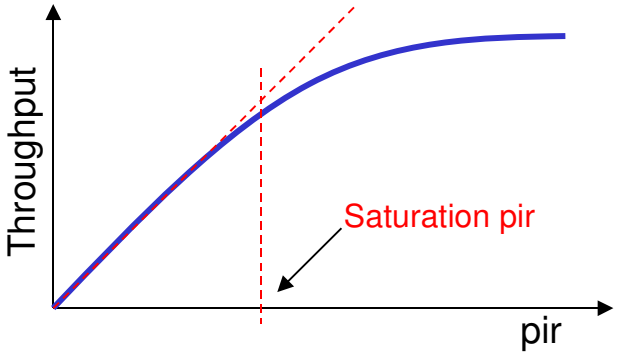
MMS







APSRA Performance (2/2)

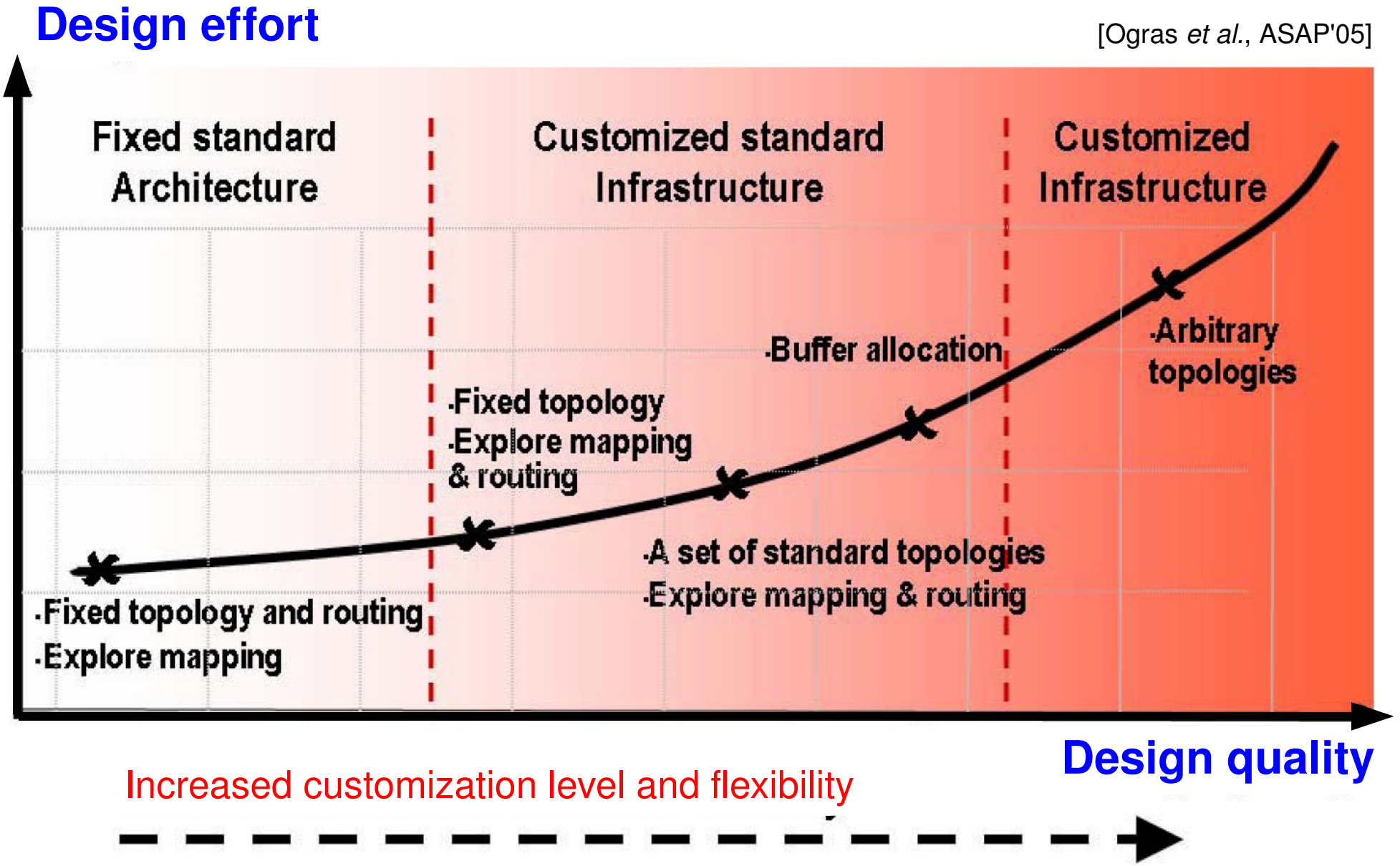


Traffic scenario	Max. pir (packets/cycle/IP) XY	OE	APSRA	APSRA improvement vs. XY	vs. OE
Random	0.012	0.011	0.012	0.0%	14.3%
Locality	0.019	0.020	0.021	10.5%	5.0%
Transpose 1	0.011	0.015	0.027	145.5%	80.0%
Transpose 2	0.011	0.016	0.027	145.5%	68.8%
Hotspot-4c	0.003	0.004	0.004	13.6%	7.1%
Hotspot-4tr	0.003	0.003	0.004	29.6%	12.9%
Hotspot-8r	0.004	0.006	0.007	71.8%	13.6%
Mms	0.017	0.017	0.020	12.6%	12.6%
Average improvement				***53.6%***	***26.8%***

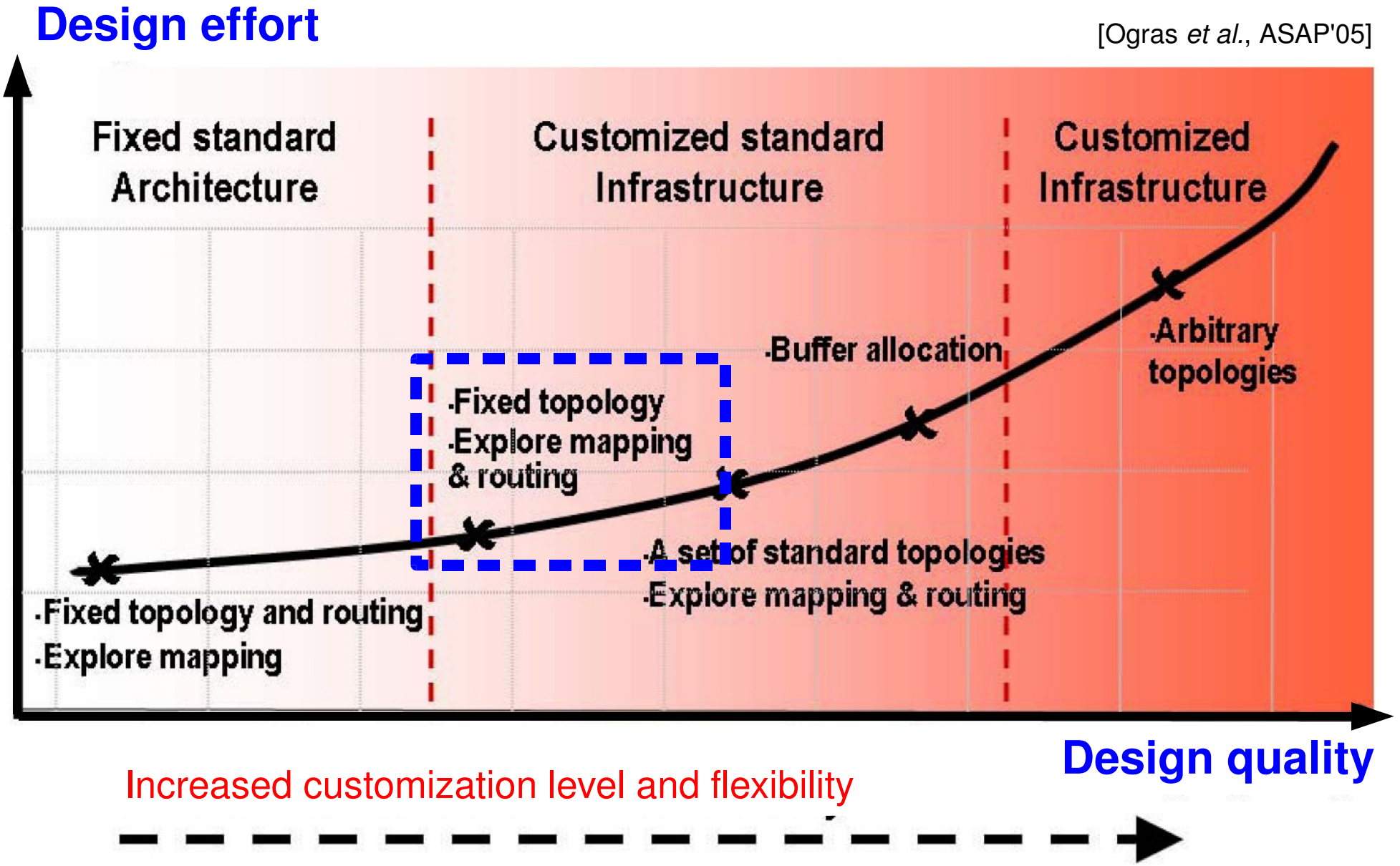
Outline

- Application Specific Routing Algorithms ✓
- Concurrent Mapping and Routing
- Dealing with Manufacturing Defects
- Encoding Scheme for Low Power

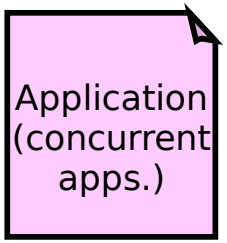
DSE for NoC Architectures

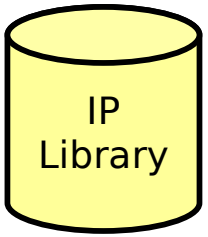


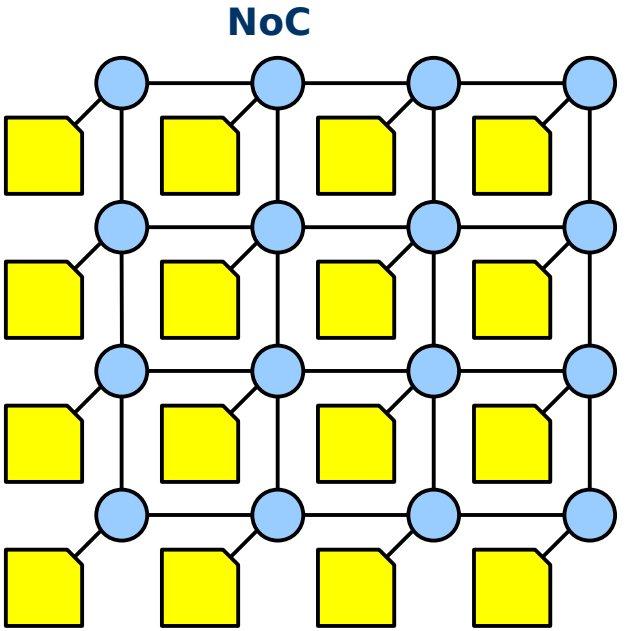
DSE for NoC Architectures



The Mapping Problem







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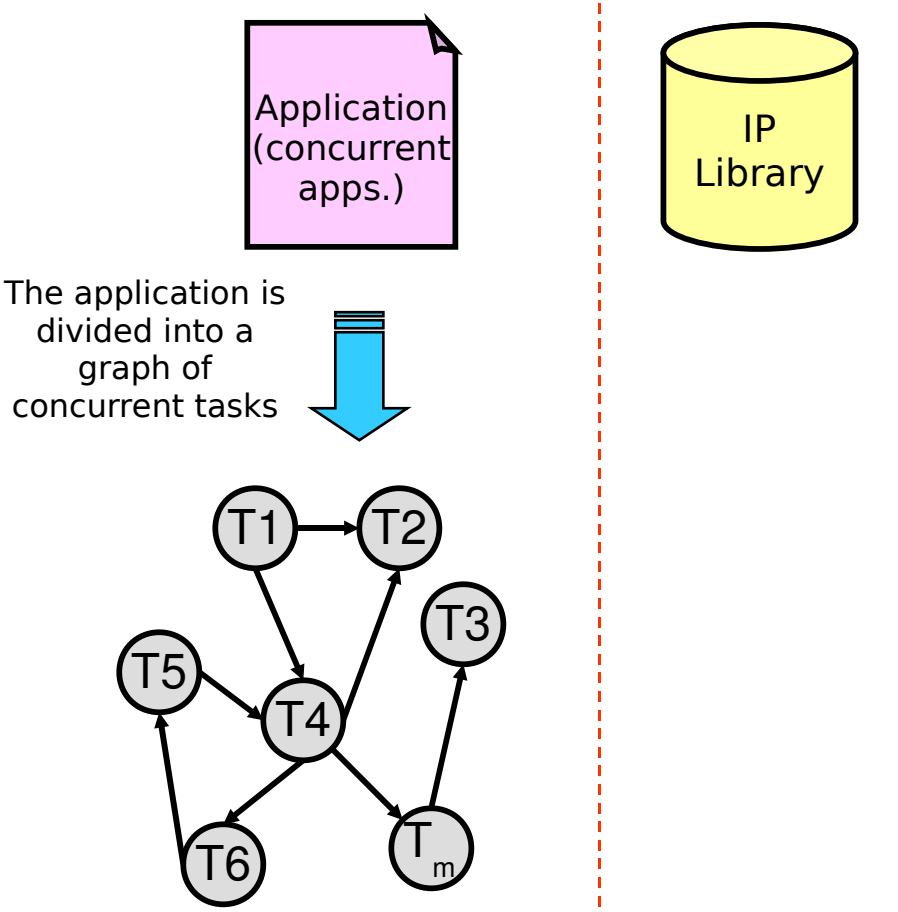

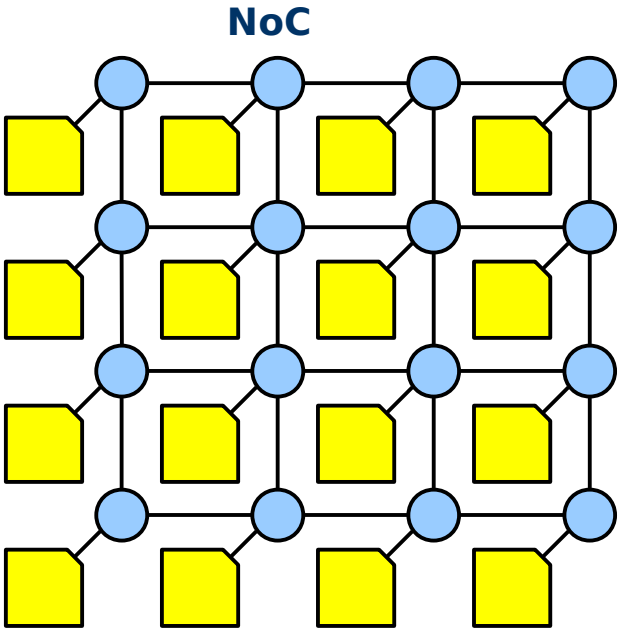

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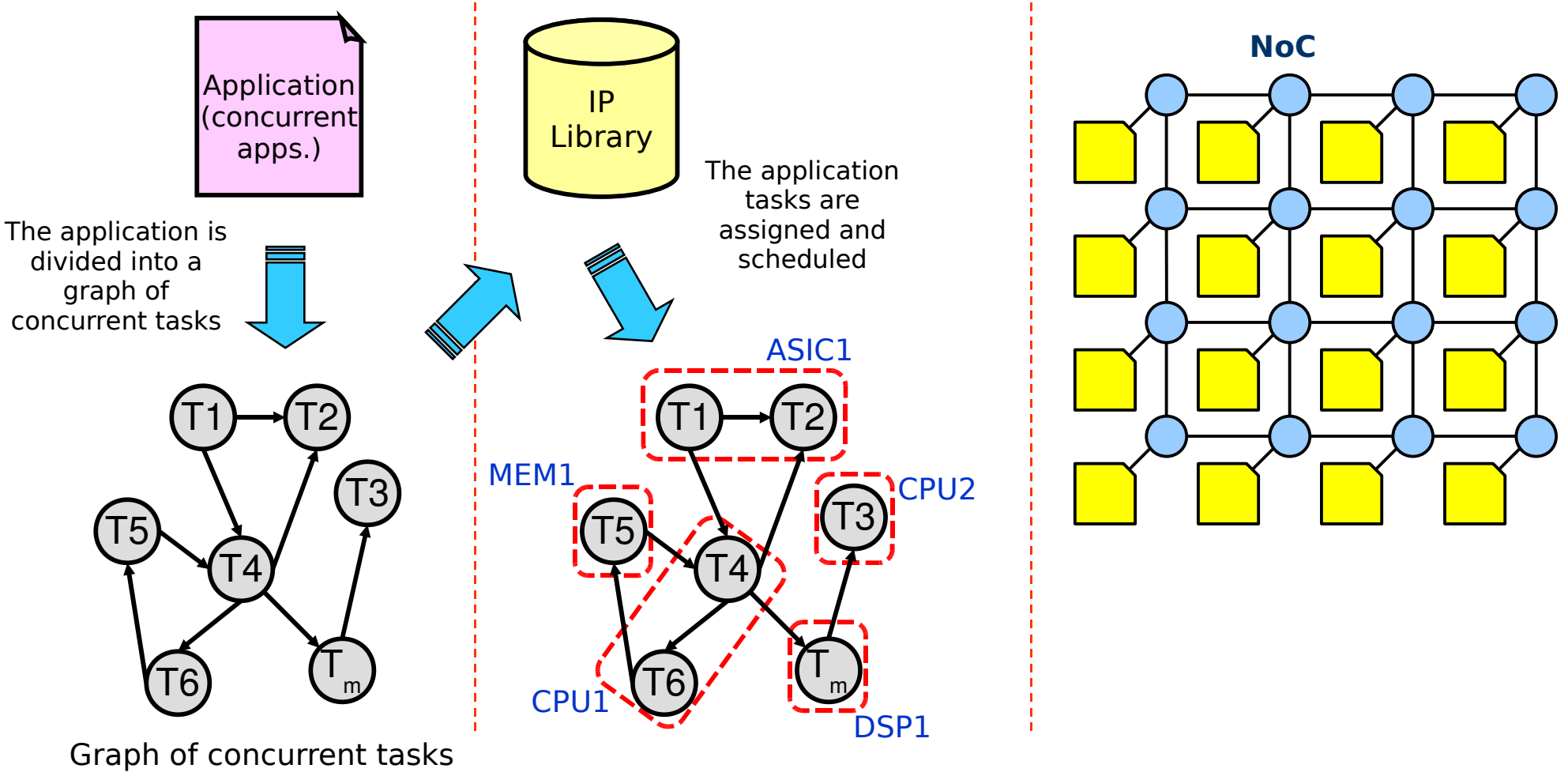

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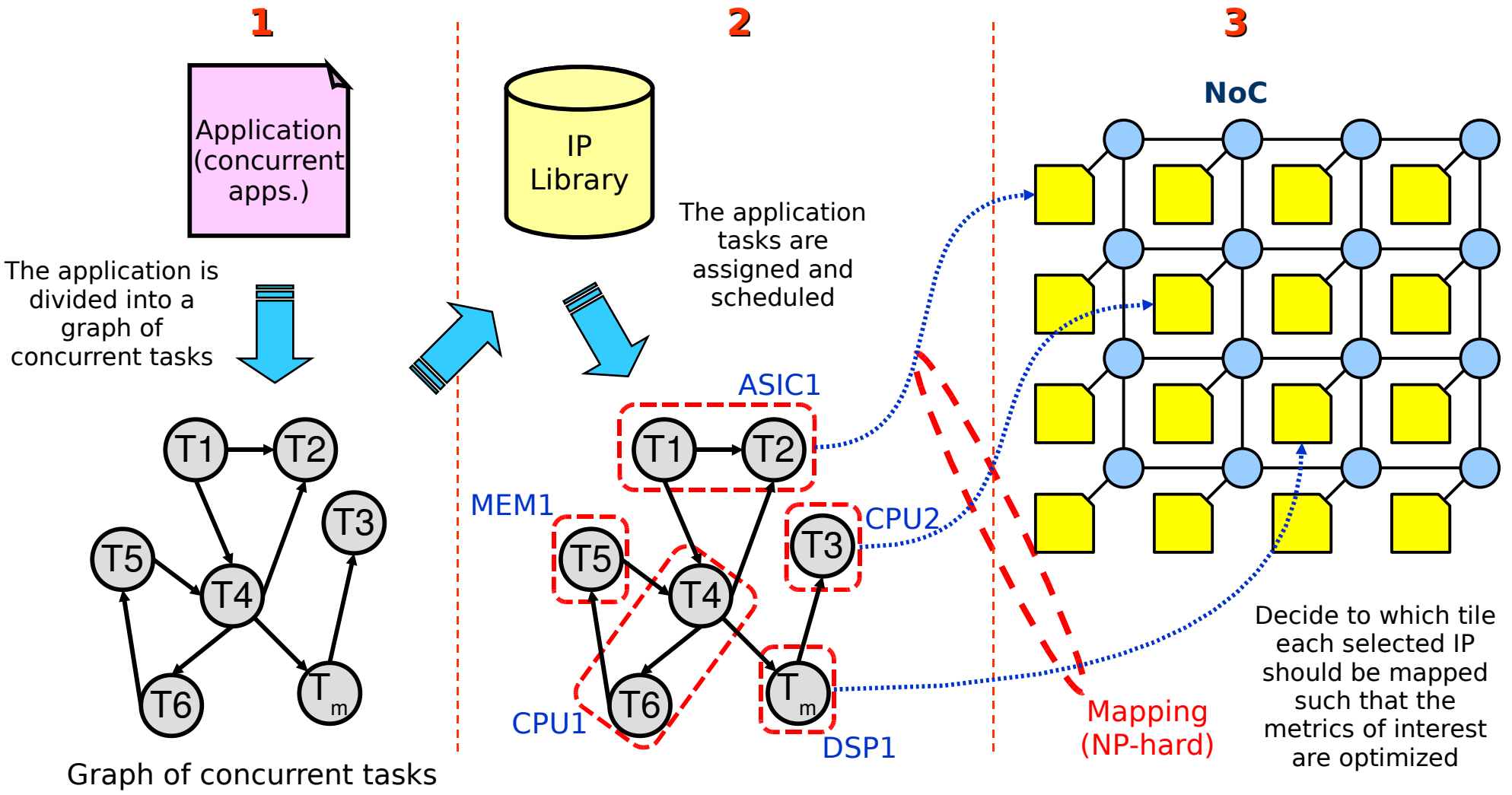
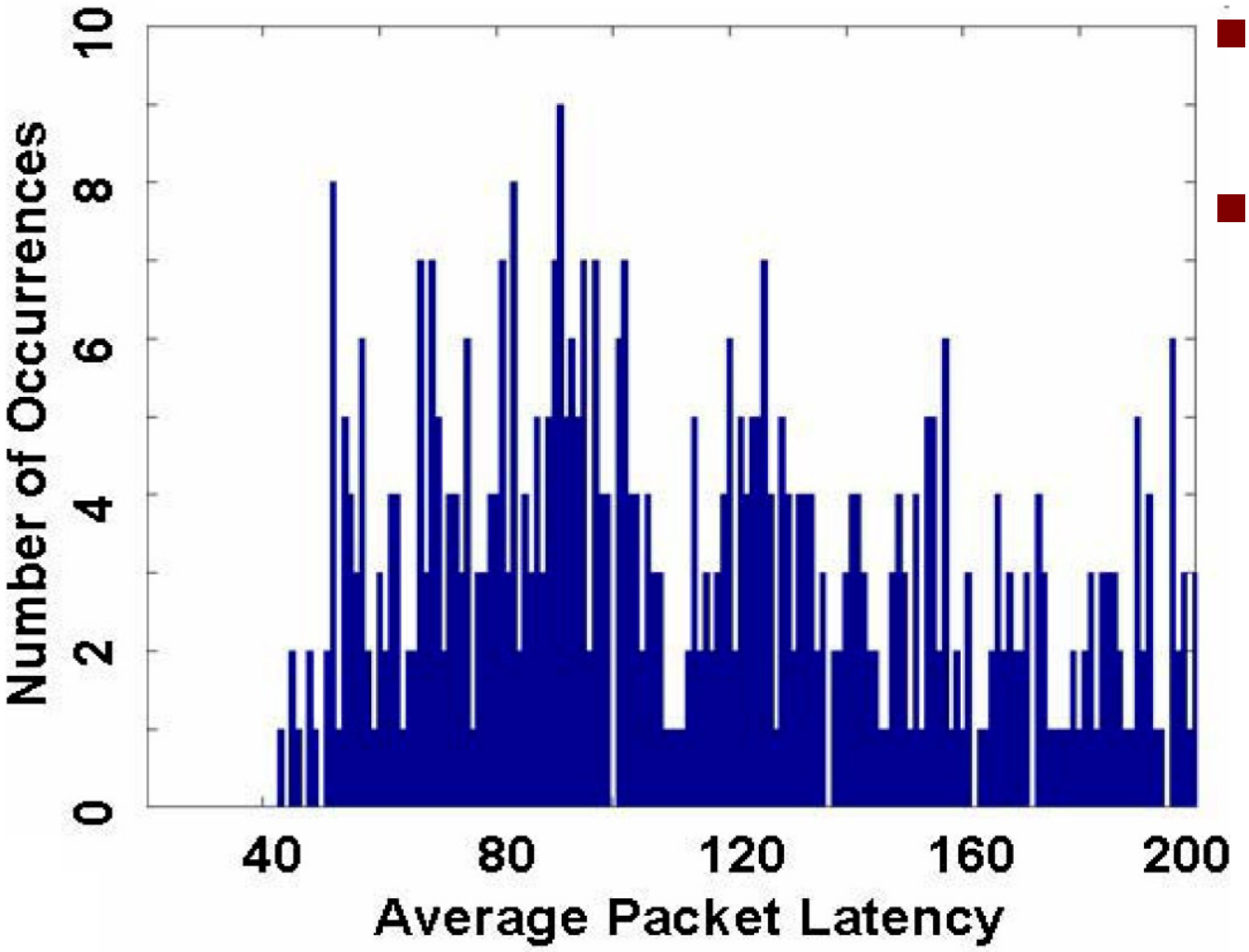


Impact of Mapping on Performance



- A/V multimedia system
  - ➔ Mapped on 16 IPs
- Average packet latency of 3000 random mappings
  - ➔ Results for the top 478 mappings. The
  - ➔ Remaining 2522 mappings have latency much higher than 200 clock cycles

Problem Formulation

- Given
  - ➔ An application (or a set of concurrent applications) already mapped and scheduled into a set of IPs
  - ➔ A network topology
- Find **the best mapping** and **the best routing function** which
  - ➔ Maximize Performance (Minimize the mapping coefficient)
  - ➔ Maximize fault tolerant characteristics (Maximize the *robustness index*)
- Such that
  - ➔ The aggregated communications assigned to any channel do not exceed its capacity

Robustness Index

- Is an extension of the concept of *path diversity*

Robustness Index

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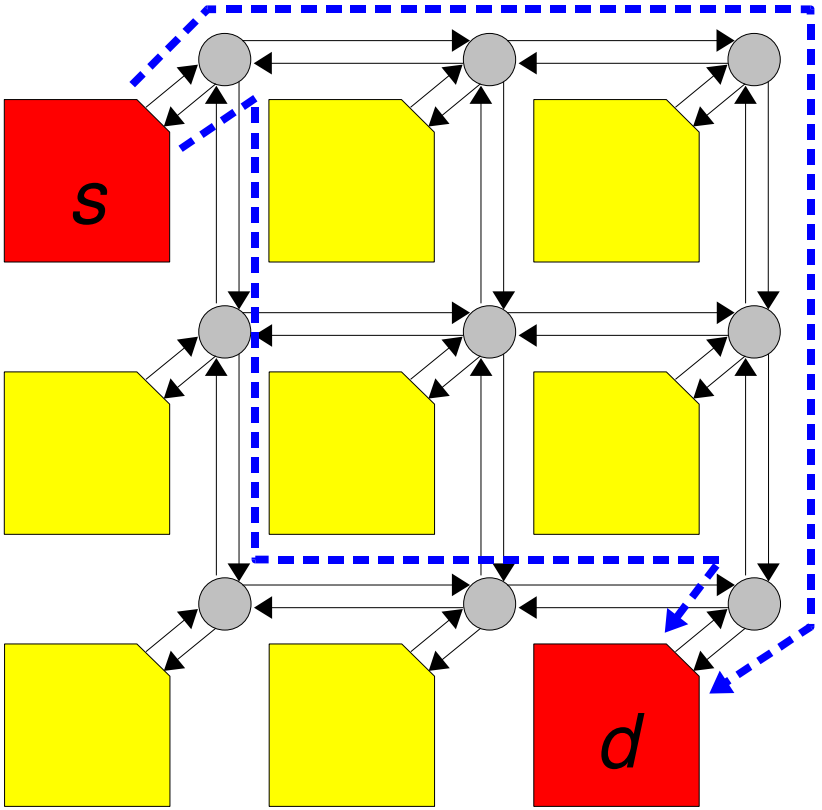
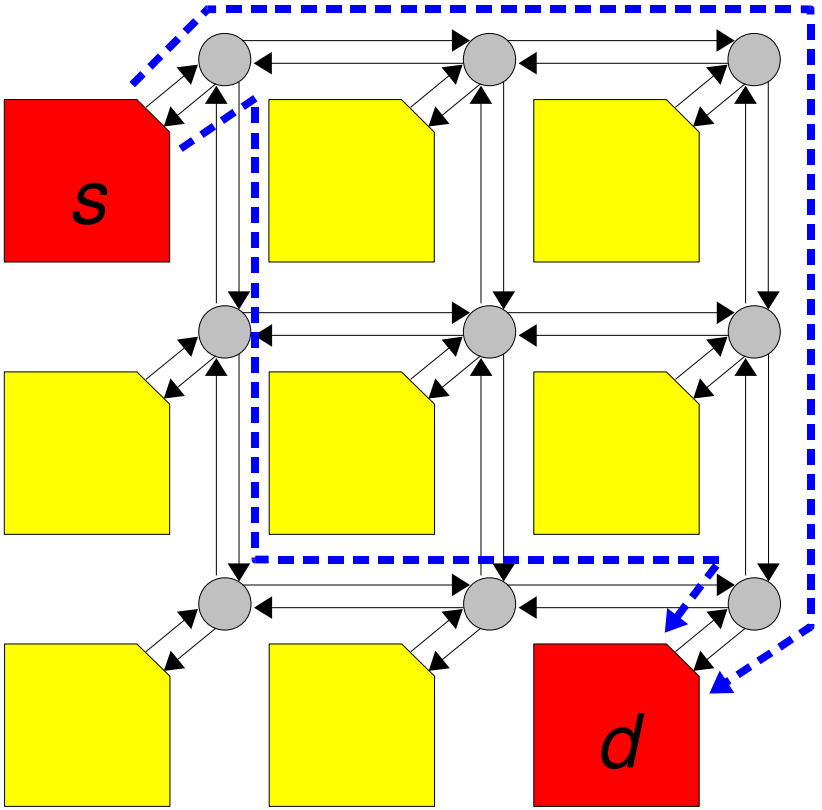


A single link fault does not compromise the communication from *s* to *d*

Robustness Index

- Is an extension of the concept of *path diversity*



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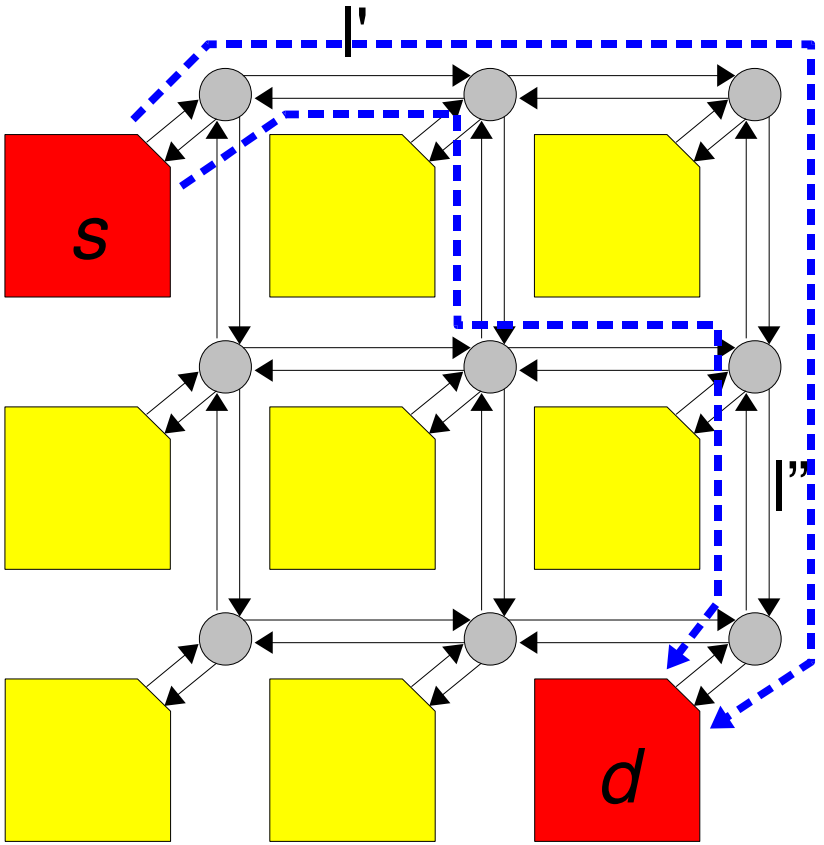
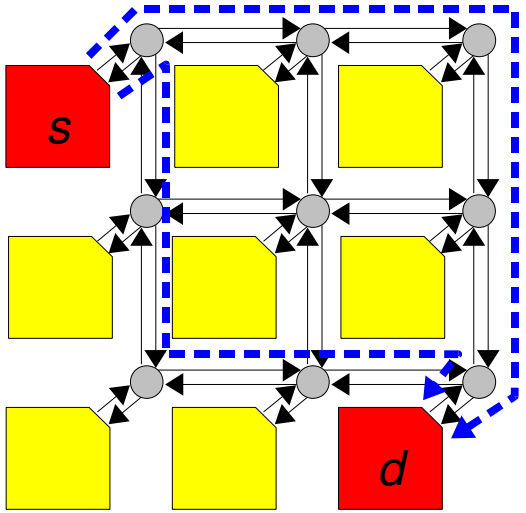


A single link fault in either l' or l” makes it impossible the communication from *s* to *d*

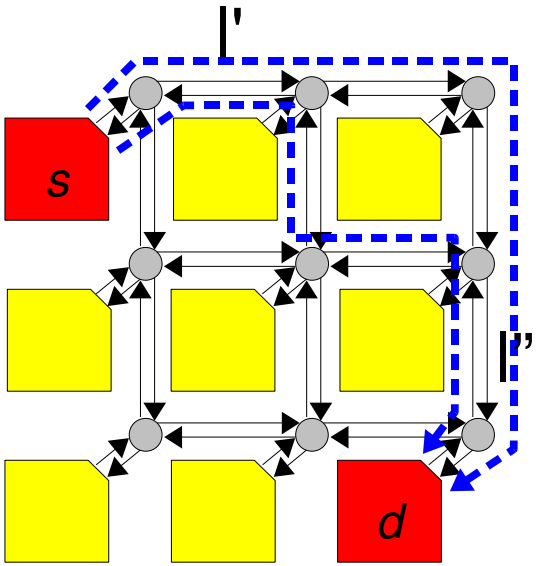
Robustness Index

- Is an extension of the concept of *path diversity*

$$RI(c)=\frac{1}{|L(c)|}\sum_{l\in L(c)}|P(c)\setminus P(c,l)|$$



$$R(s\to d)=\frac{1+1+1+1+1+1+1+1}{8}=1$$



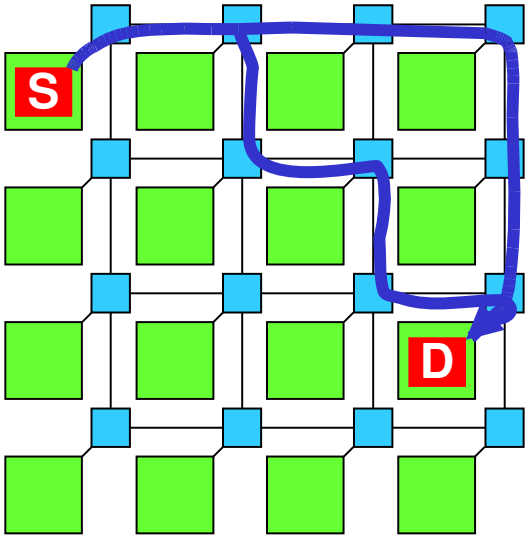
$$R(s\to d)=\frac{0+1+1+1+1+0}{6}=0.67$$

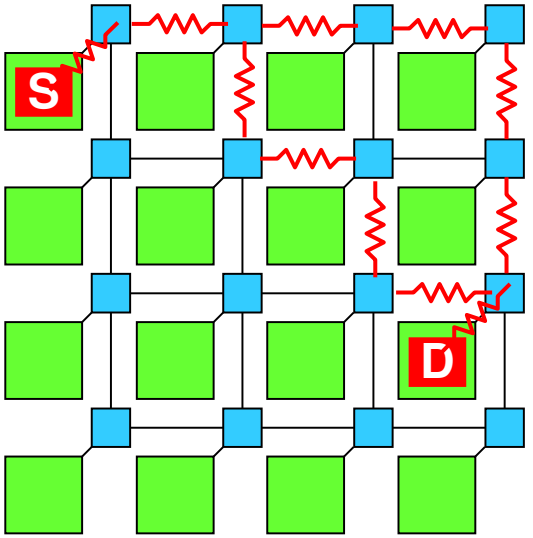
Armament to Deal with the Mapping Problem

- Characterization of NoC resources
  - ➔As the first step to develop a mapping technique for NoCs
- Find a model of the communication cost
  - ➔Correlated with the performance metrics
  - ➔Which does not require expensive simulations

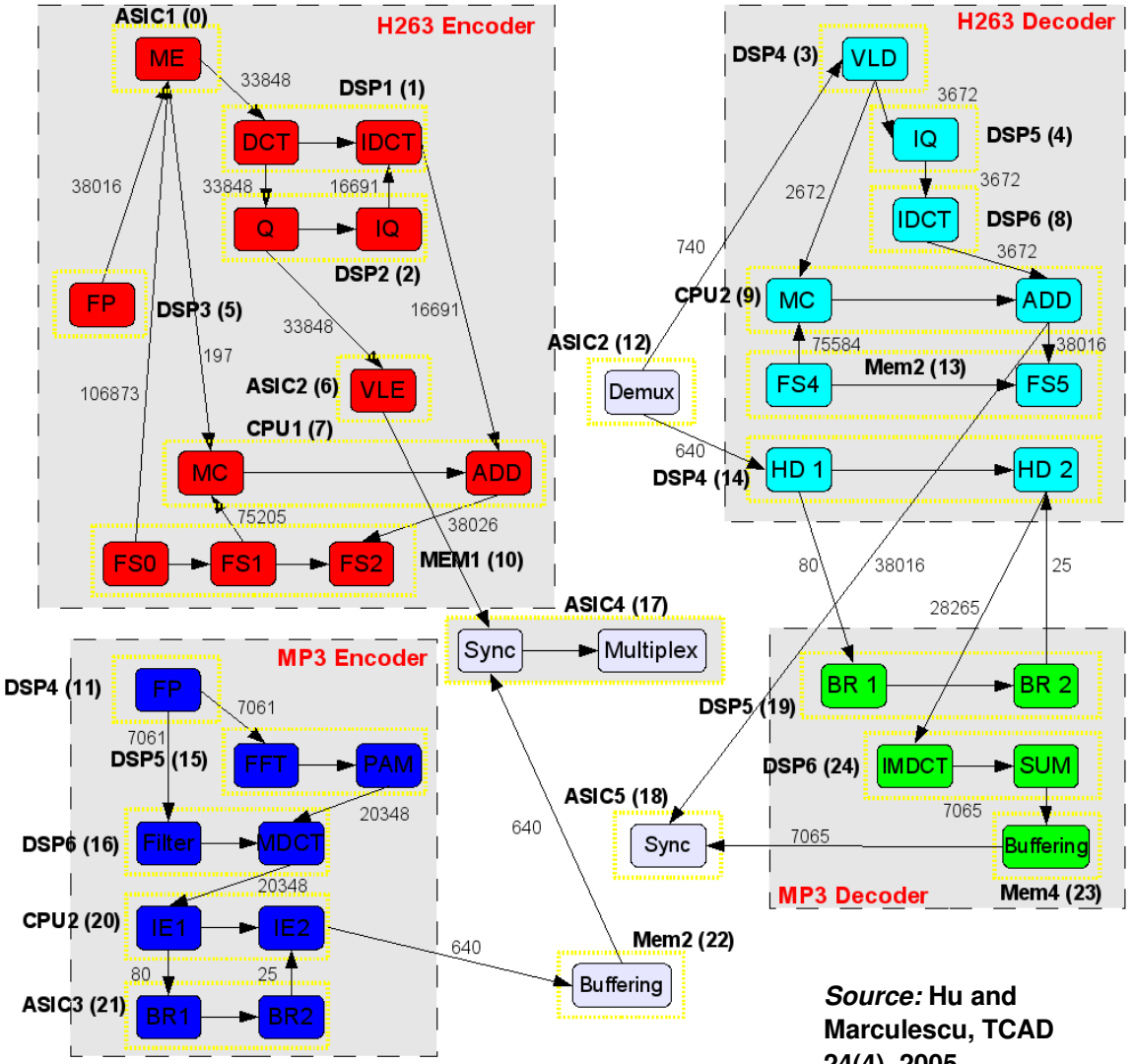
Model of Communication Cost

- Define a metric that does not depend on the traffic pattern
  - ➔ Based exclusively on the internode distance
    - ✔ Topology
    - ✔ Routing algorithm
- Equivalent distance
  - ➔ Analogy to the electrical equivalent resistence





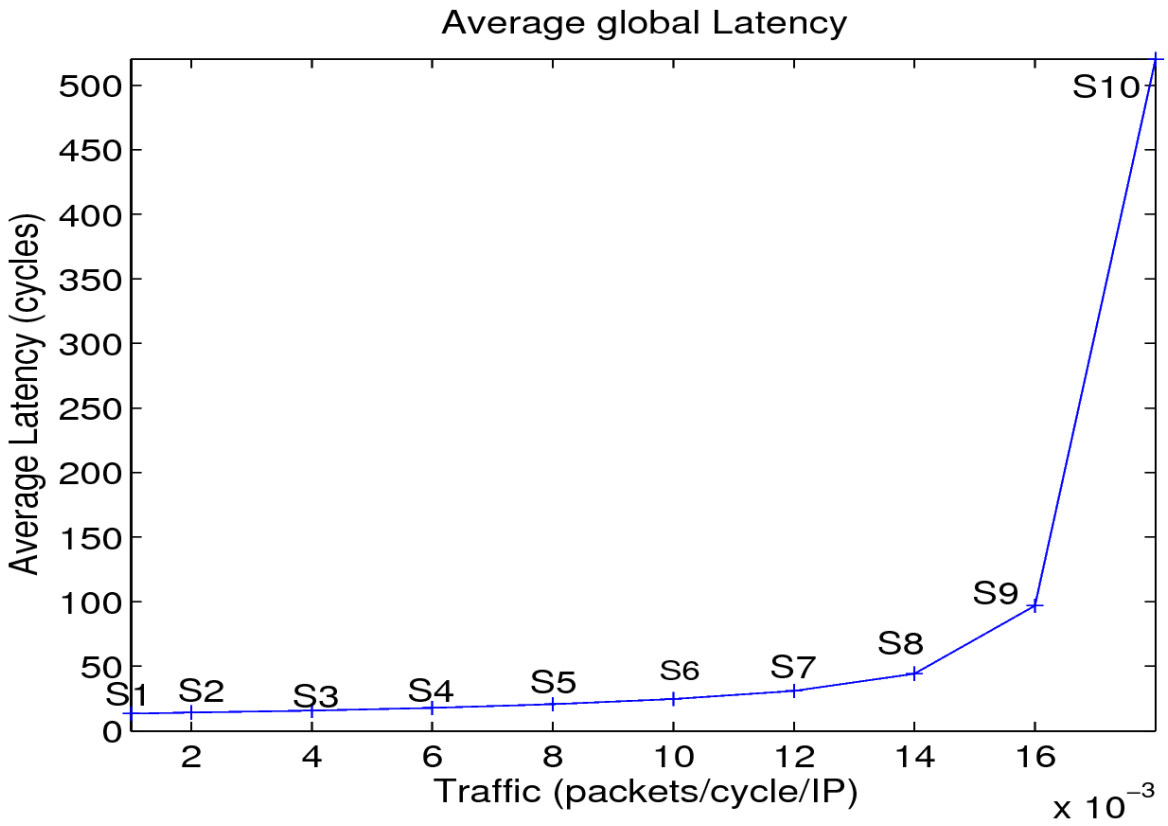
Multi Media System



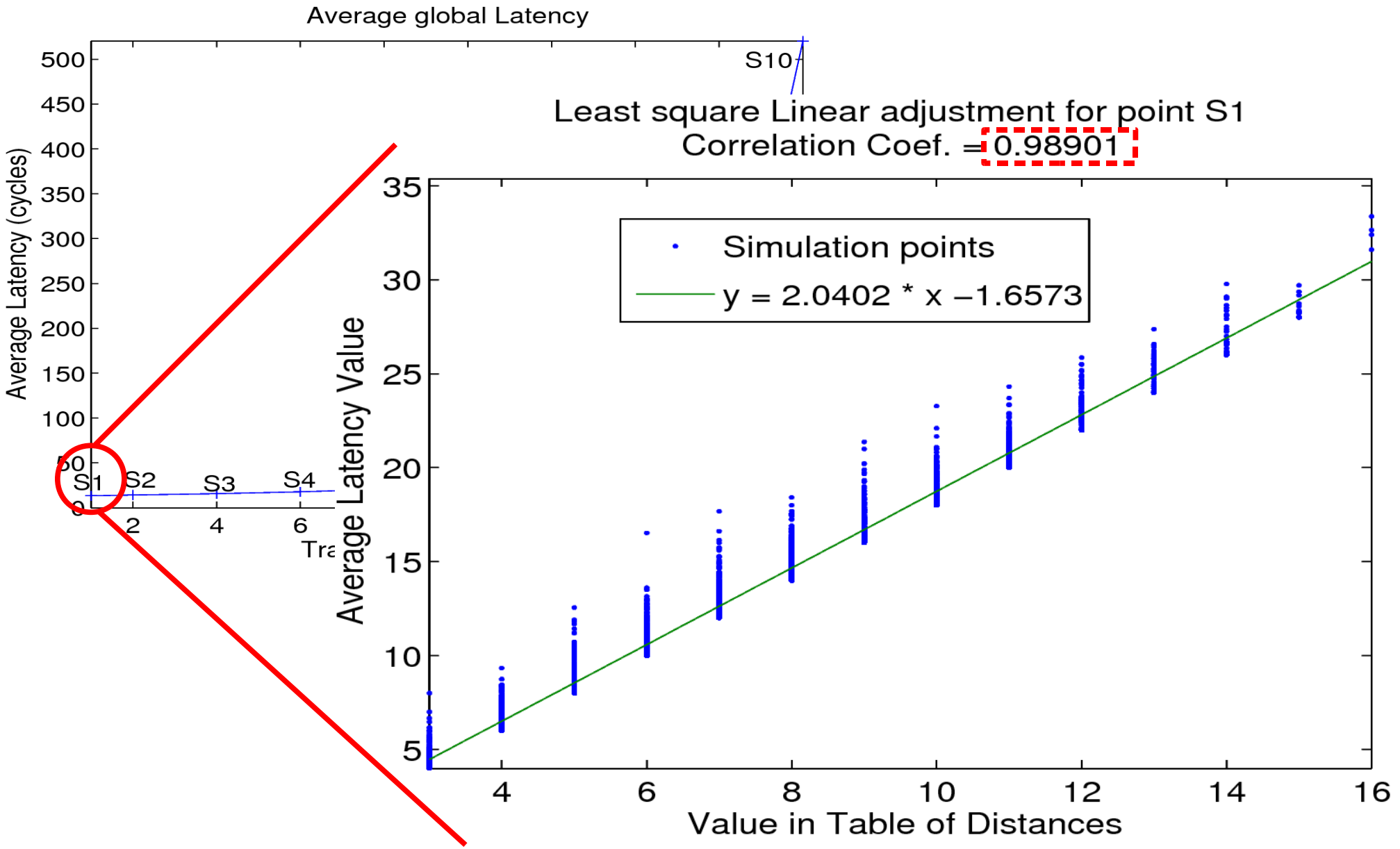
Source: Hu and Marculescu, TCAD 24(4), 2005

- 8x8 mesh-based NoC
- 8-flits packets
- 3-flits buffers
- SS packets injection distribution
- 50 simulations per point

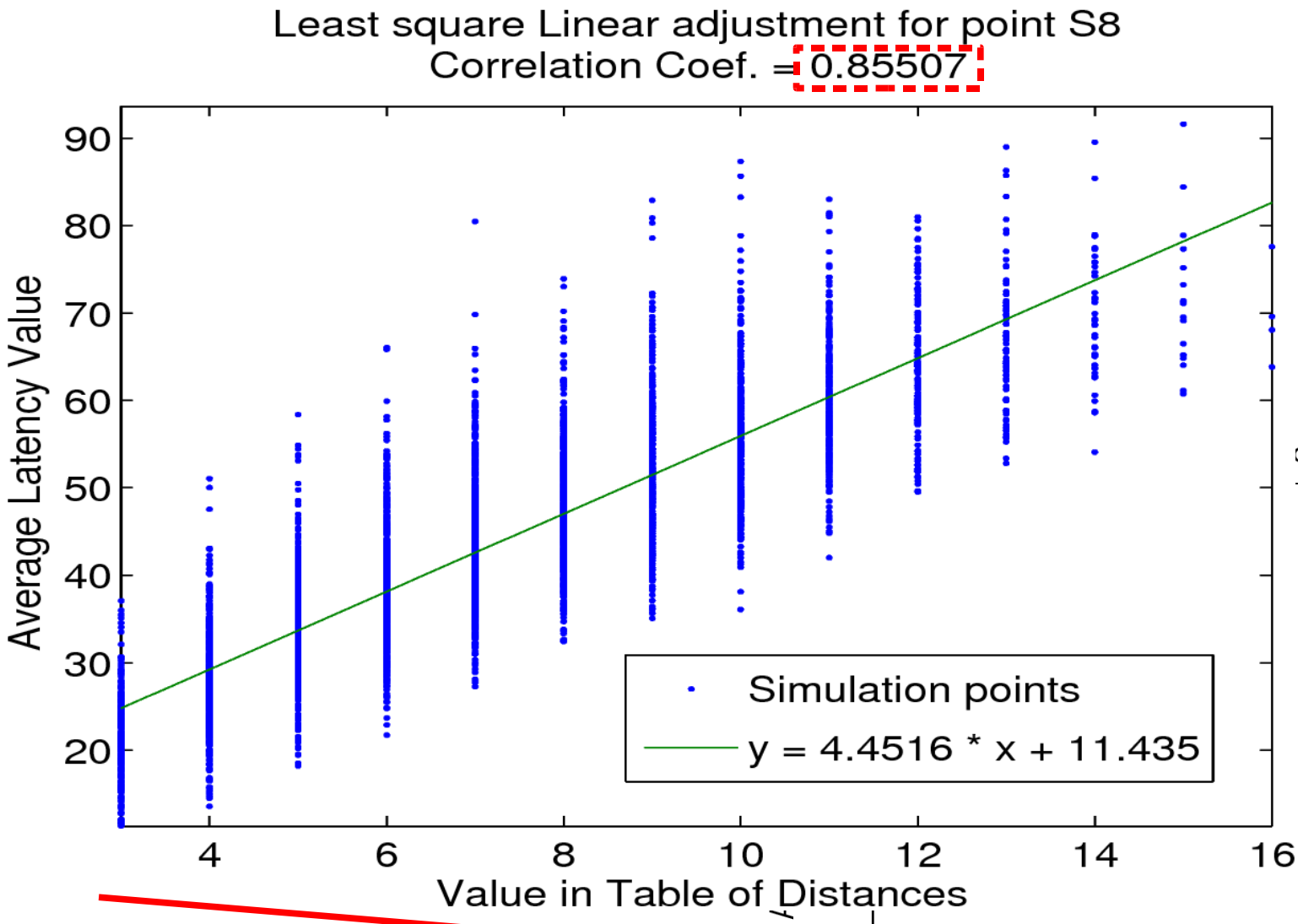
Simulation Results



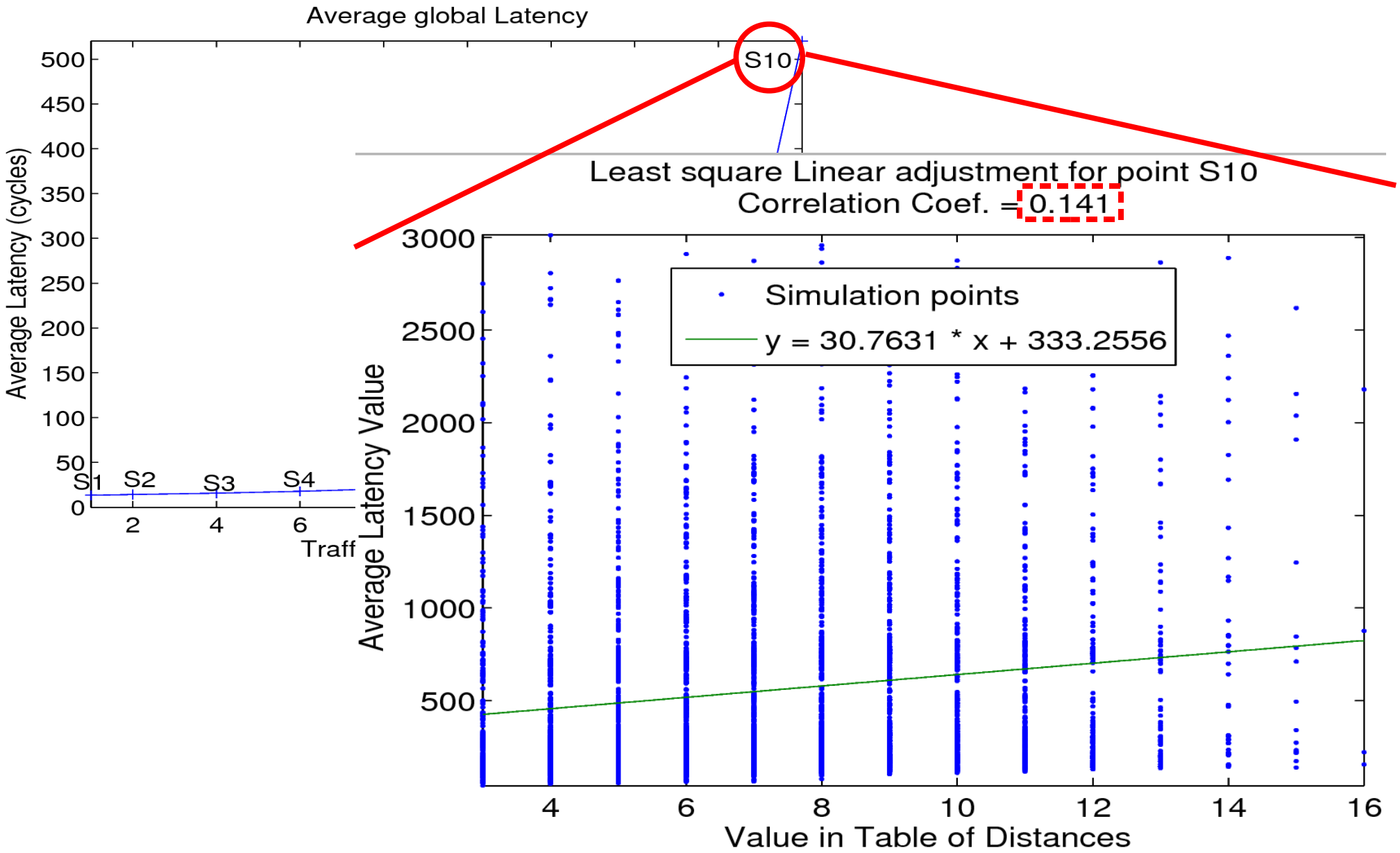
Correlation Index for *S1*



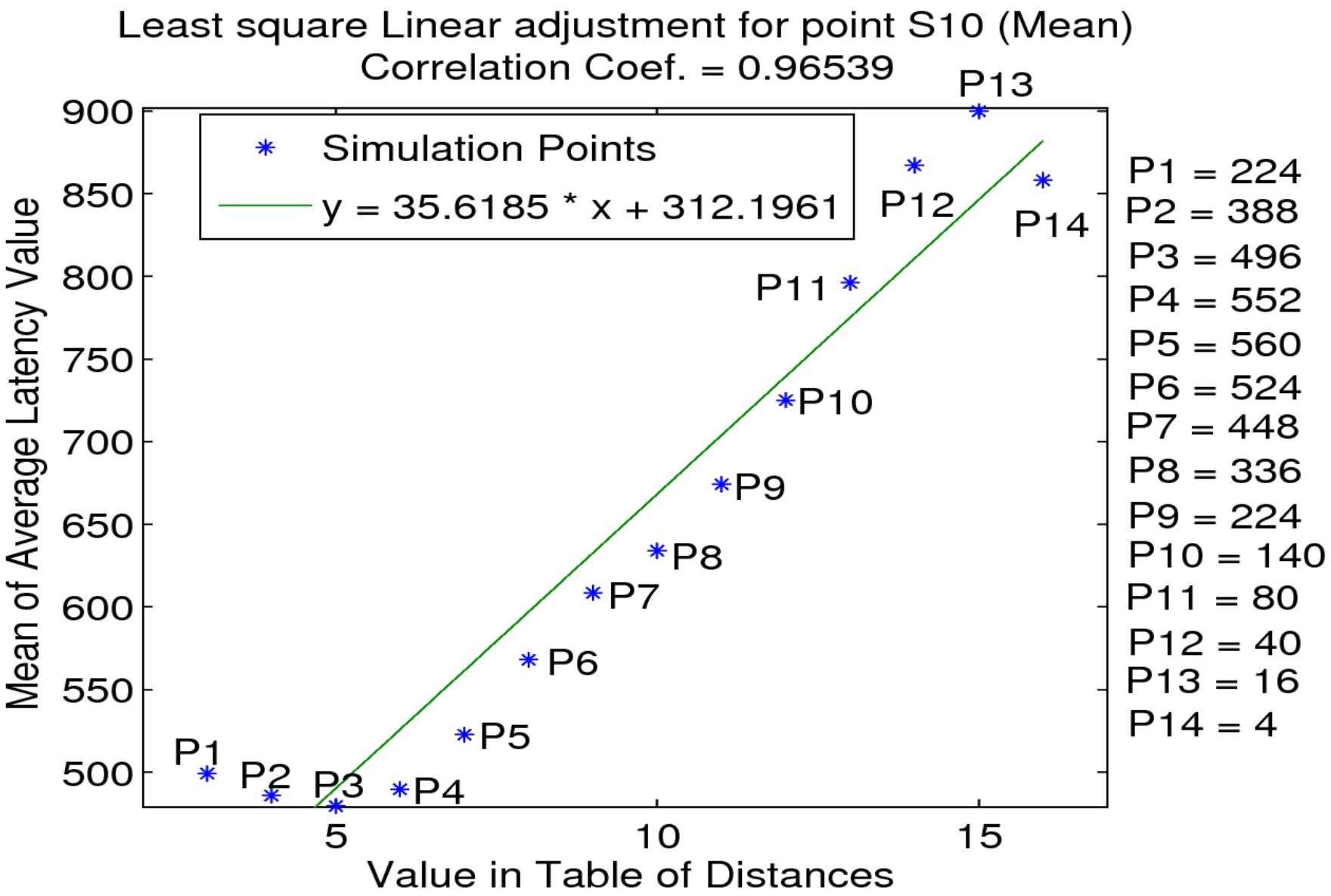
Correlation Index for *S8*



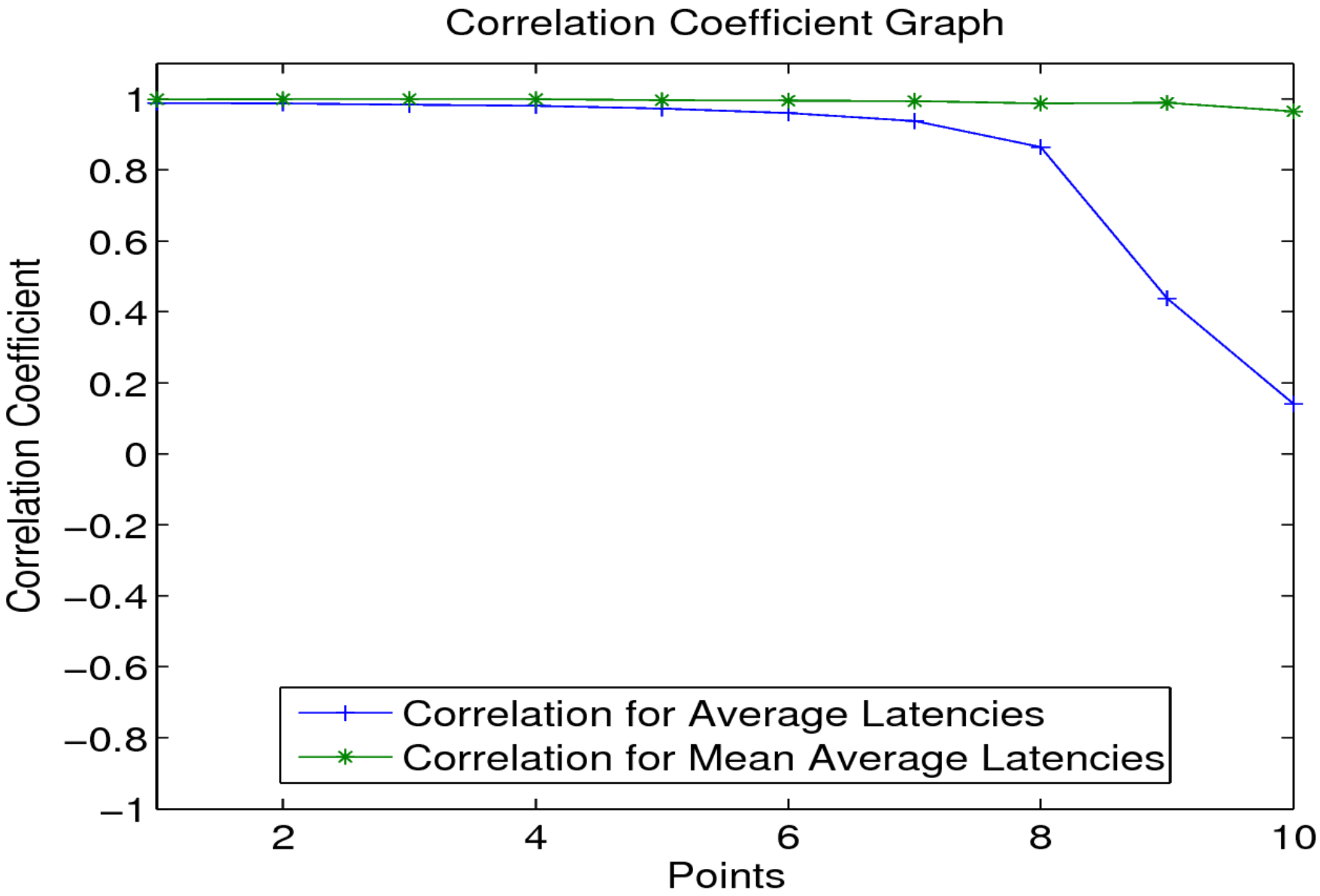
Correlation Index for *S10*



Correlation with the Mean of the Avg Latencies

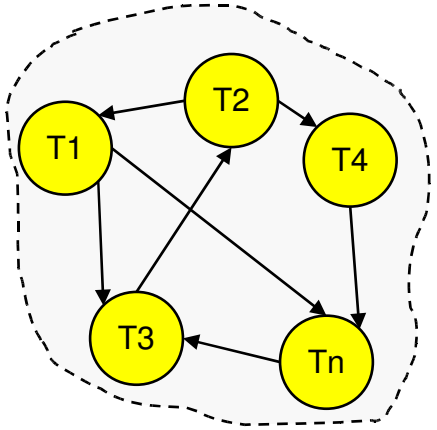


Correlation Coefficients

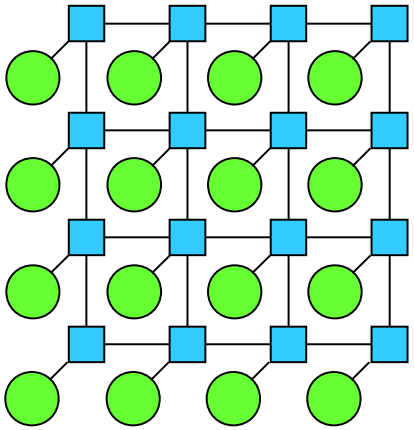


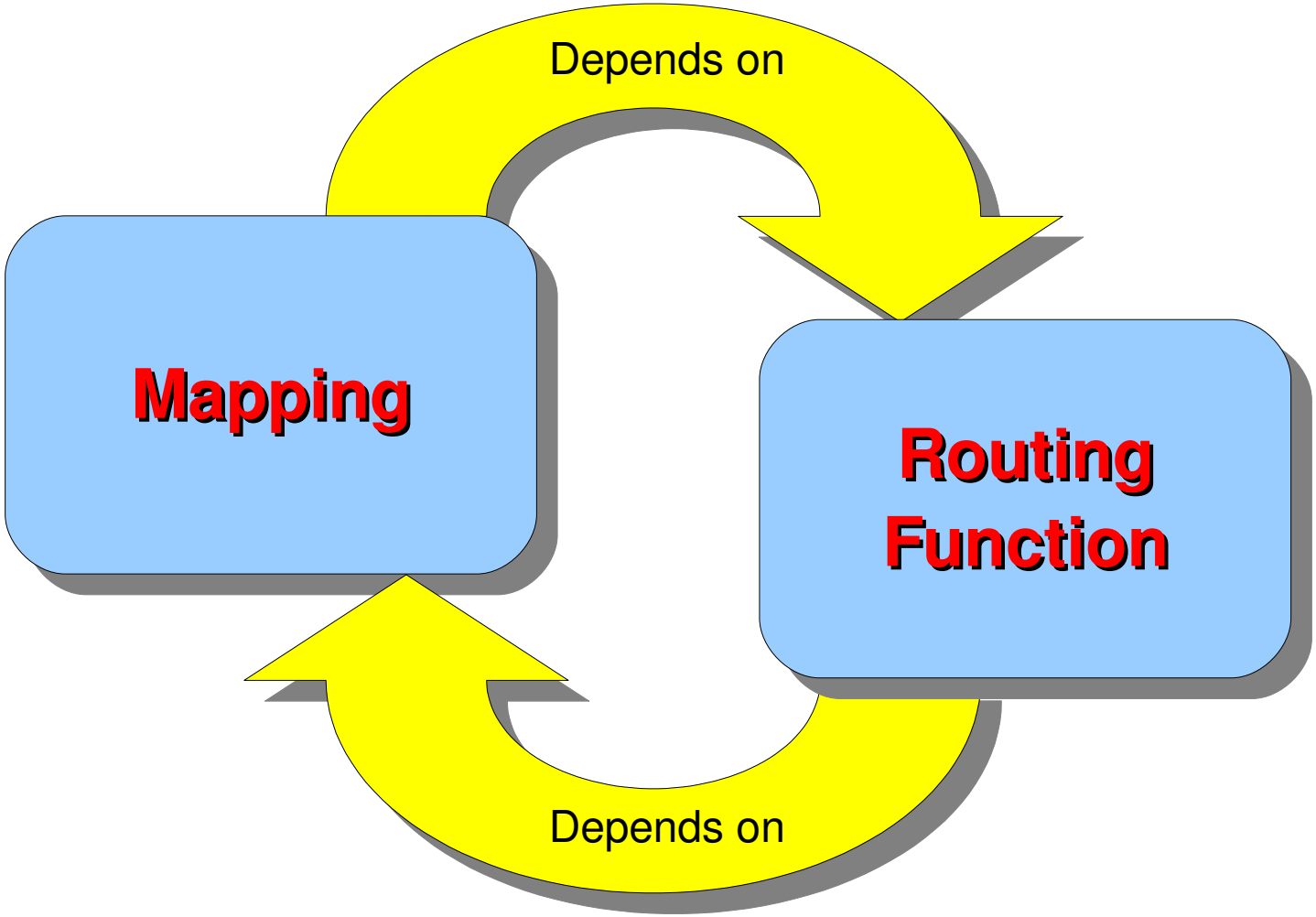
Cyclic Dependency

Application

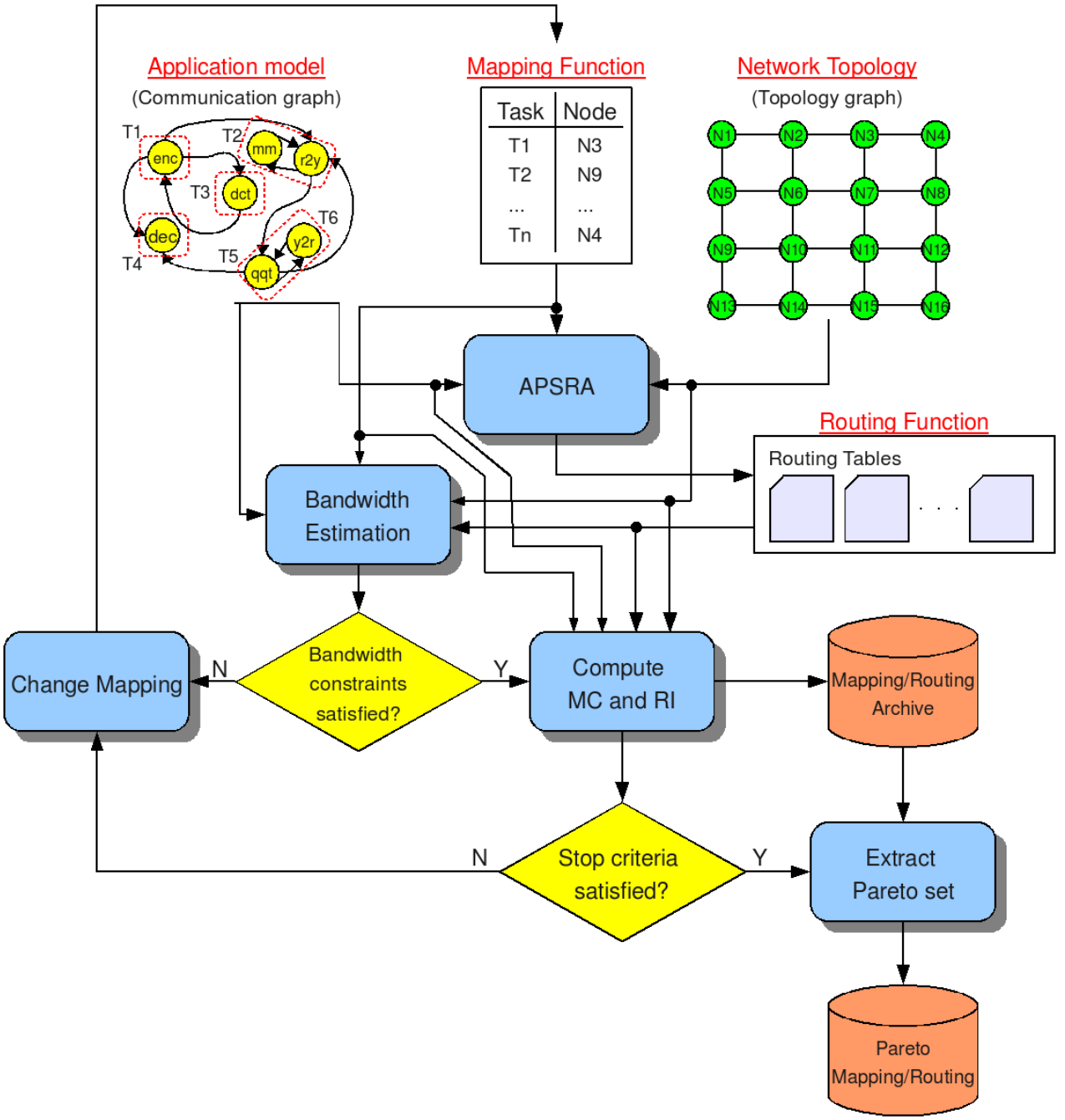


Network Topology

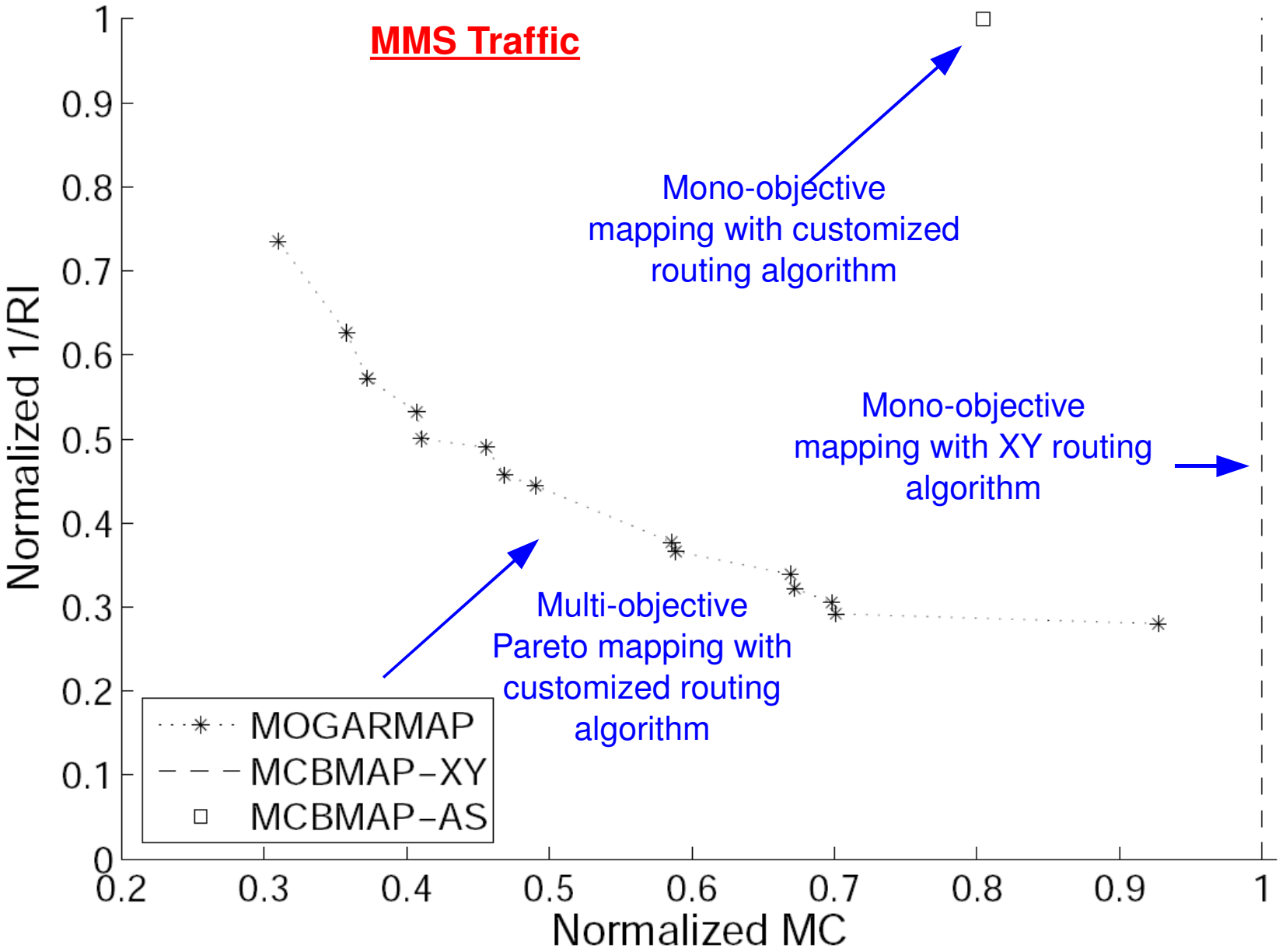




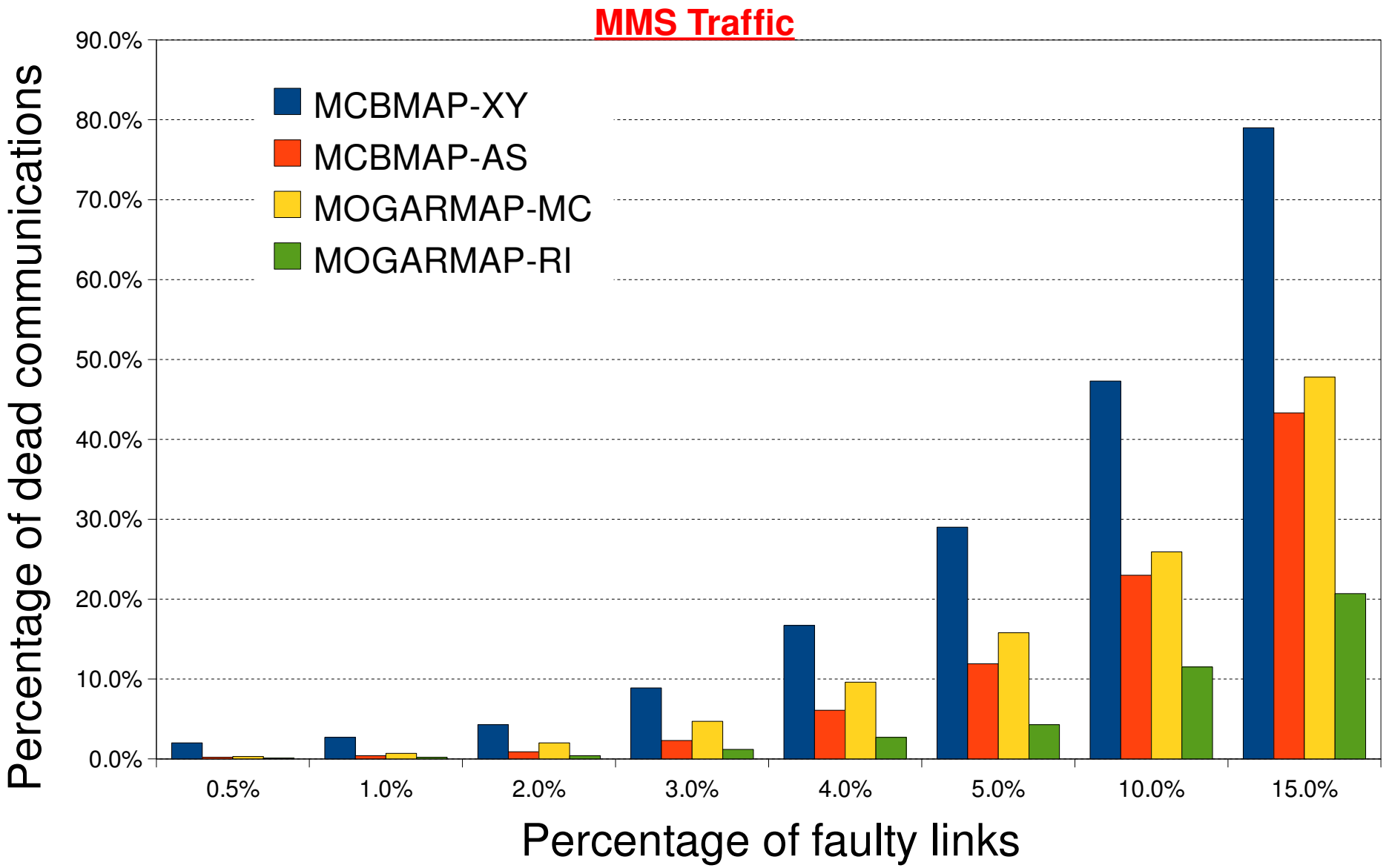
Design Space Exploration Flow



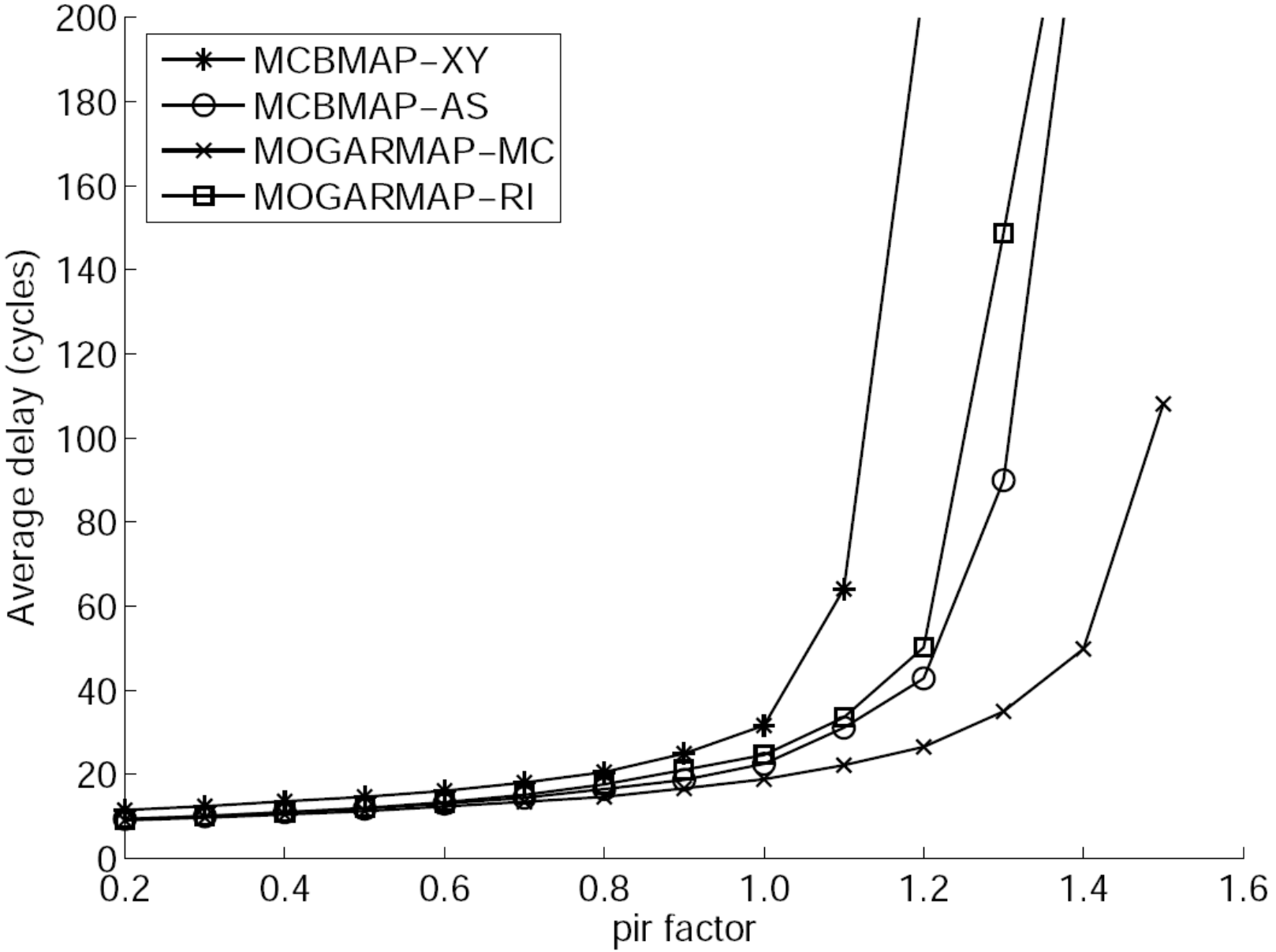
Experiments: Pareto front



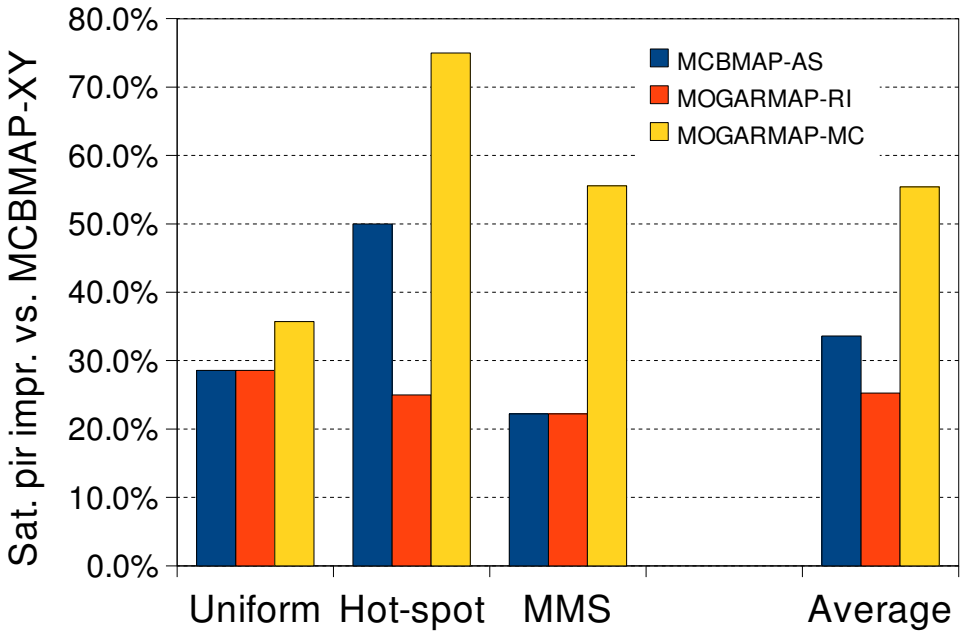
Experiments: Dead Comms



Experiments: Delay

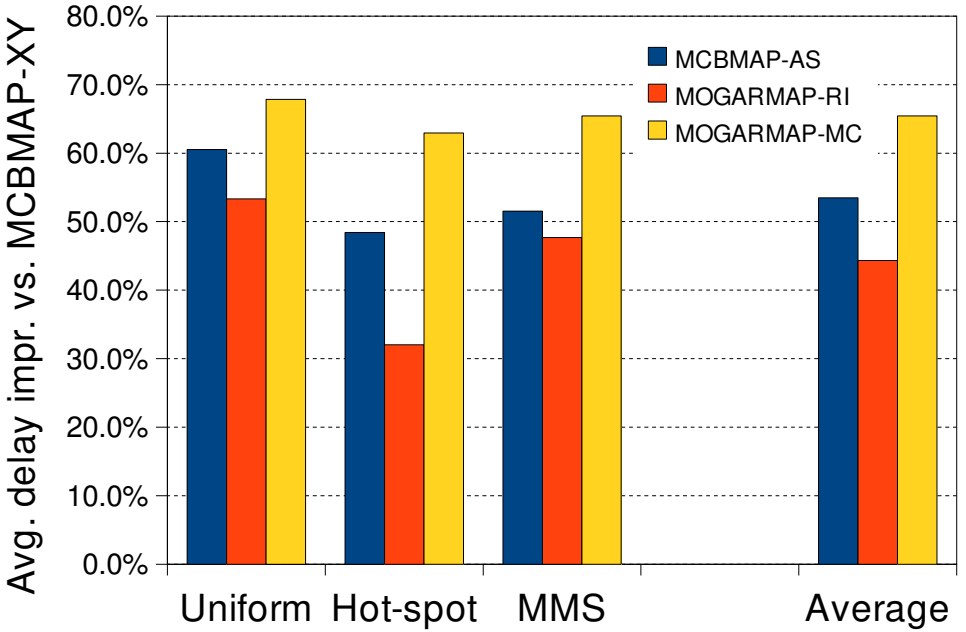


Experiments: Summary Improvement



Saturation *pir* improvement
(MCBMAP-XY as baseline)

Average delay reduction
(MCBMAP-XY as baseline)



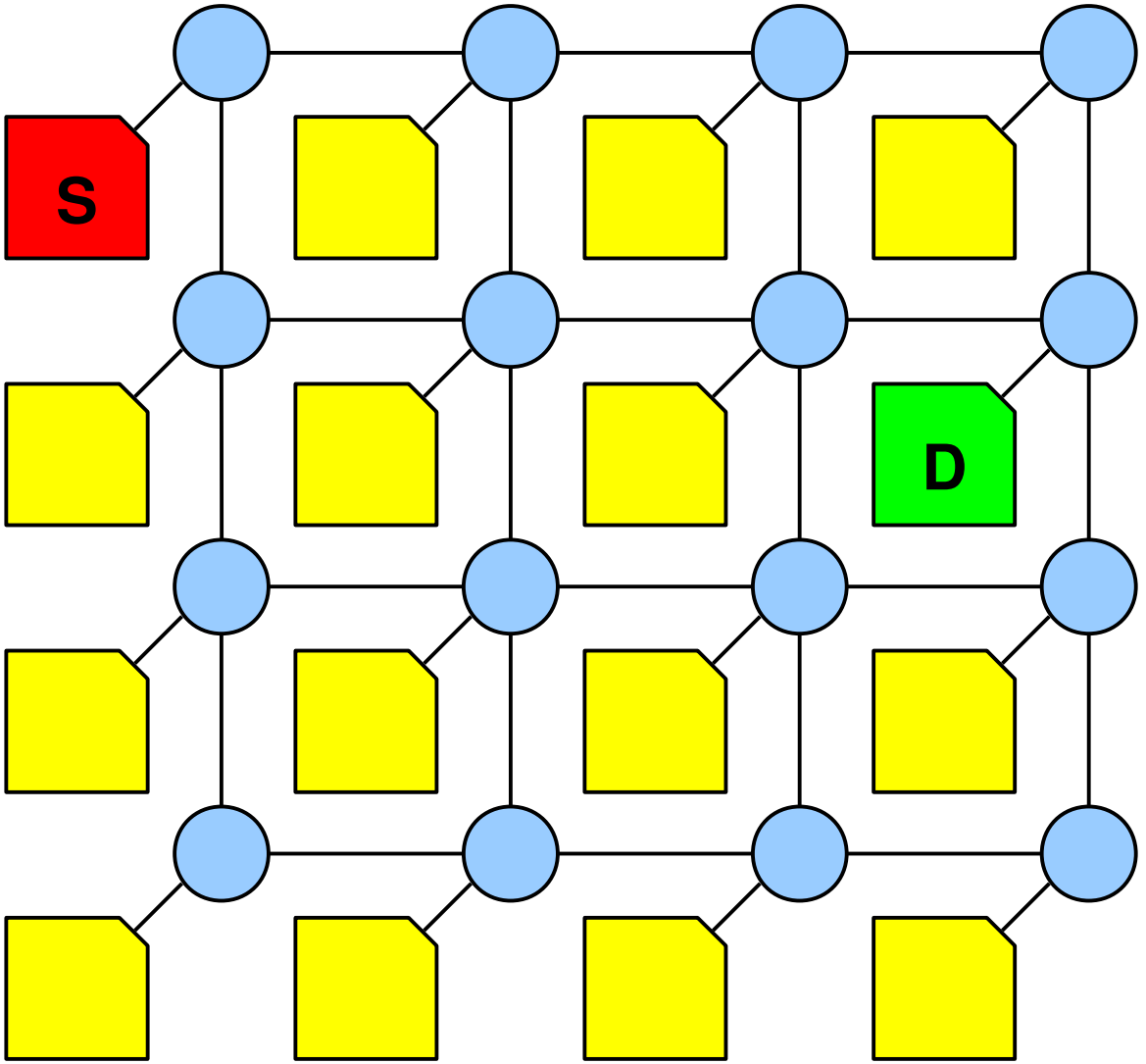
Outline

- Application Specific Routing Algorithms ✓
- Concurrent Mapping and Routing ✓
- Dealing with Manufacturing Defects
- Encoding Scheme for Low Power

Introduction and Motivations

- Initial yield of complex SoC is very small
  - ➔Yield goes down with size and complexity of the chip
  - ➔Dealing with the reduction of yield due to manufacturing defects
    - ✔Isolate faulty blocks of the chip
    - ✔Using the chip as a “depowered” chip (E.g., Sun UltraSparc T1)
- On-chip communication system
  - ➔Represents the heart of the system
  - ➔Gets a quite high percent of the system silicon area
    - ✔E.g., 20% of the silicon area in Intel's TeraScale 80-cores chip
    - ✔High probability of being affected by manufacturing defects

Managing Faulty Links



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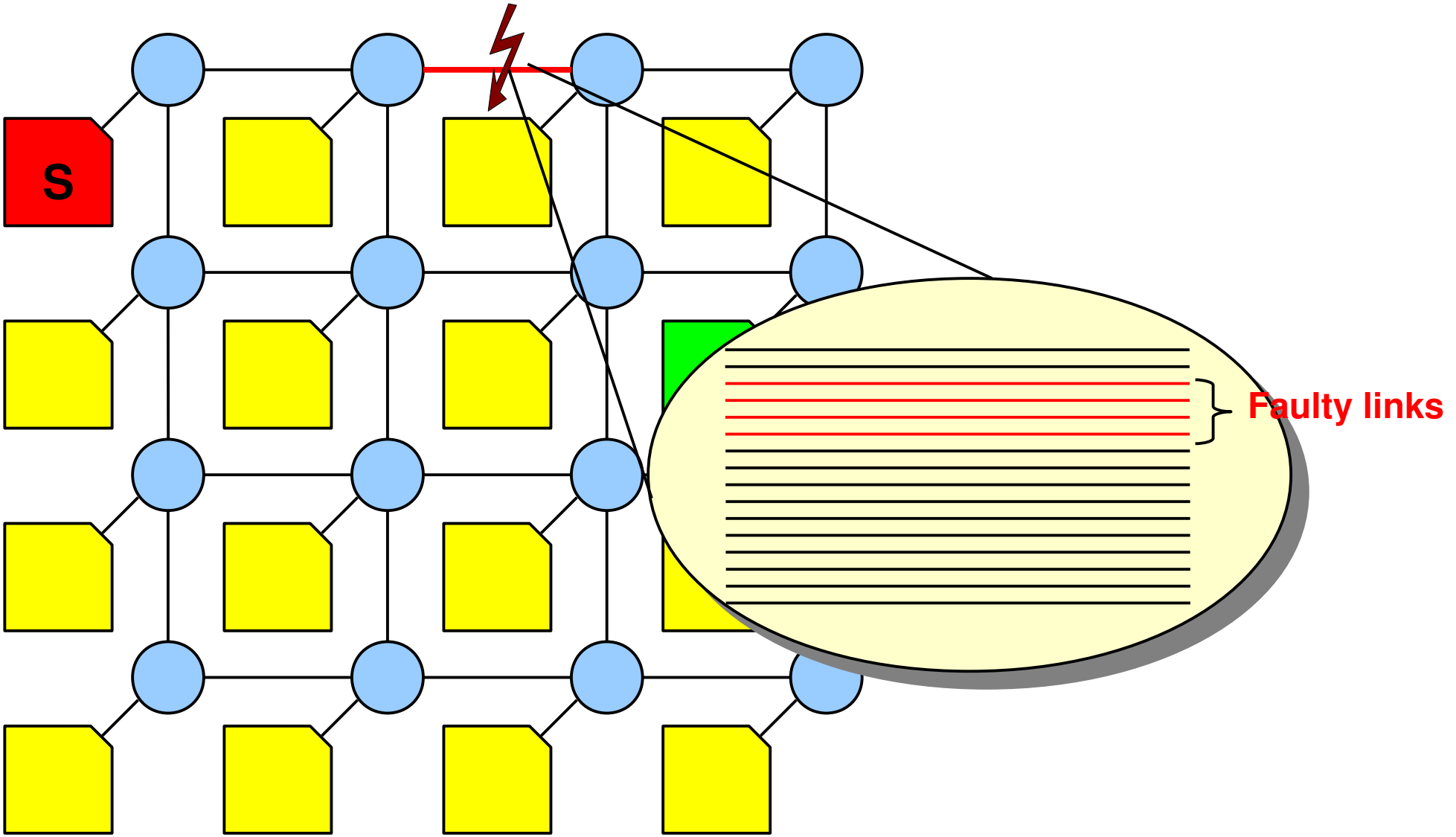
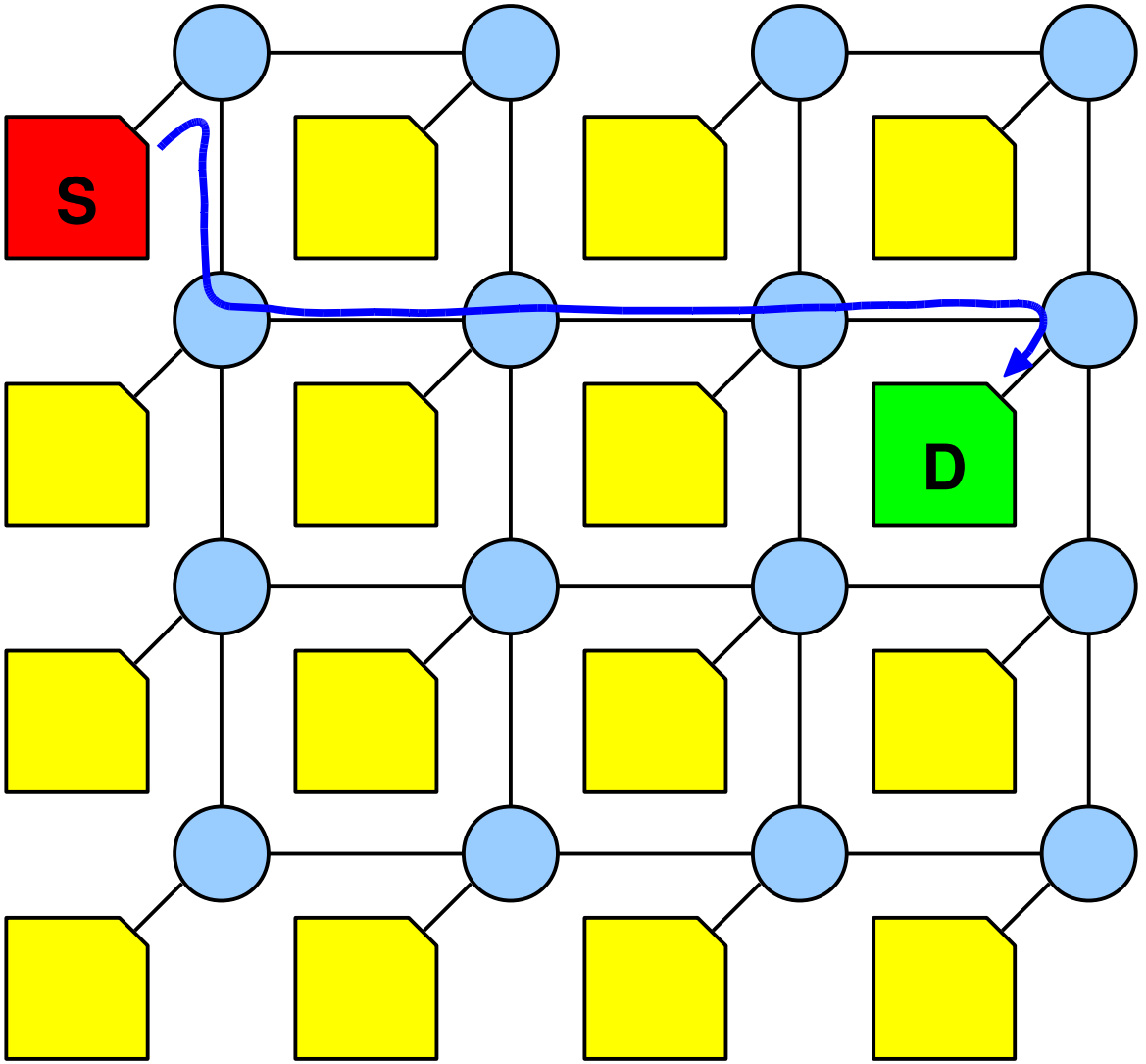
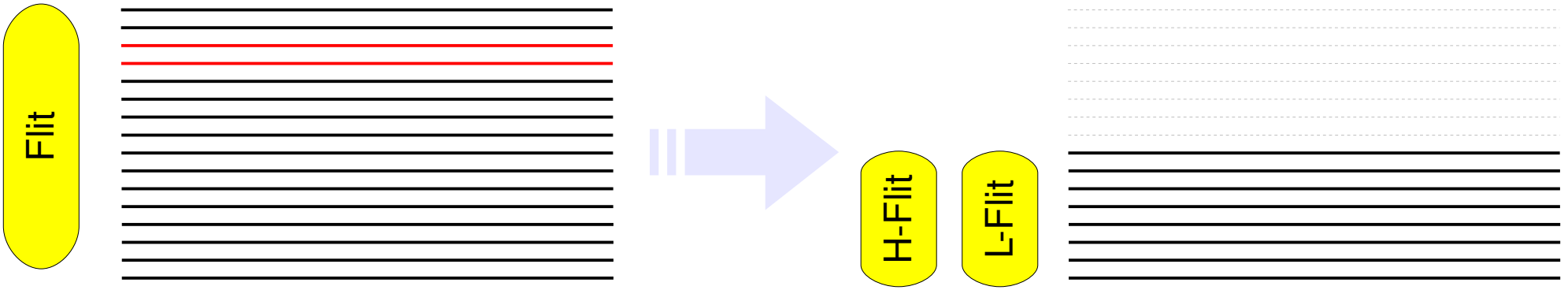


Managing Faulty Links

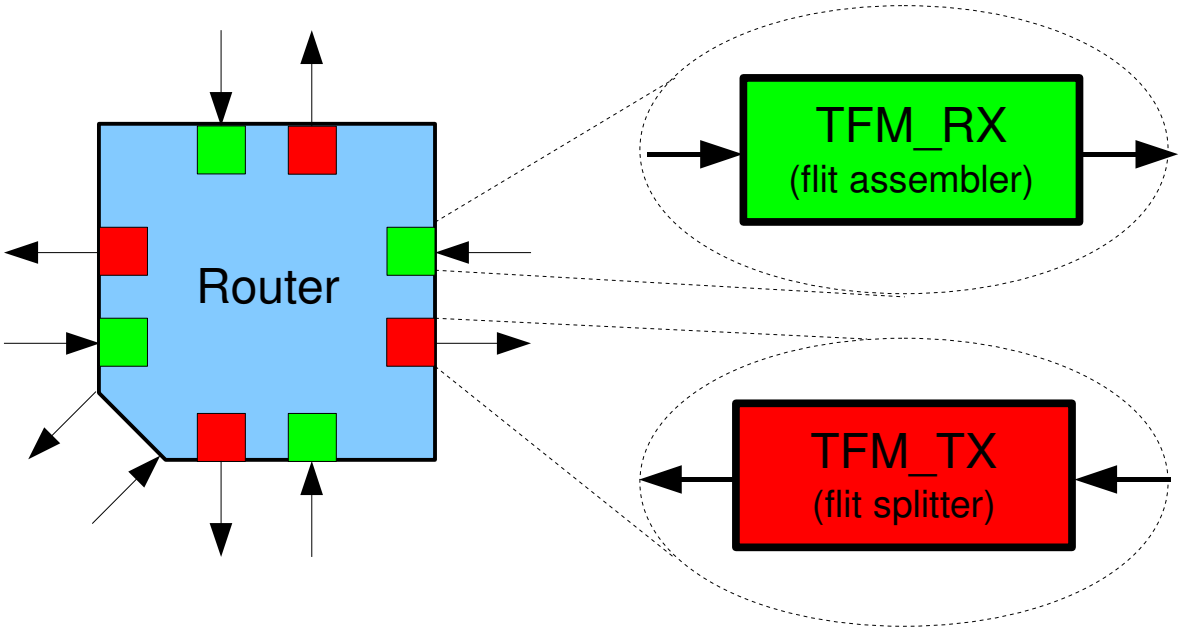


- Faulty links elimination
  - ➔ The *routing function* is computed on the basis of the network **filtered** by all the *fully faulty* or *partially faulty* links

Managing Faulty Links

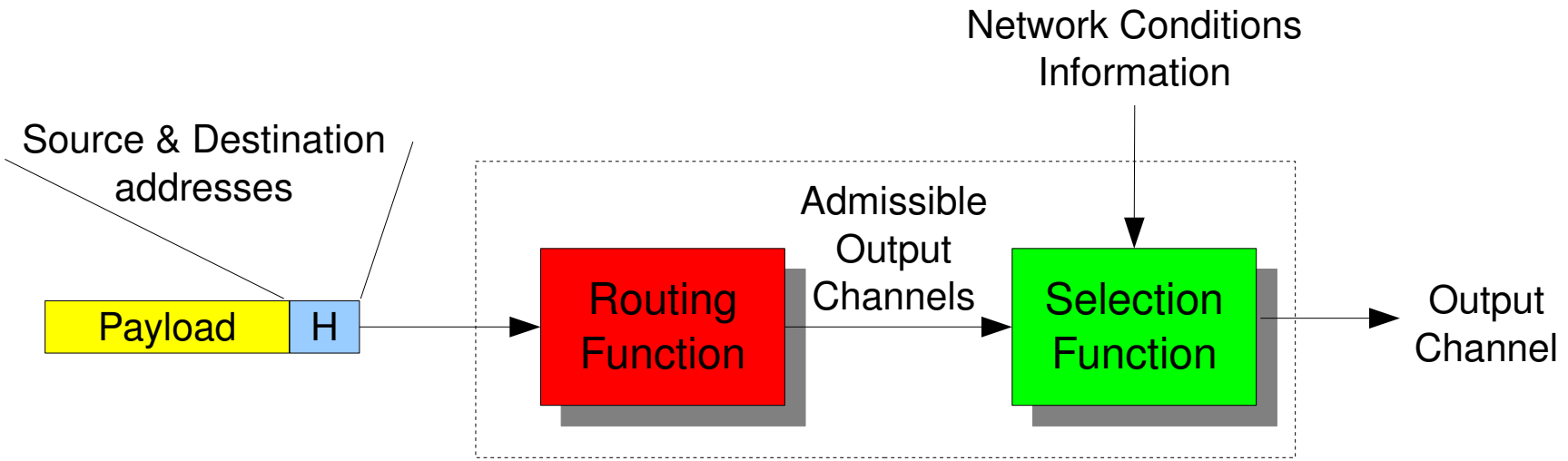


- Partially Faulty Links usage
  - ➔ The *routing function* is computed on the basis of the network filtered by all partially faulty links with a *fault degree* greater than a certain threshold

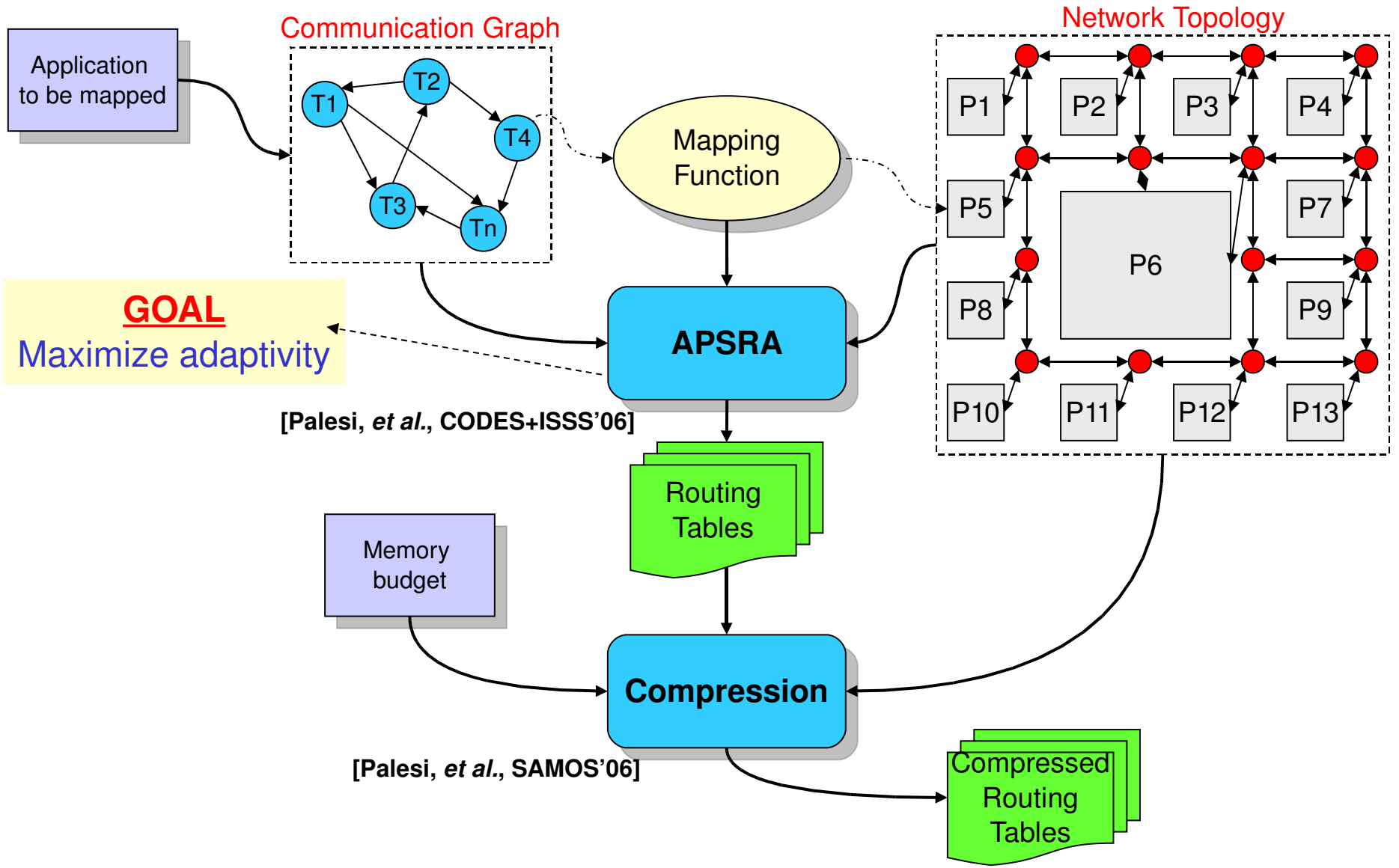


Two Questions

- How routing paths are determined?
  - ➔Routing function
- When does a partially faulty link should be used?
  - ➔Selection function



Routing Function

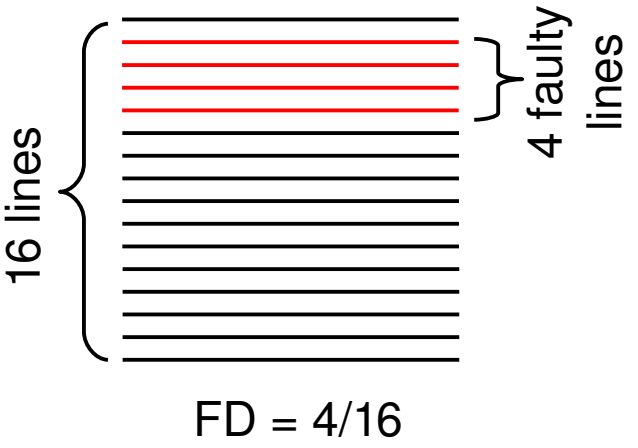


Selection Function

- Faulty Links elimination (**FE**)
- Partially Faulty Links usage strategy (**FU**)
- Partially Faulty Links usage with Look-ahead strategy (**FUL**)
- Load Balancing based strategies (**LB**)
  - ➔**FE+LB**
  - ➔**FU+LB**
  - ➔**FUL+LB**

Partially Faulty Links usage Strategy

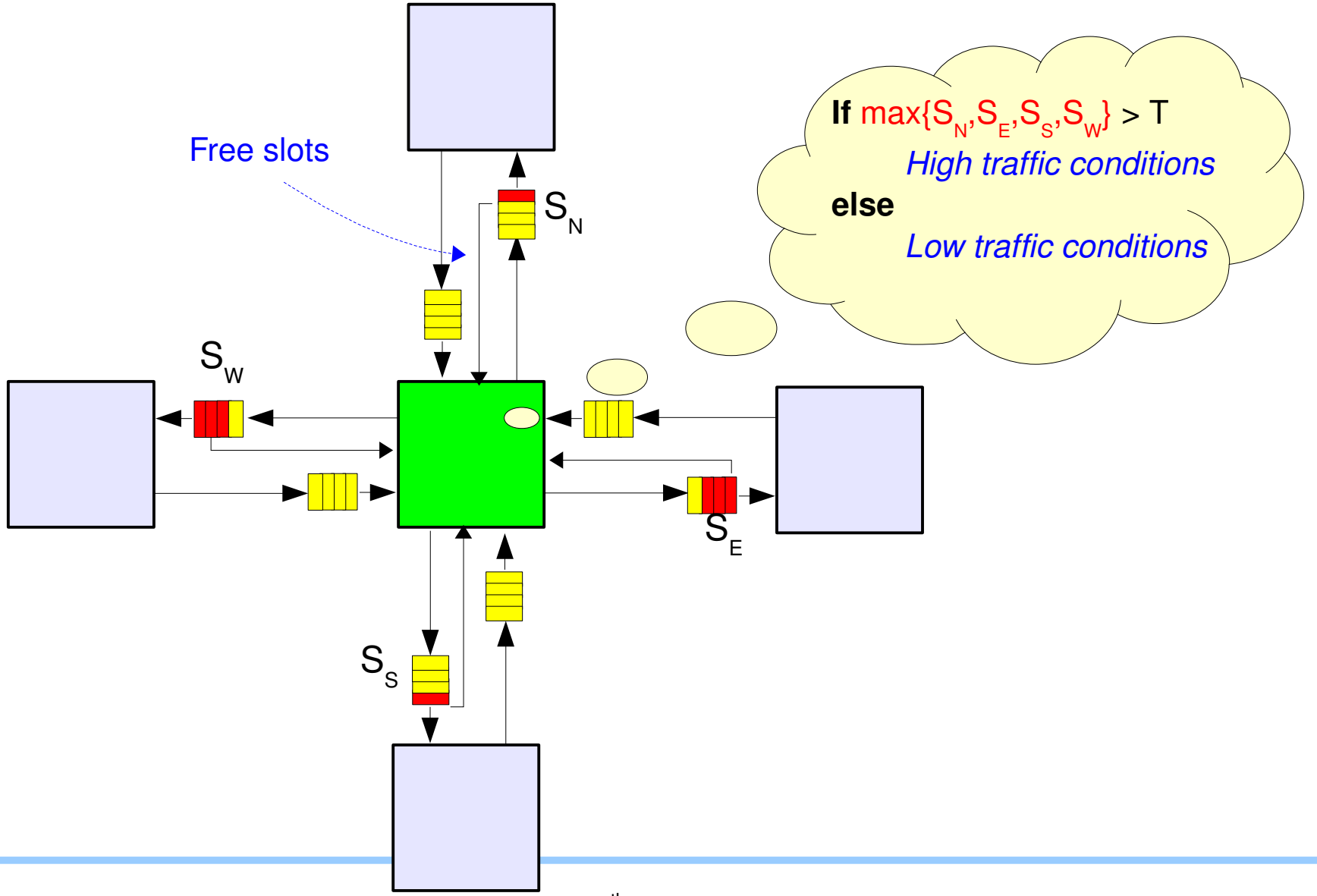
- In *low traffic* conditions
  - ➔Only fault free links are chosen, if available. Otherwise, links with lowest FD are chosen
- In *high traffic* conditions
  - ➔A link is selected with a probability inversely proportional to its FD



$$Pr^{(F)}(l_i) = \frac{1 - FD(l_i)}{1 - \sum_{l_j \in L_{ao}} FD(l_j)}$$

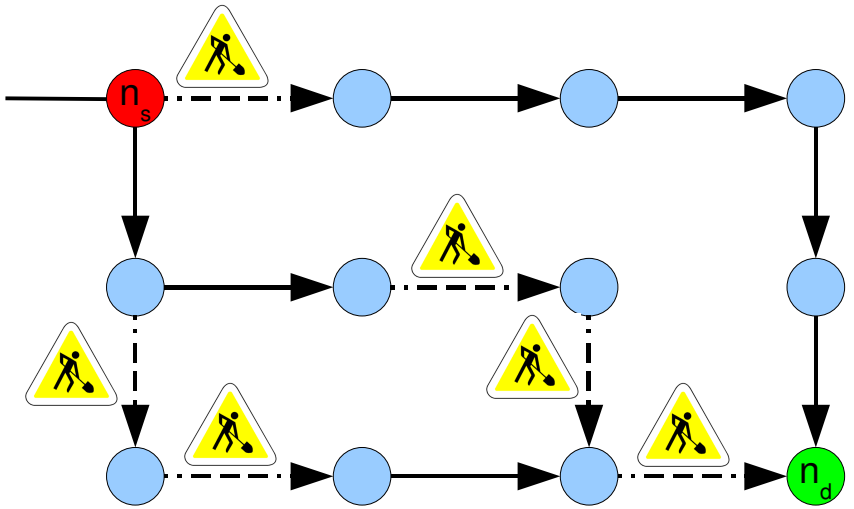
Detecting Traffic Conditions

- Hu and Marculescu, *DyAD: Smart Routing for Networks-on-Chip*, DAC 2004



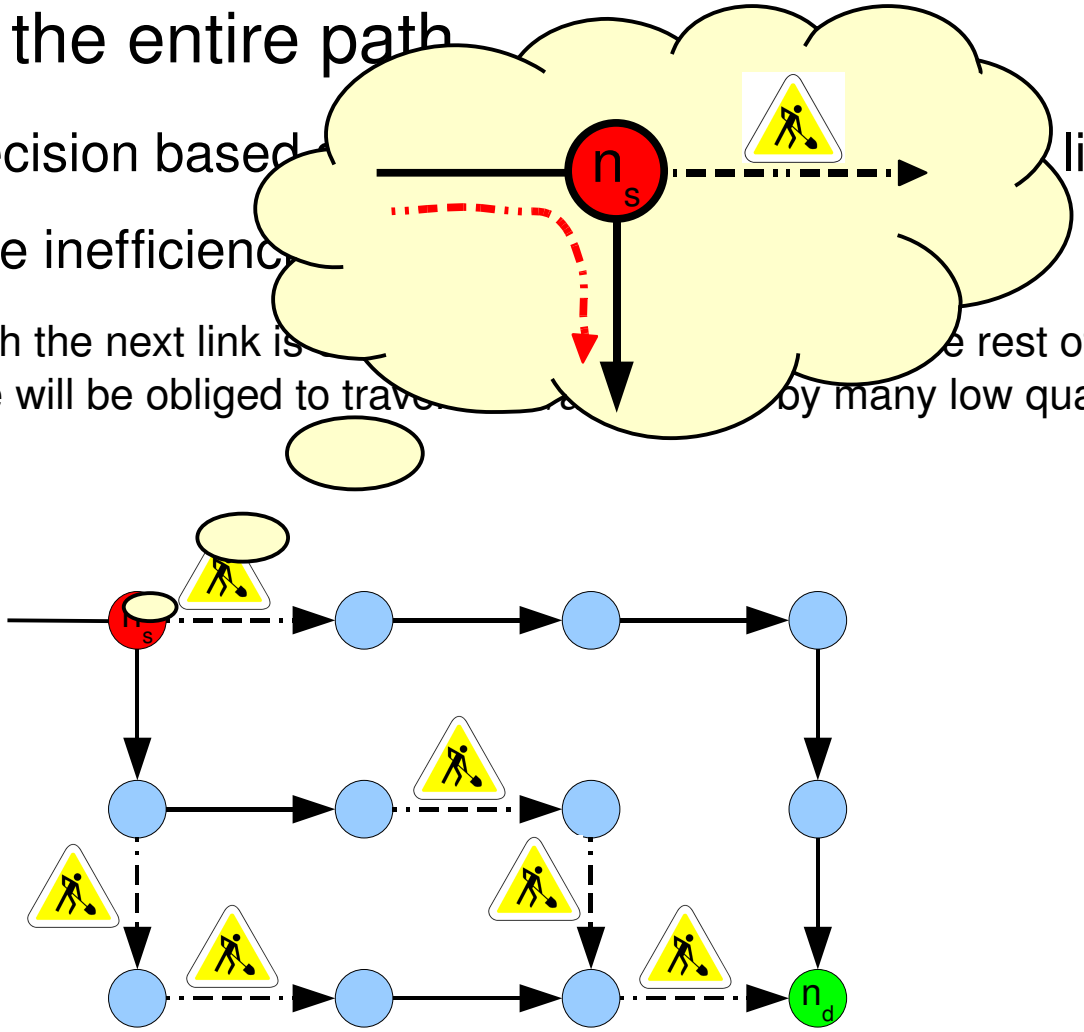
Limitation of FU strategy

- The selection function used in FU, does not take into consideration the entire path
  - ➔ It takes the decision based solely on the quality of the next link
  - ➔ This can cause inefficiencies
    - ✔ *E.g.*, although the next link is of high-quality (*e.g.*, fault free), the rest of the path(s), in which the message will be obliged to travel on is/are formed by many low quality links



FU with Look-ahead Strategy (FUL)

- The selection function used in FU, does not take into consideration the entire path
  - ➔ It takes the decision based [illegible] link
  - ➔ This can cause inefficienc[illegible]
    - ✔ *E.g.*, although the next link is [illegible] rest of the path(s), in which the message will be obliged to trav[illegible] by many low quality links



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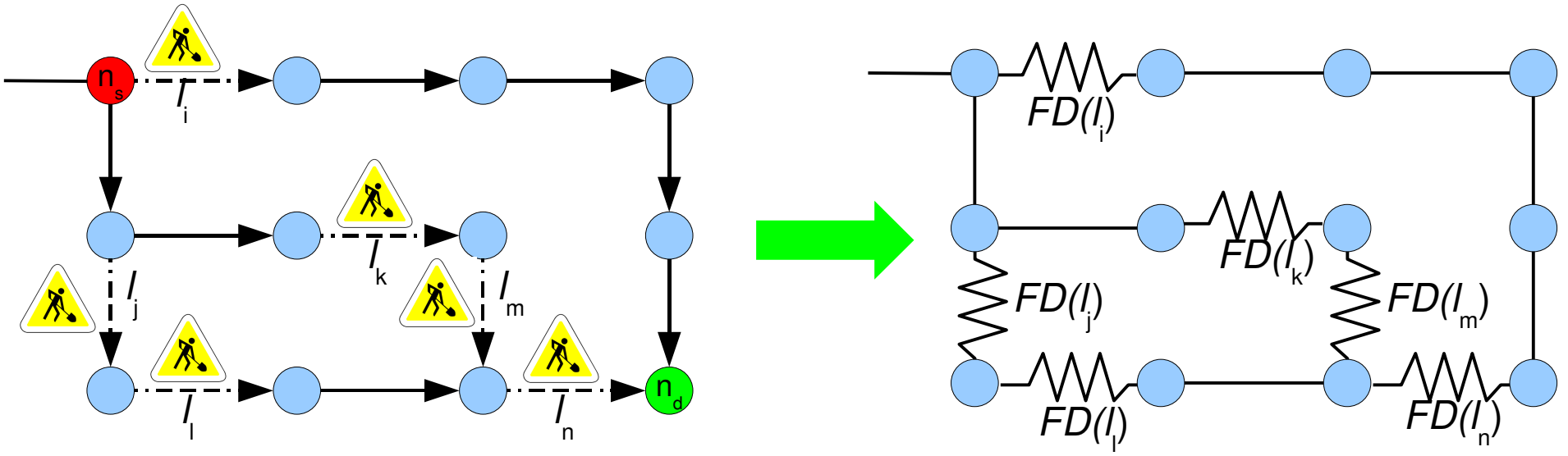
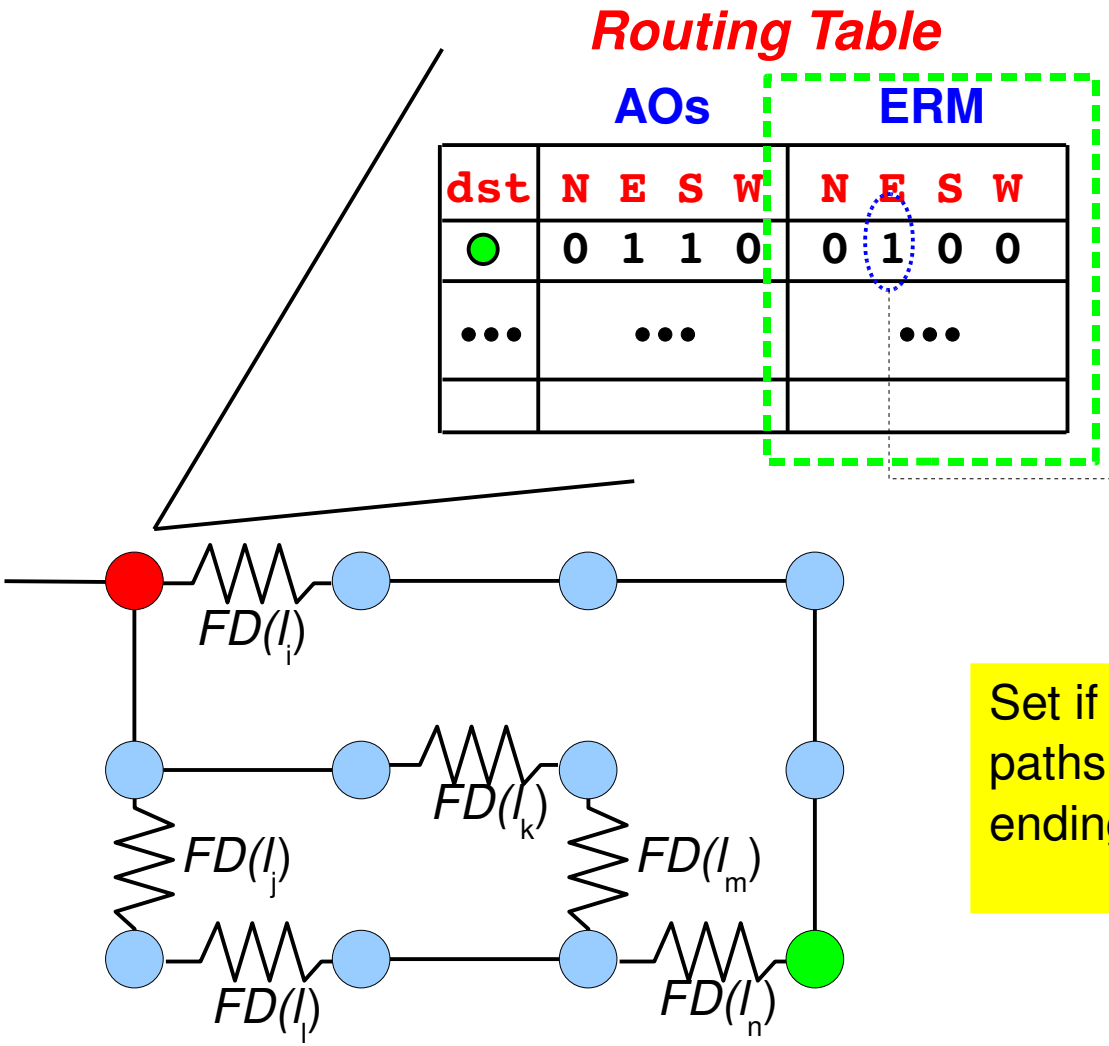
- The selection function used in FU, does not take into consideration the entire path
  - ➔ It takes the decision based solely on the quality of the next link
  - ➔ This can cause inefficiencies
    - ✔ *E.g.*, although the next link is of high-quality (*e.g.*, fault free), the rest of the path(s), in which the message will be obliged to travel on is/are formed by many low quality links



FU with Look-ahead Strategy (FUL)



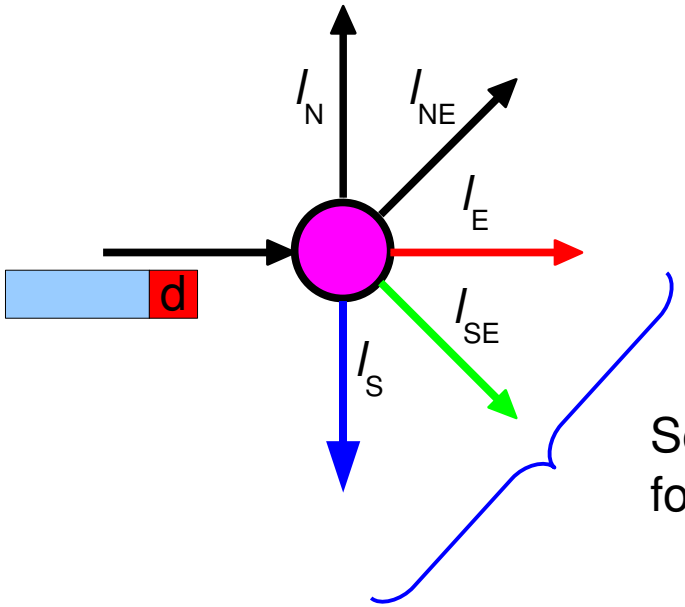
Set if the equivalent resistance of paths having as first link **E** and ending at node ● is minimum

FU with Look-ahead Strategy (FUL)

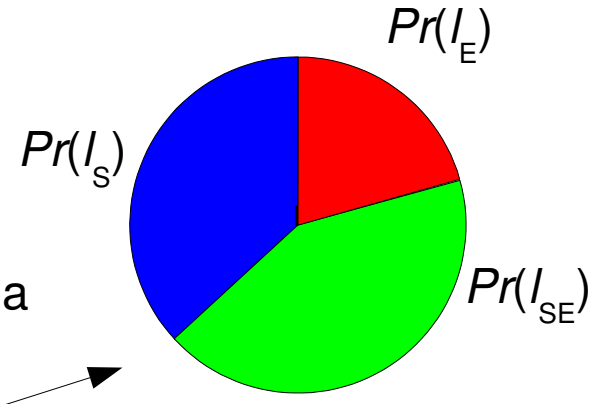
- In *low traffic* conditions
  - ➔One of the *AO* links I_i such that the *i*-th bit of ERM is set, is randomly chosen
    - ✔If multiple faulty free paths exist, they are always used
- In *high traffic* conditions
  - ➔The same as FU

Load Balancing Technique

- Determining the best set of *selection probabilities* which allow to *optimally distributing* the traffic over the network



Set of admissible outputs for a certain destination



Selection probabilities for a given router and a given destination

Selection Function

Load Balancing Technique

- Traffic Function ***TF(l,X)***
  - ➔Returns an estimation of the traffic load on network link ***l*** when the set of selection probabilities ***X*** is used
- Goal

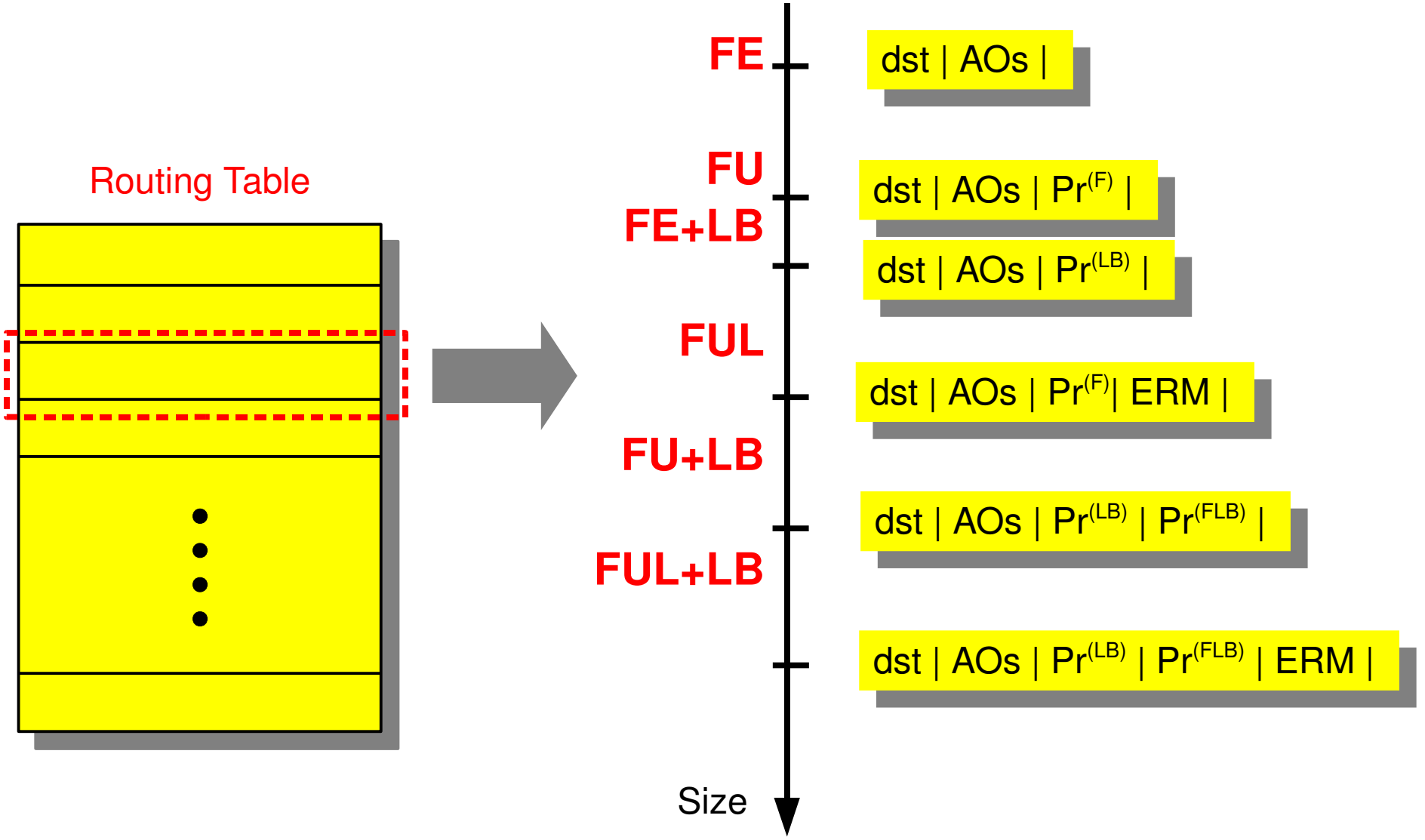
$$\min_{X} \operatorname{var}_{l \in L} TF(l,X)$$

  - ➔Such that X is a feasible set of selection probabilities ($x_i \in [0,1]$, $\Sigma x_{li,d,lo}=1$)
  - ➔Sequential Quadratic Programming Optimization

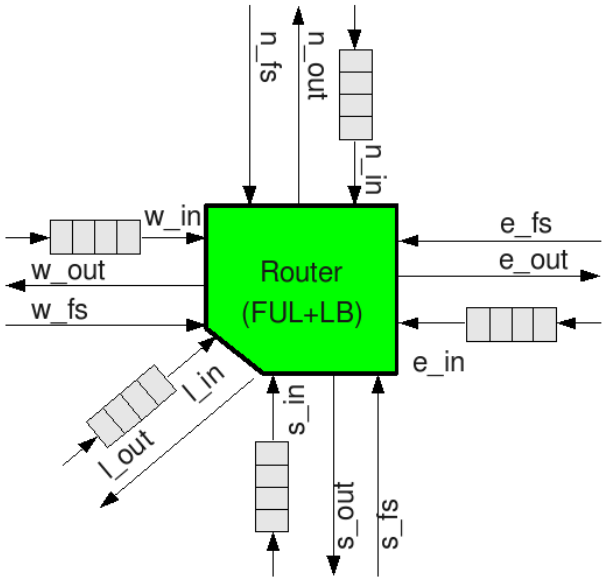
Load Balancing based Strategies

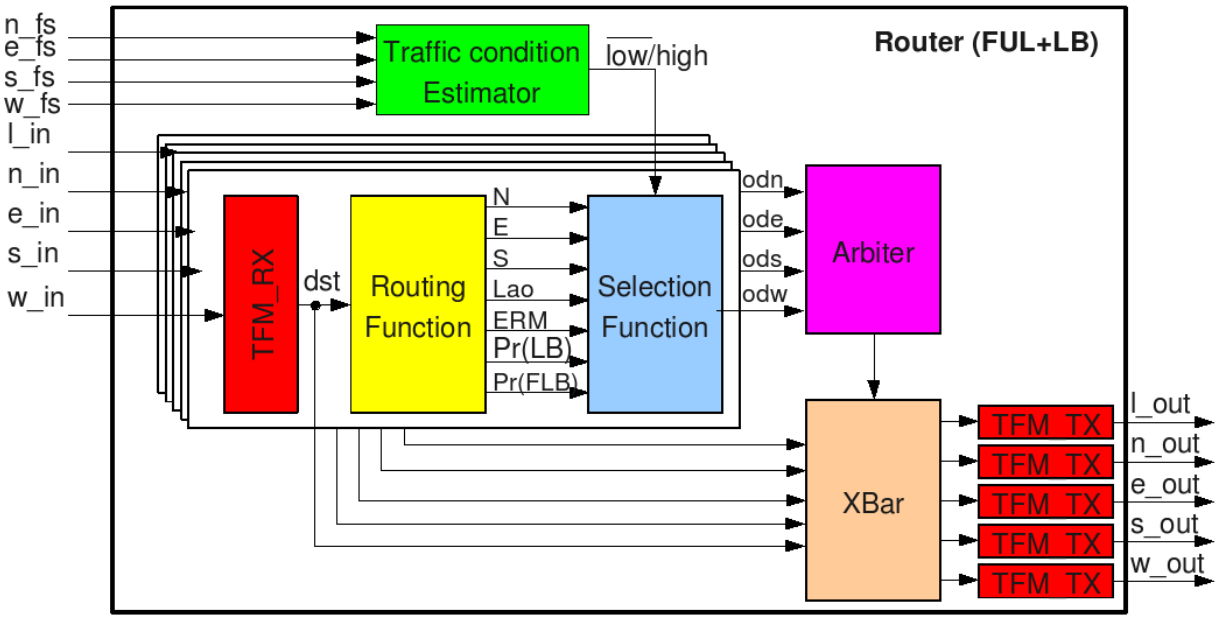
- Fault Elimination + LB (**FE+LB**)
  - ➔ Selection function based on the selection probabilities computed resolving the LB problem ($Pr^{(LB)}$)
- Partially Faulty Links usage strategy + LB (**FU+LB**)
  - ➔ In *low traffic* conditions
    - ✔ Selection function uses $Pr^{(LB)}$
  - In *high traffic* conditions
    - $Pr^{(FLB)} = Pr^{(LB)} \sqrt{Pr^{(F)}}$
- Partially Faulty Links usage with Look-ahead strategy + LB (**FUL+LB**)
  - ➔ In *low traffic* conditions
    - ✔ Selection function uses $Pr^{(LB)}$ between AOs where ERM is set
  - In *high traffic* conditions
    - Like FUL+LB

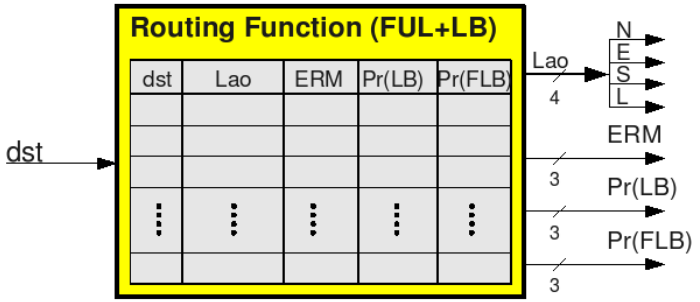
Entry in Routing Table

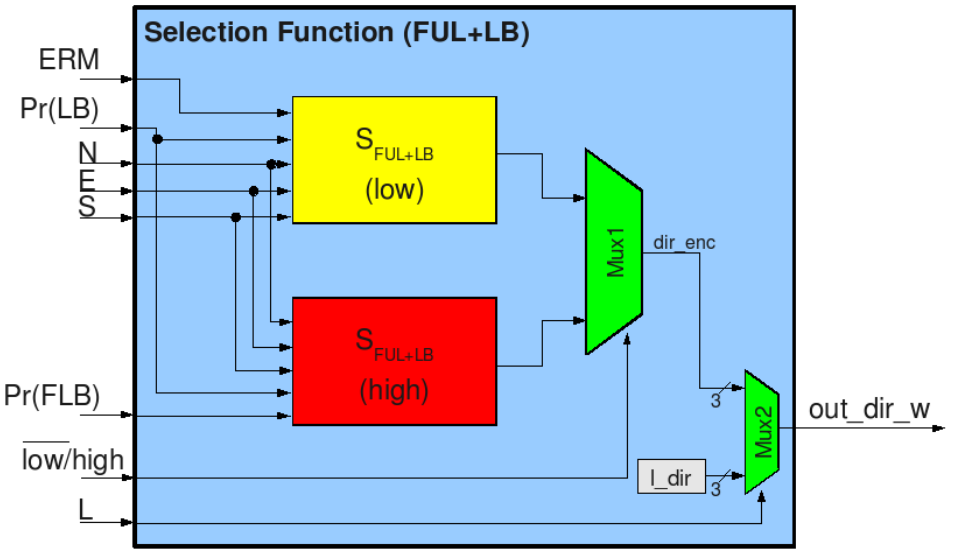


Router Architecture (FUL+LB)

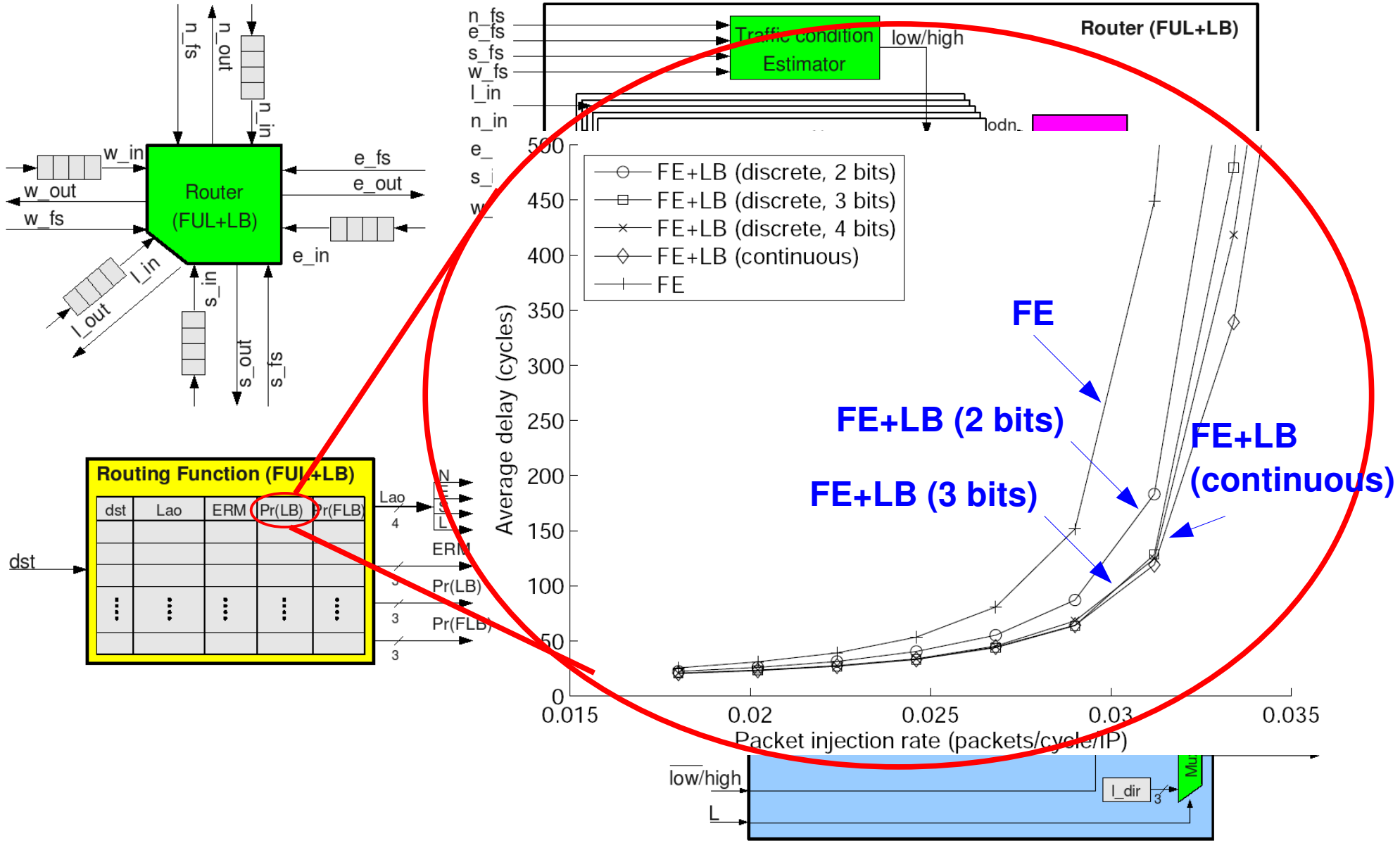






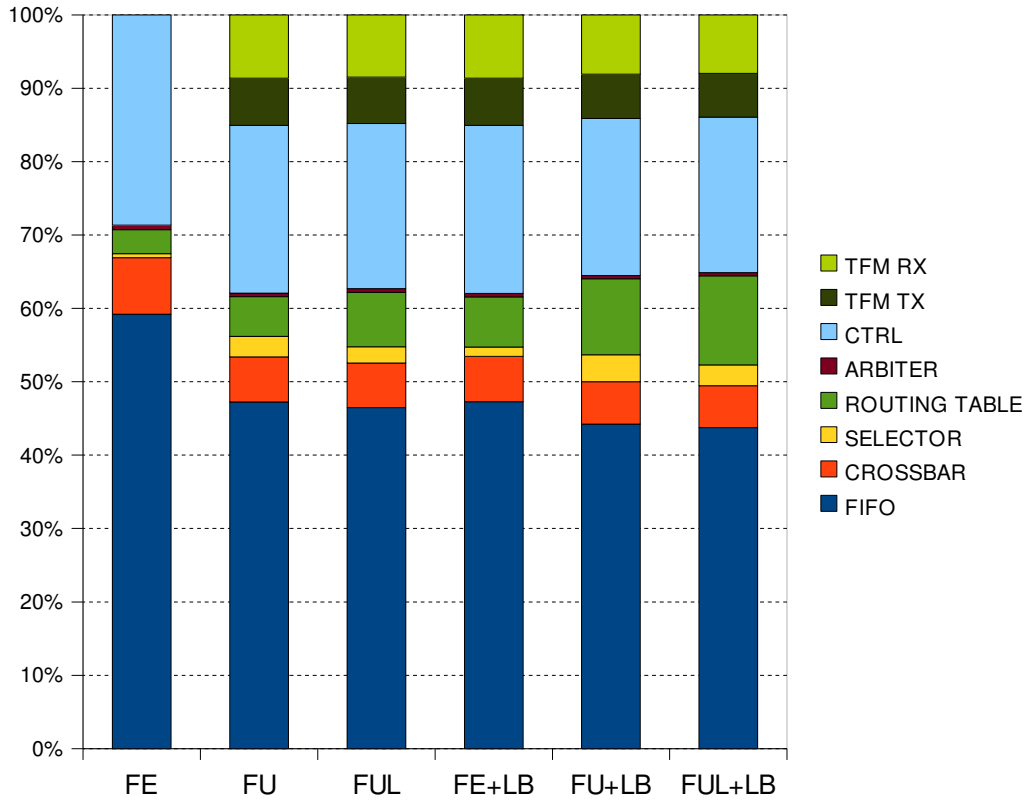


Router Architecture (FUL+LB)

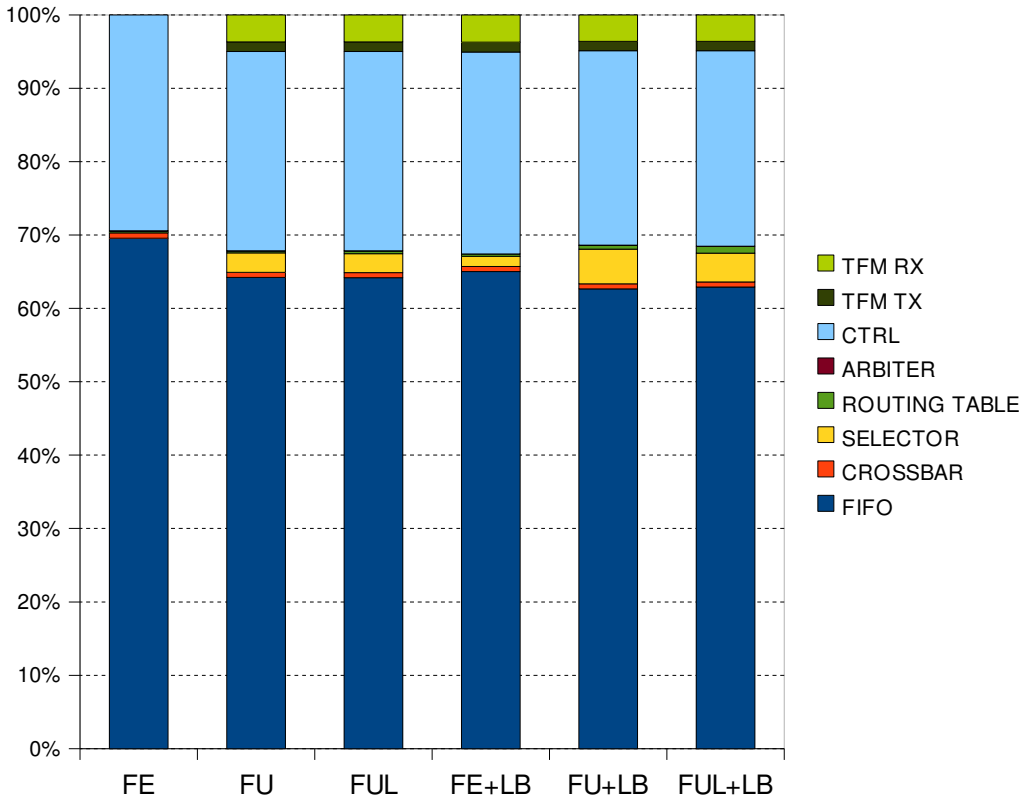


Implication on Router Design

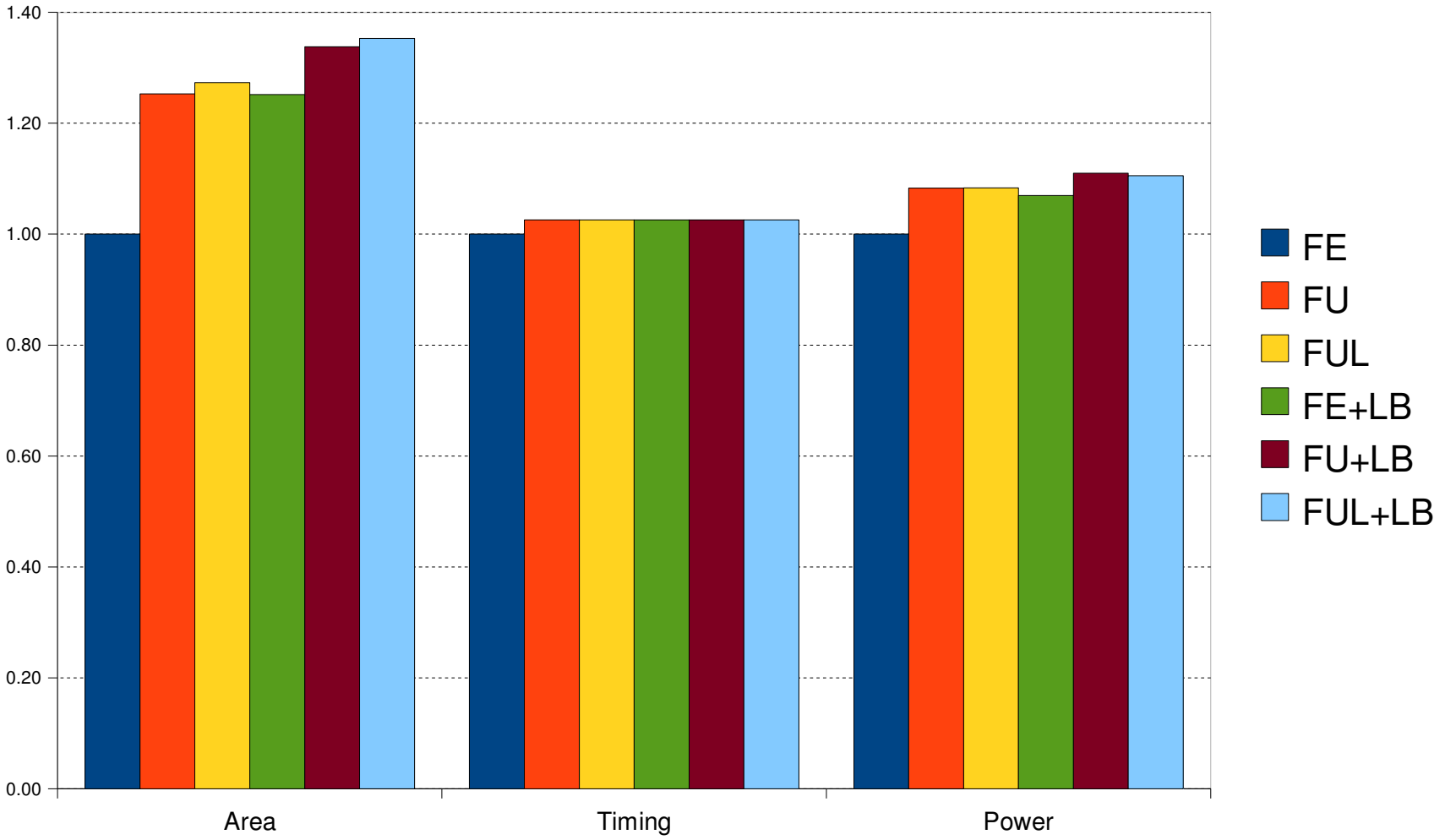
Area Breakdown



Power Breakdown

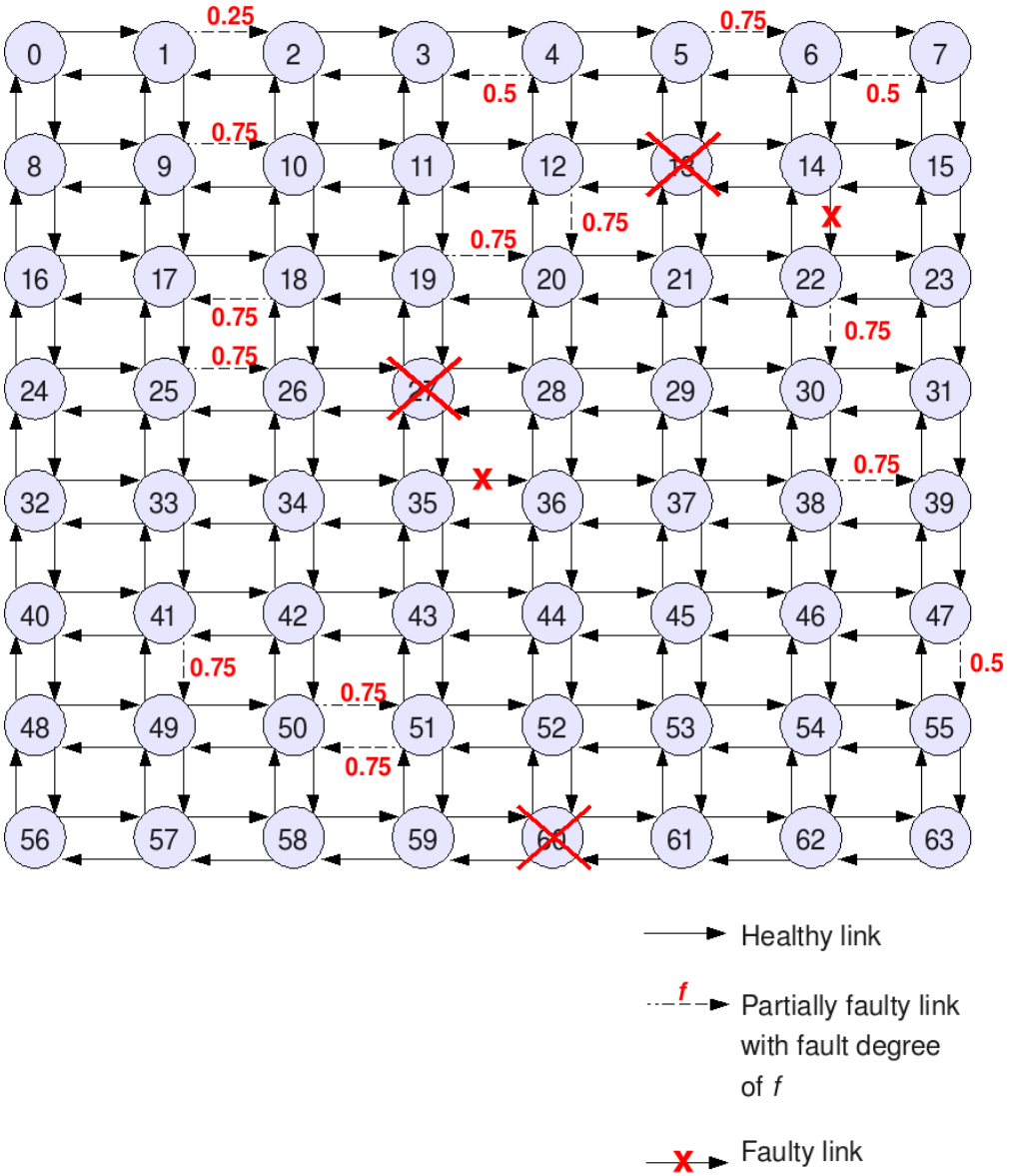


Implication on Router Design



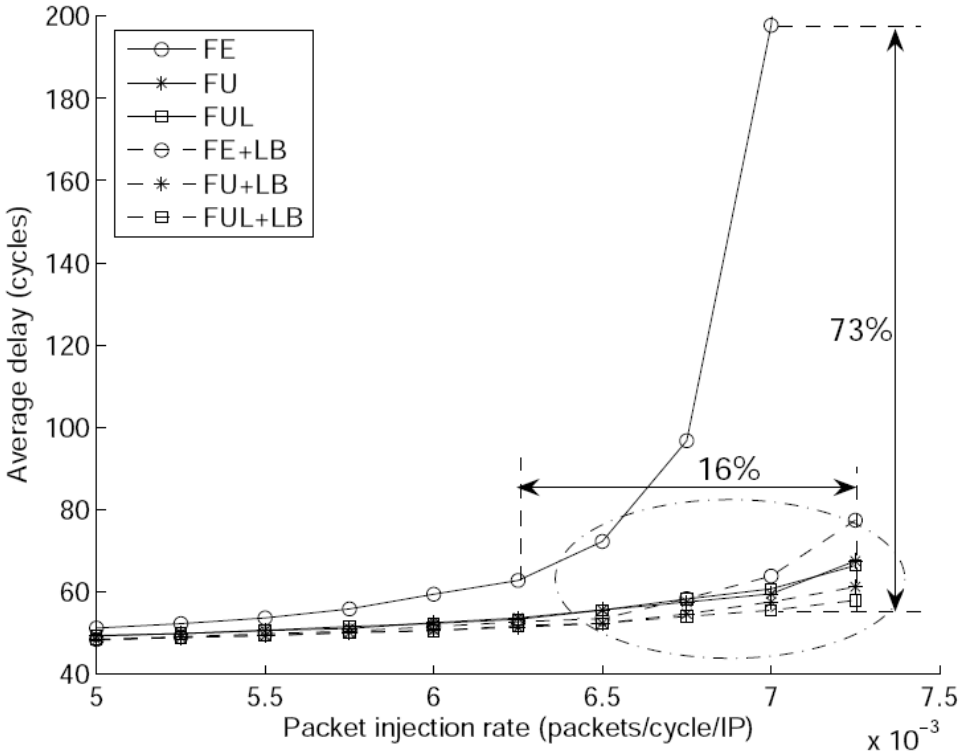
Performance Evaluation

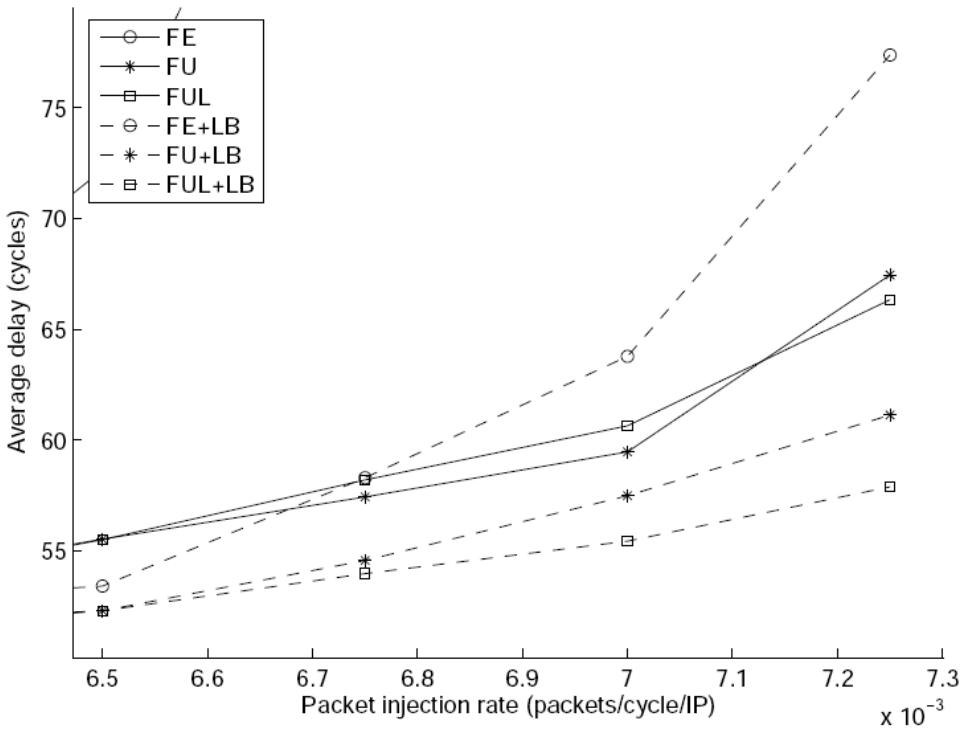
- Simulation platform: *Noxim*
- Traffic scenarios: Uniform, transpose, bit-reversal, butterfly, shuffle
- 8x8 mesh-based NoC architecture
  - ➔ Buffers: 4 flits
  - ➔ Packet size: random 2-16 flits
  - ➔ Poisson packet injection distribution
  - ➔ Simulation time: 100,000 clock cycles (warm-up session: 10,000 clock cycles)



Delay Variation

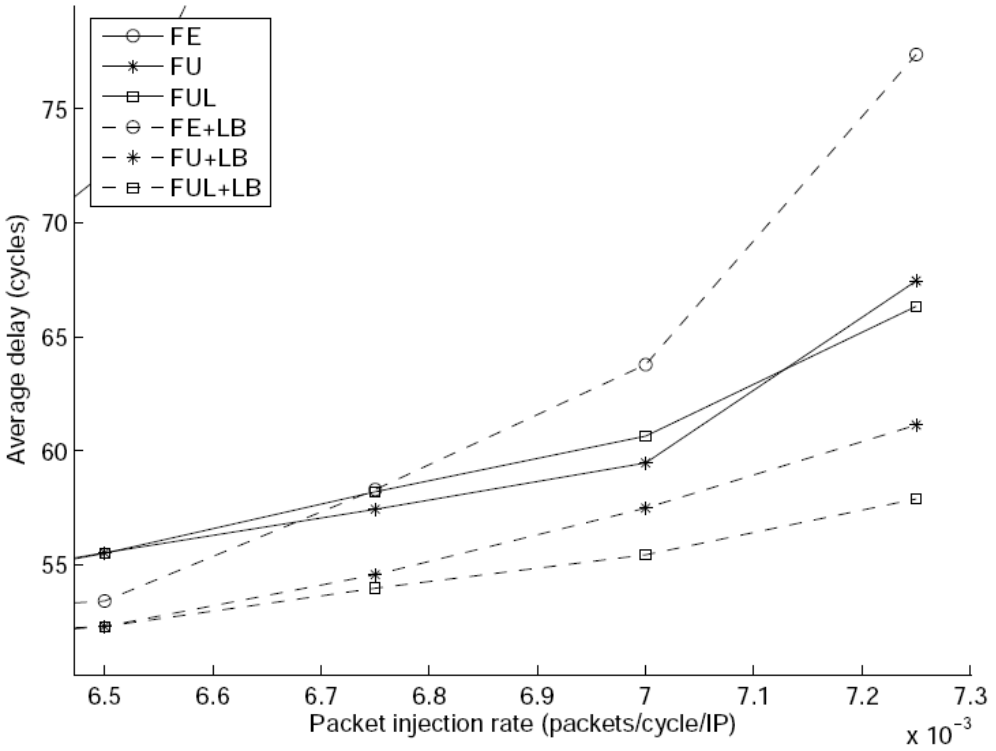
Delay variation under *uniform* traffic

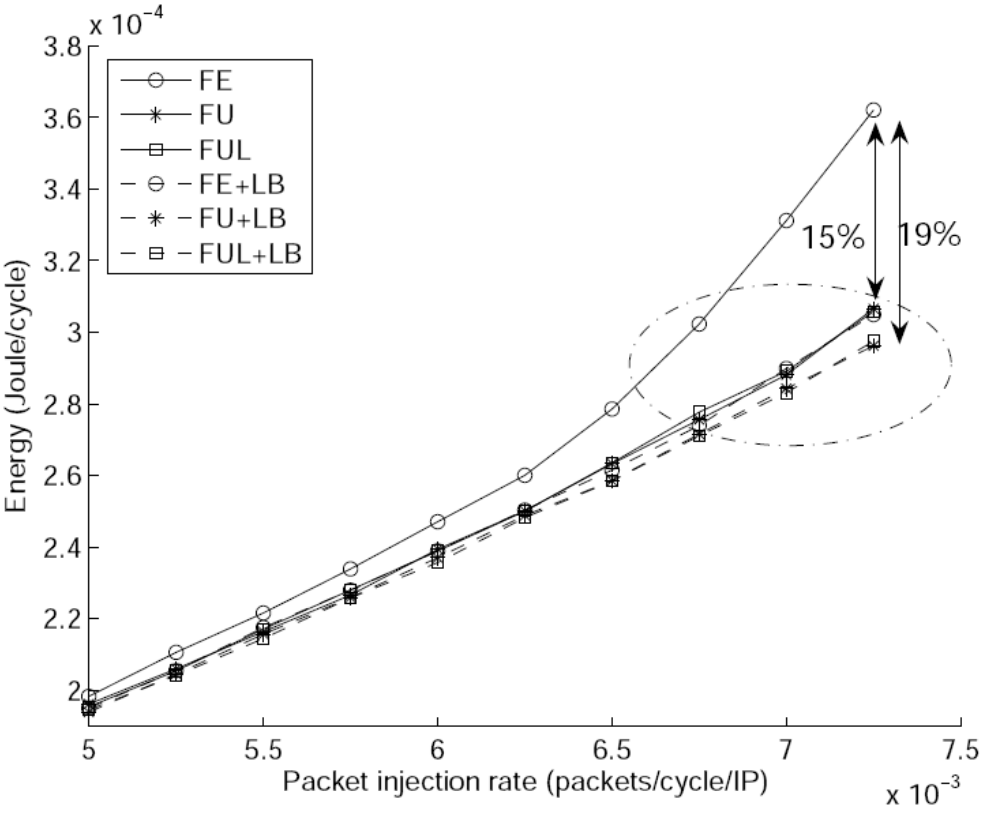




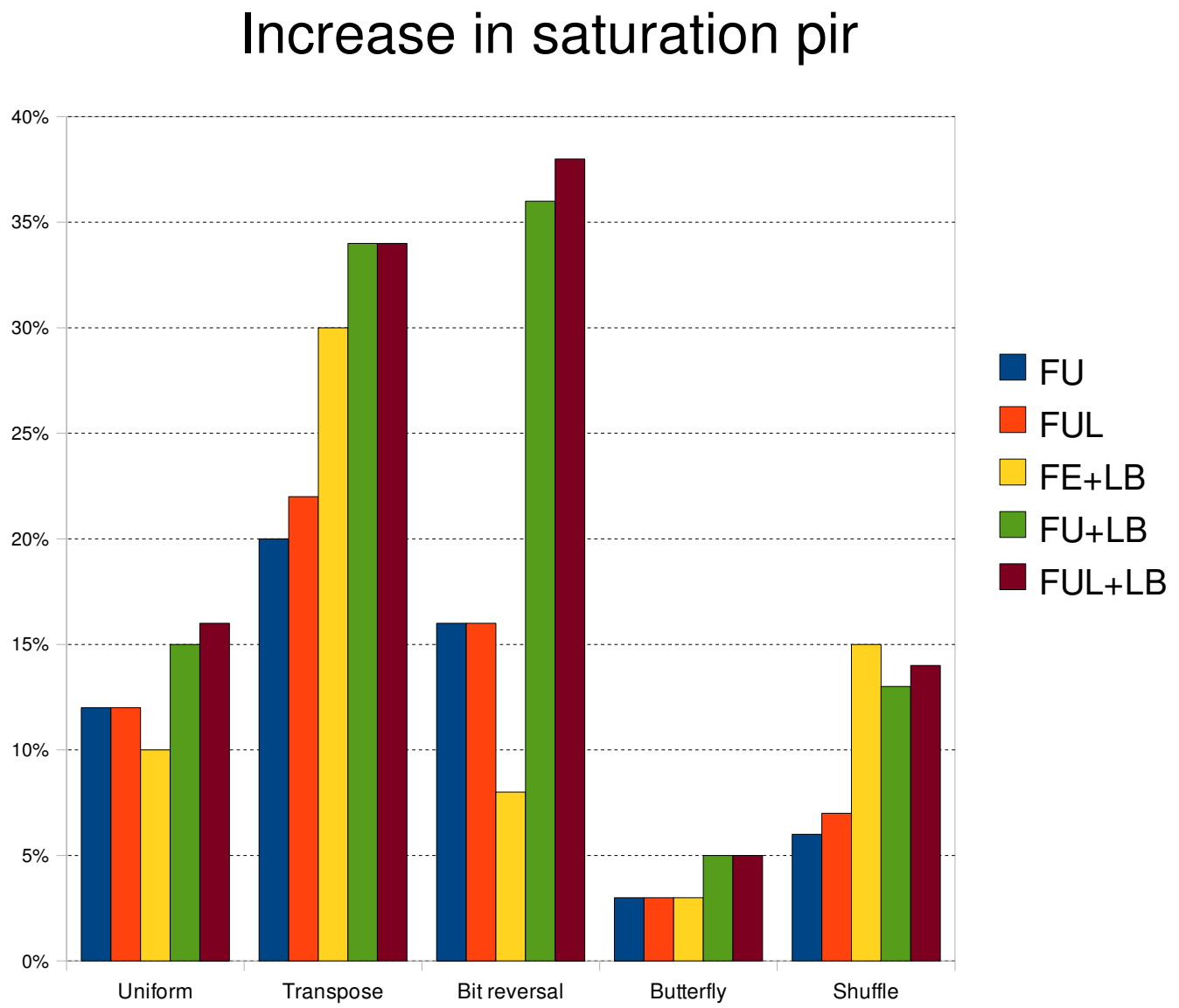
Energy Variation

Energy variation under *uniform* traffic

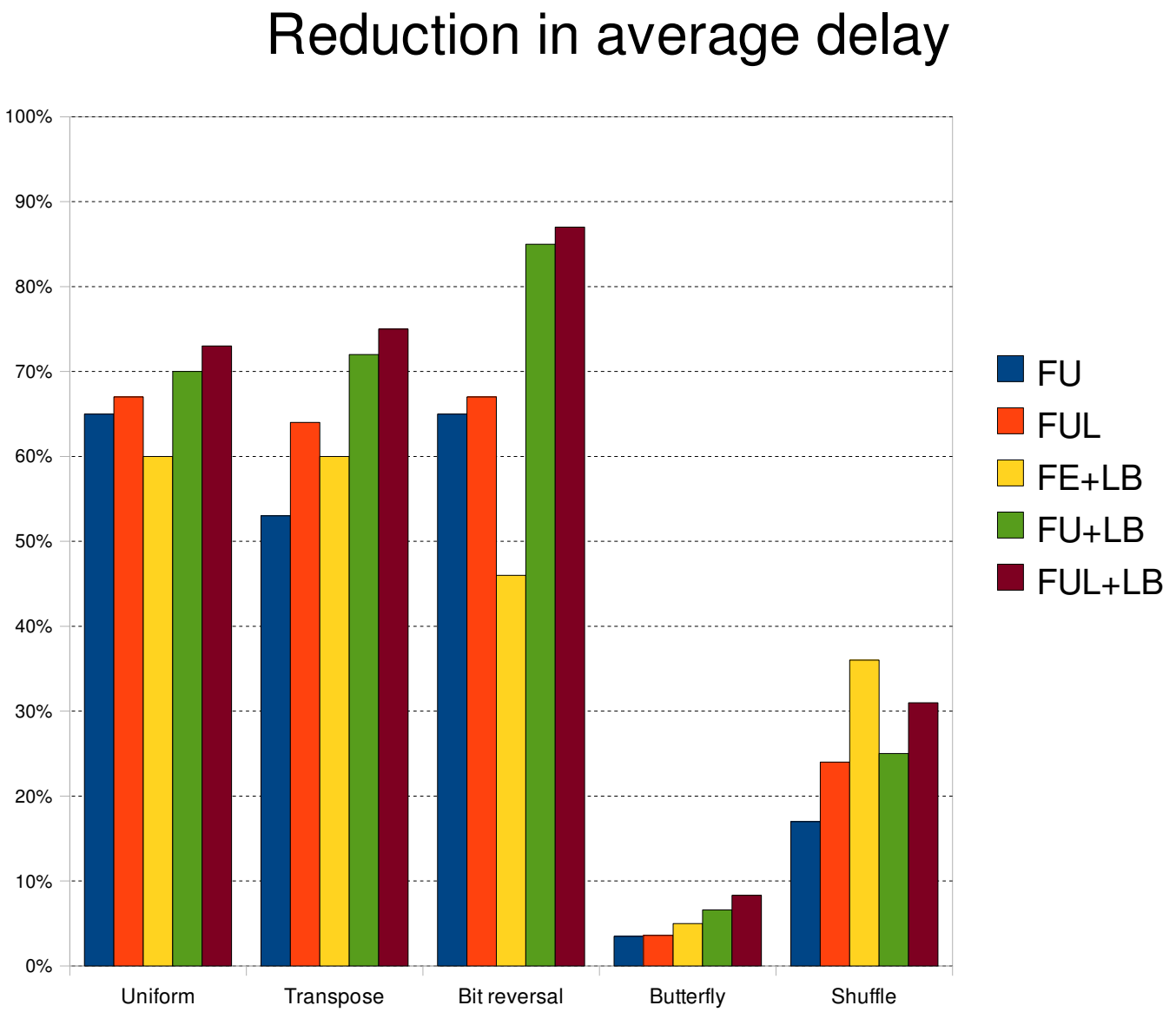




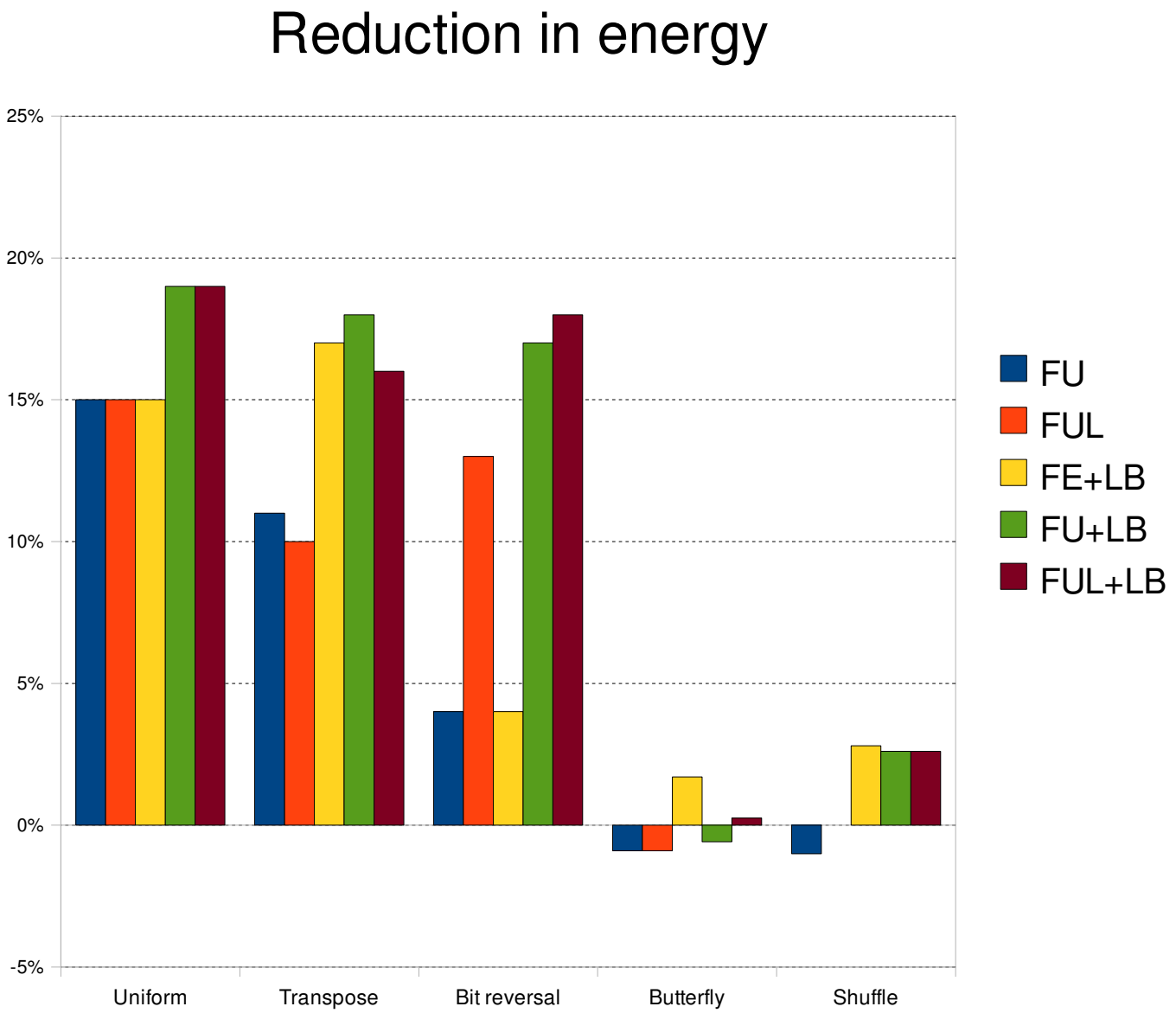
Improvement in Saturation *pir*



Improvement in Average Delay

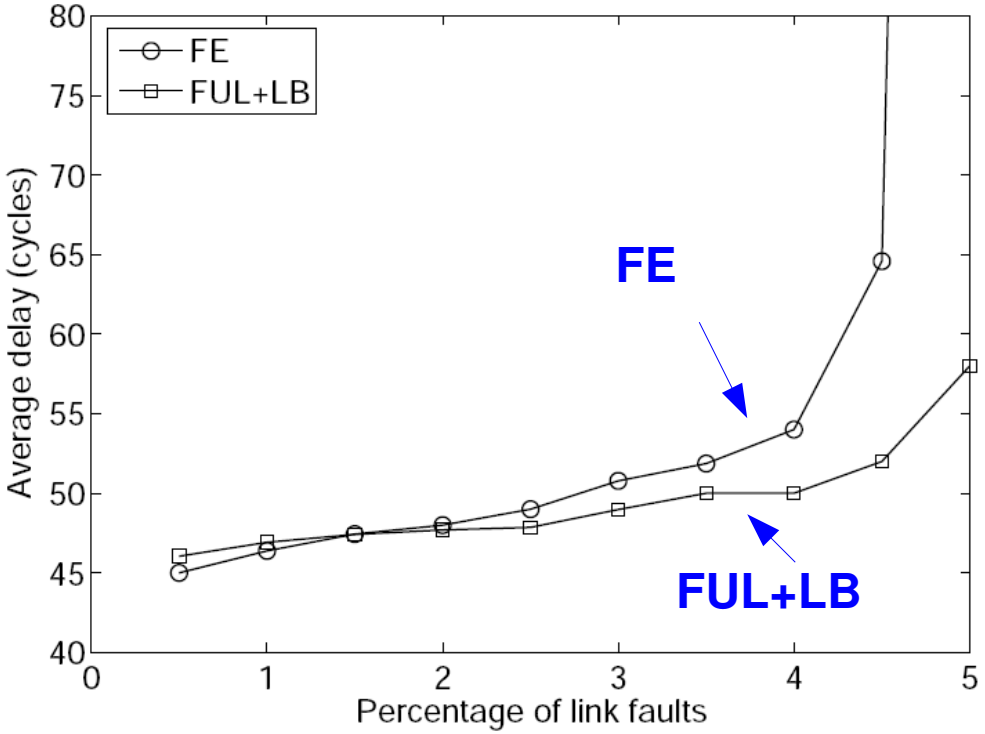


Reduction in Energy

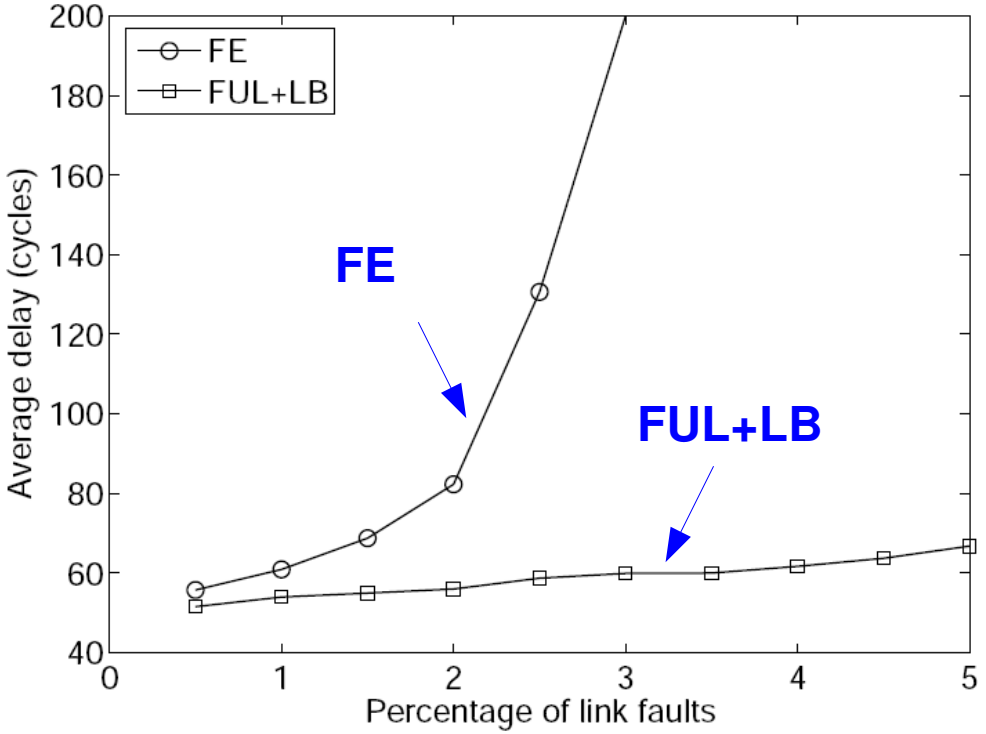


Delay vs. Percentage of Link Faults

Faults random distributed



Faults random clustered



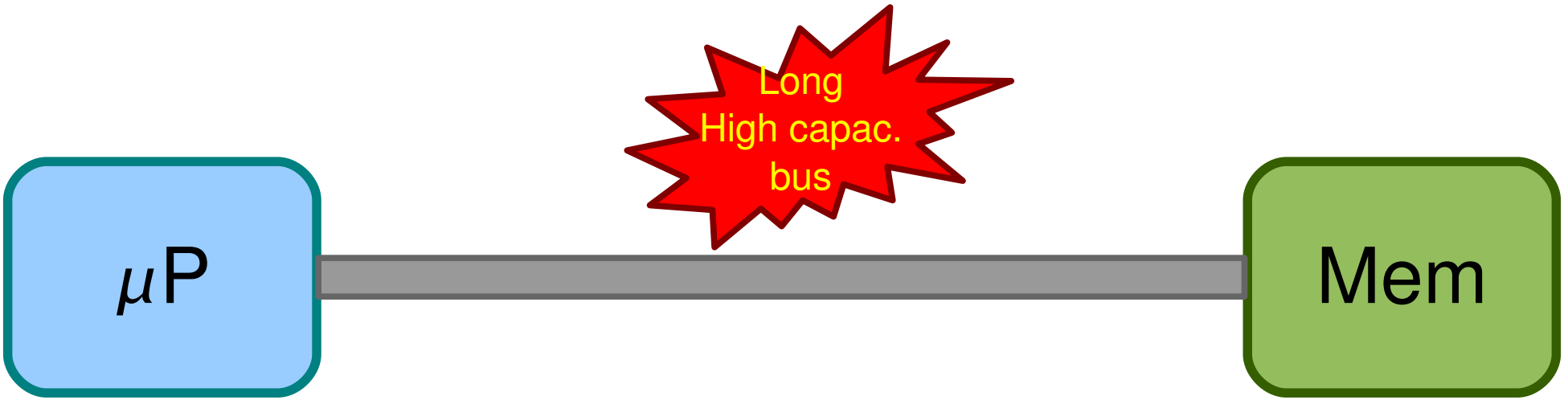
Outline

- Application Specific Routing Algorithms ✓
- Concurrent Mapping and Routing ✓
- Dealing with Manufacturing Defects ✓
- Encoding Scheme for Low Power

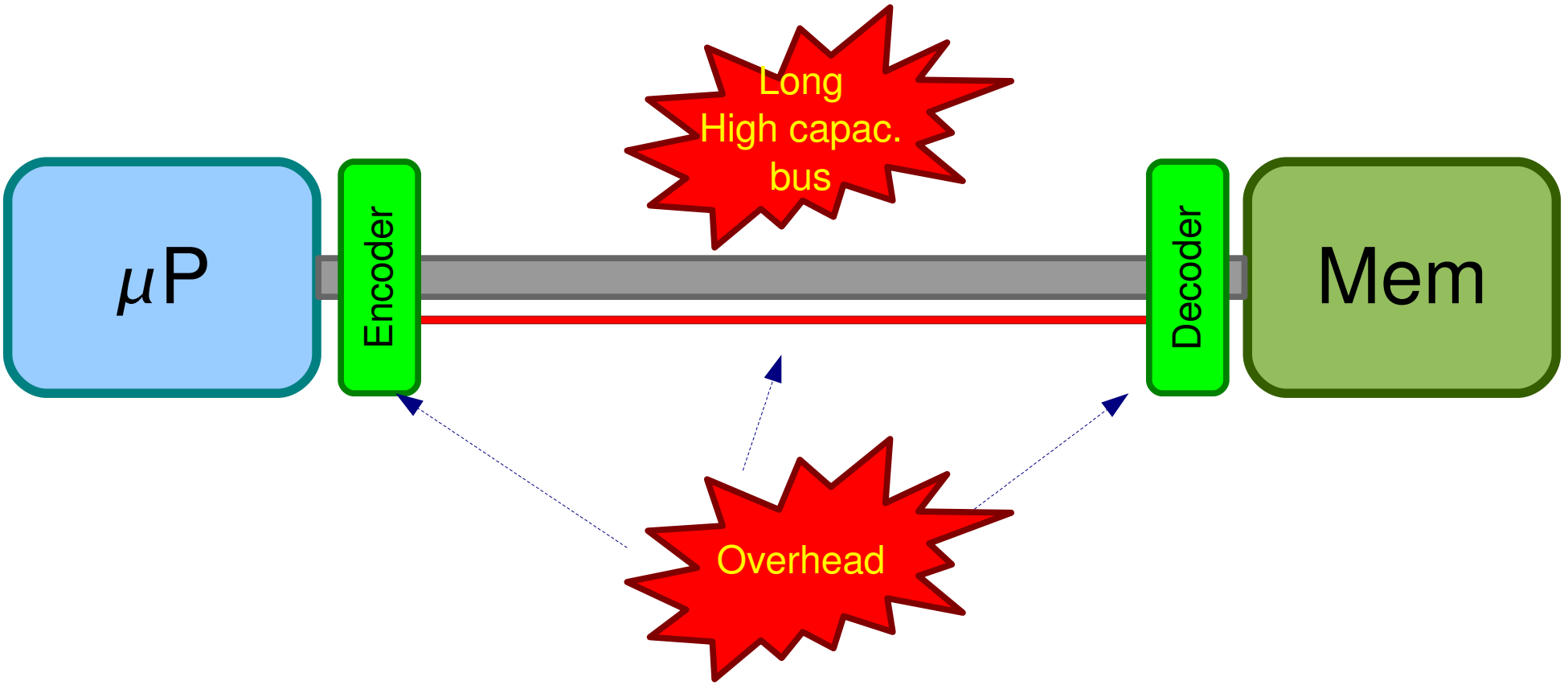
Motivations

- The interconnect system is one of the main elements which characterizes the system in terms of both power dissipation and energy consumption
  - ➔Approx 28% in the Intel's 80-tiles TeraFLOPS
- As technology shrinks, the power ratio between NoC links and routers increases
  - ➔Links are becoming more power hungry than routers

General Scheme – bus-based Archs



General Scheme – bus-based Archs

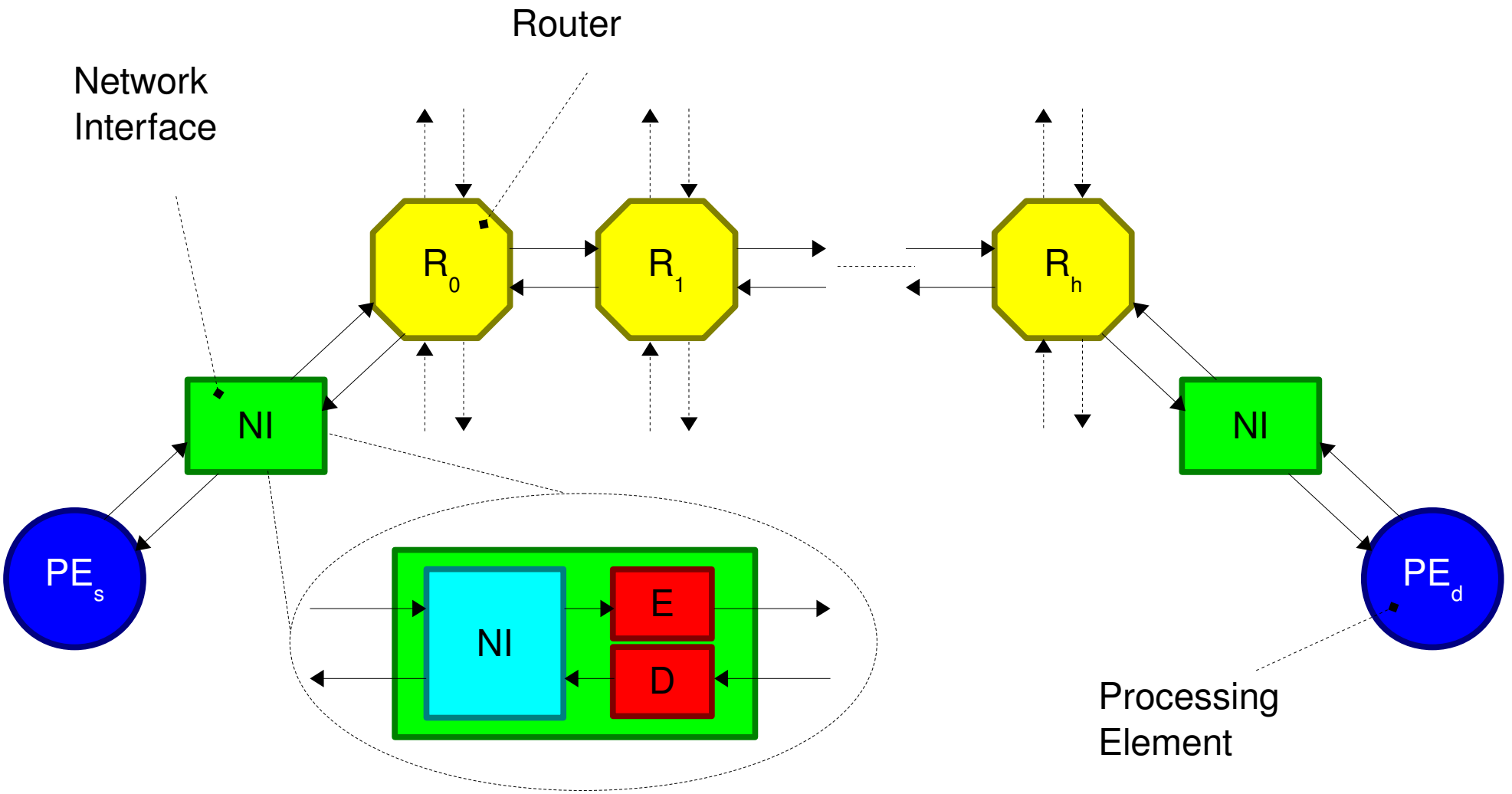


Encoding Schemes

- Applied in the context of bus-based architectures
- Bus-invert method [Stan and Burleson, TVLSI'95]
- Gray code [Su *et al.*, D&T'94]
- T0 method [Benini *et al.*, GLS-VLSI'97]
- Working-zone encoding [Mussoll *et al.*, PDAW'98]
- …
- Do not take into account coupling effects

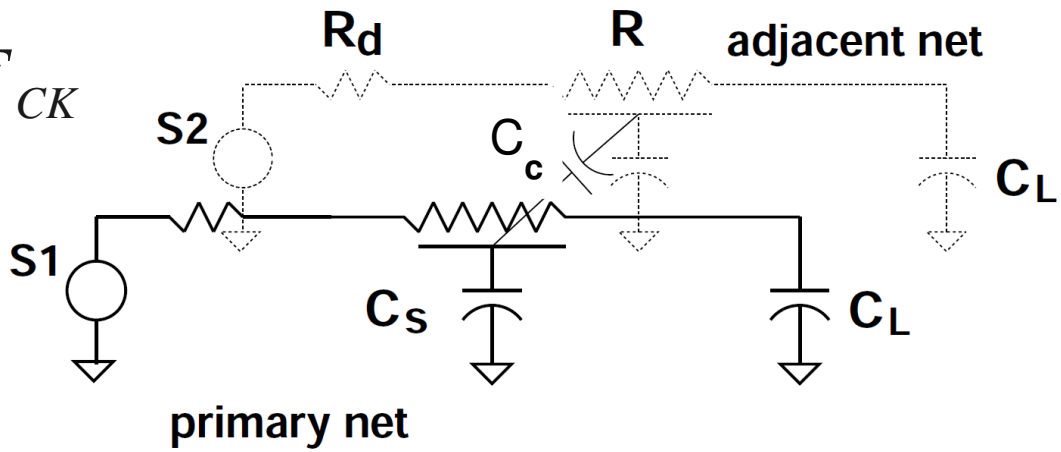
  ➔Dominant in DSM regime

General Scheme – NoC Archs

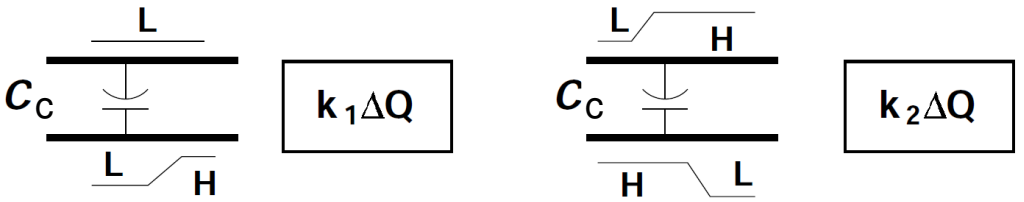


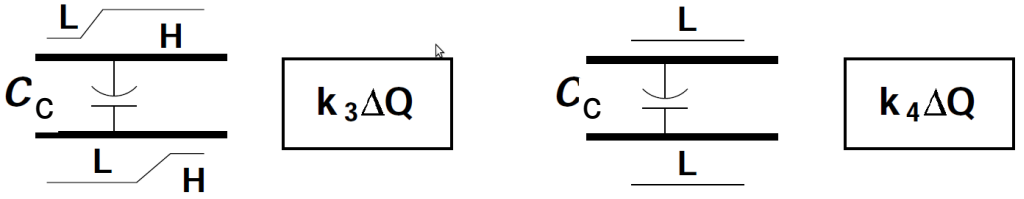
Power Model

$$P = [T_{0\to1}(C_s + C_l) + T_c C_c] V_{dd}^2 F_{CK}$$



$$T_c = k_1 T_1 + k_2 T_2 + k_3 T_3 + k_4 T_4$$

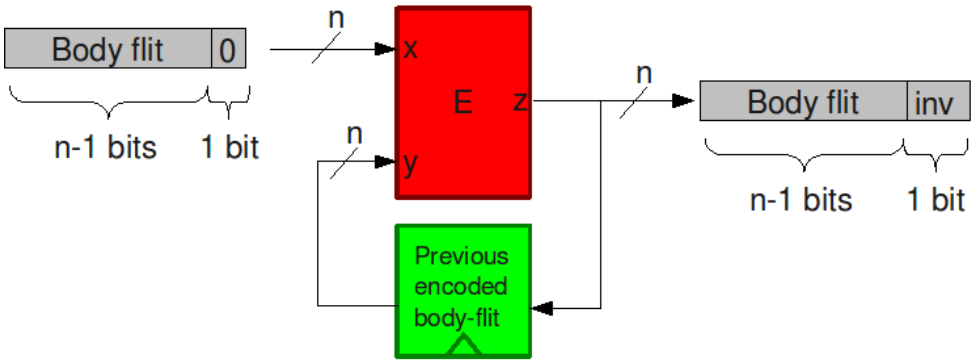


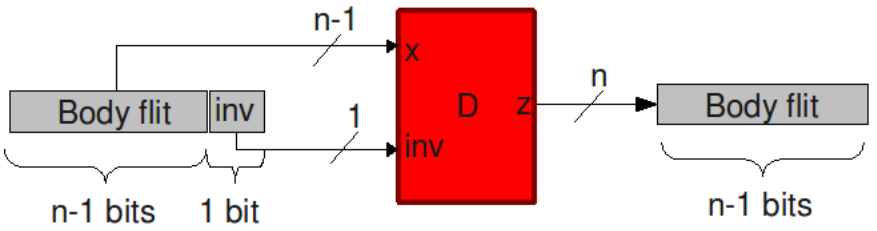


Proposed Scheme (1/2)

$$P \propto T_{0\to1} C_s (k_1 T_1 + k_2 T_2 + k_3 T_3 + k_4 T_4) C_c$$

$$P' \propto T'_{0\to1} C_s (k_1 T'_1 + k_2 T'_2 + k_3 T'_3 + k_4 T'_4) C_c$$





- Invert if $P > P'$

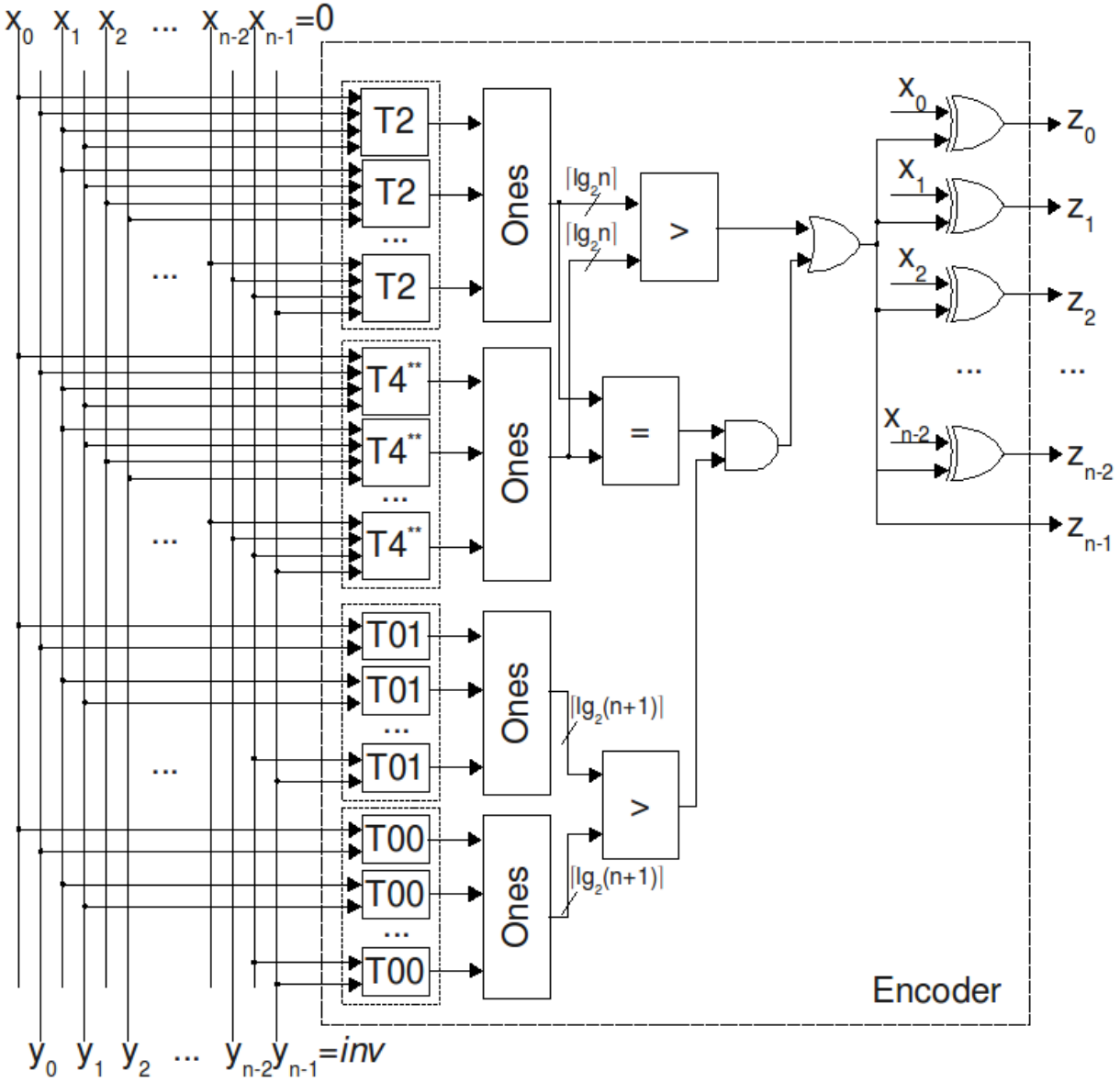
Proposed Scheme (2/2)

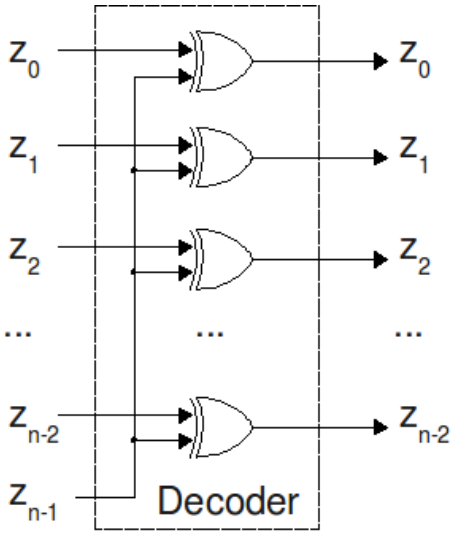
Time	Normal				Inverted			
	Type I				Type I			
$t-1$	00	00	11	11	00	00	11	11
t	01	10	01	10	10	01	10	01
	Type II				Type IV			
$t-1$	01	10			01	10		
t	10	01			01	10		
	Type III				Type IV			
$t-1$	00	11			00	11		
t	11	00			00	11		
	Type IV				Type II and III			
$t-1$	00	11	01	10	00	11	01	10
t	00	11	01	10	11	00	10	01
	T_4^*		T_4^{**}		T_3		T_2	

- Invert if $P > P'$

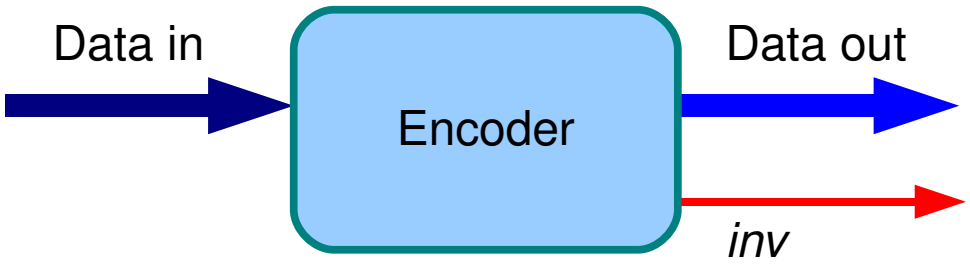
$$T_{0\to 1} + 8T_2 > T_{0\to 0} + 8T_4^{**}$$

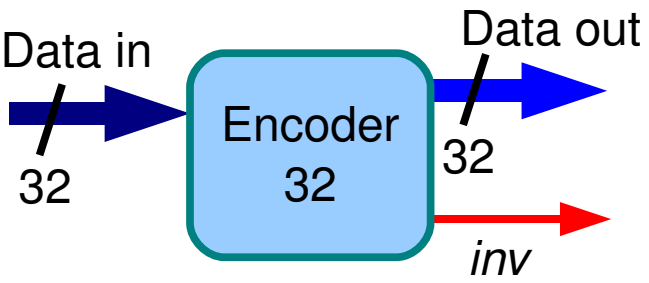
Encoder and Decoder

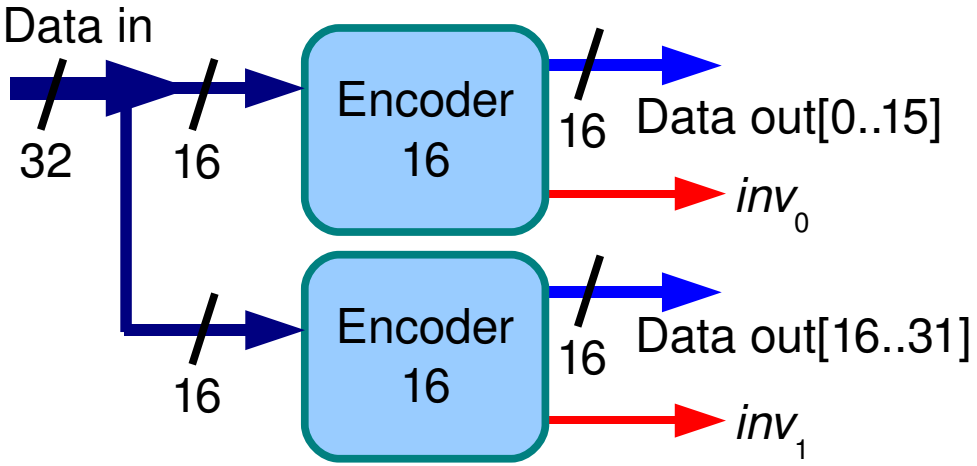


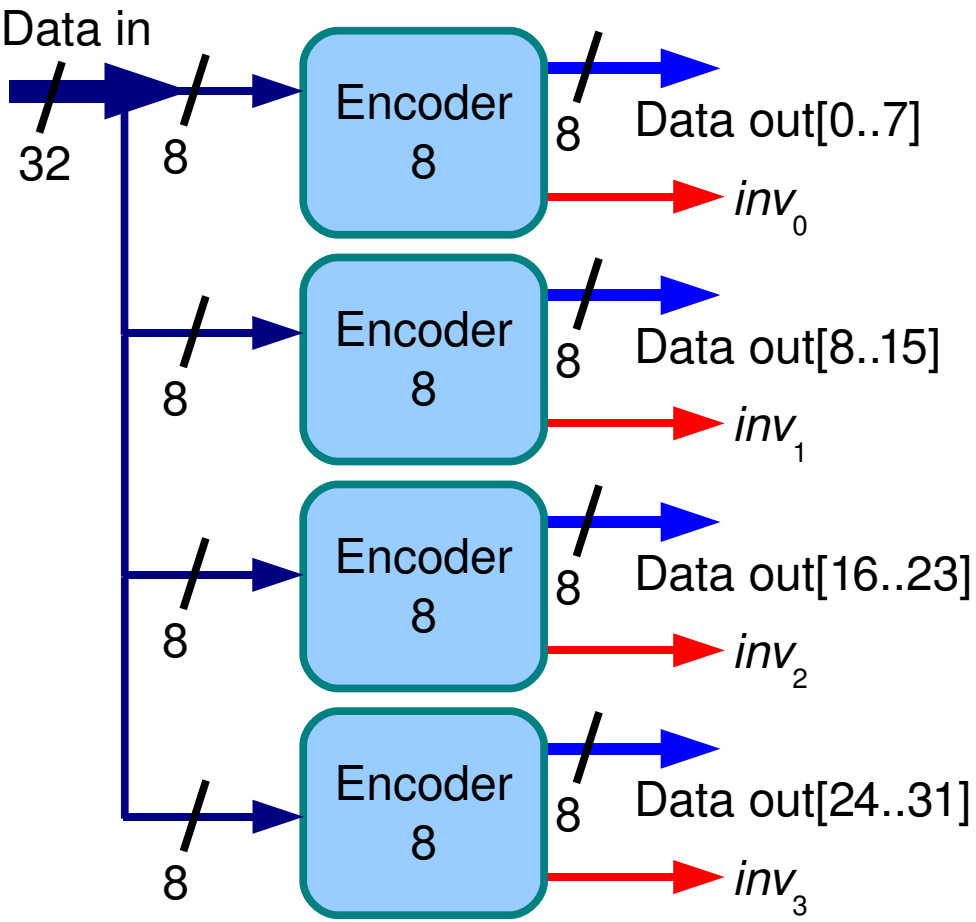


Partitions

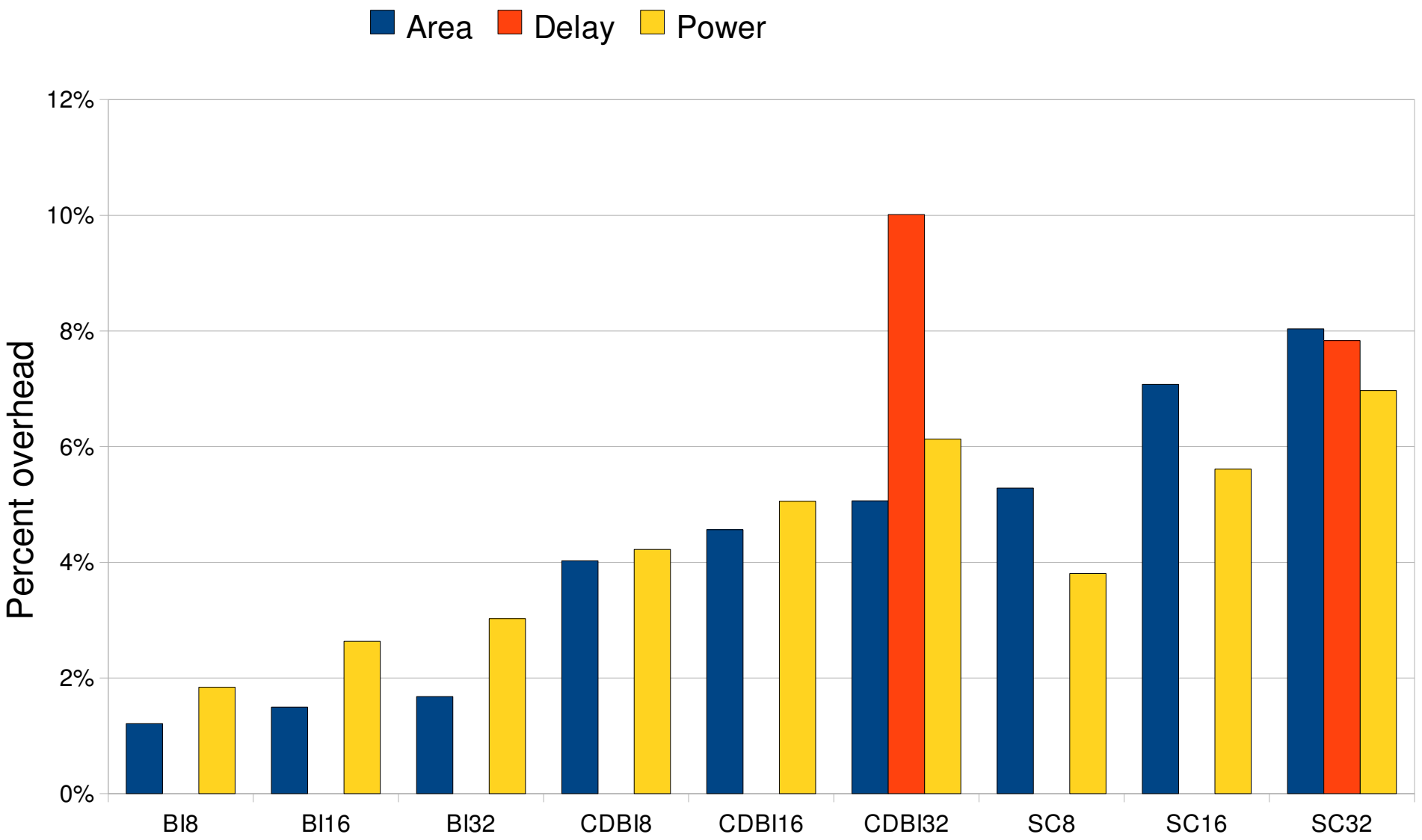

Data in
Encoder
Data out
inv


Data in
32
Encoder
32
Data out
32
inv

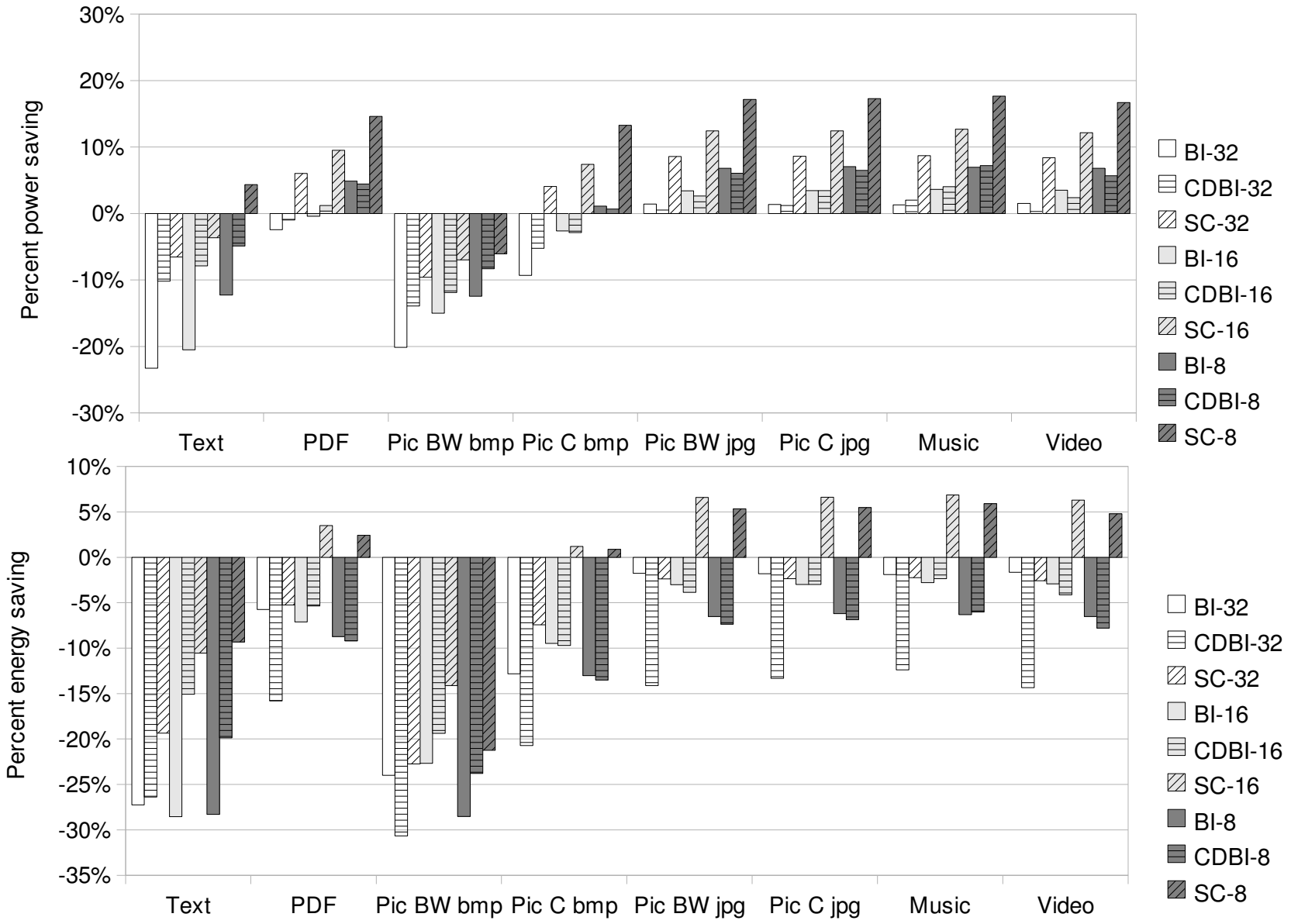

Data in
32
16
Encoder
16
16
Data out[0..15]
inv0
16
Encoder
16
16
Data out[16..31]
inv1


Data in
32
8
Encoder
8
8
Data out[0..7]
inv0
8
Encoder
8
8
Data out[8..15]
inv1
8
Encoder
8
8
Data out[16..23]
inv2
8
Encoder
8
8
Data out[24..31]
inv3

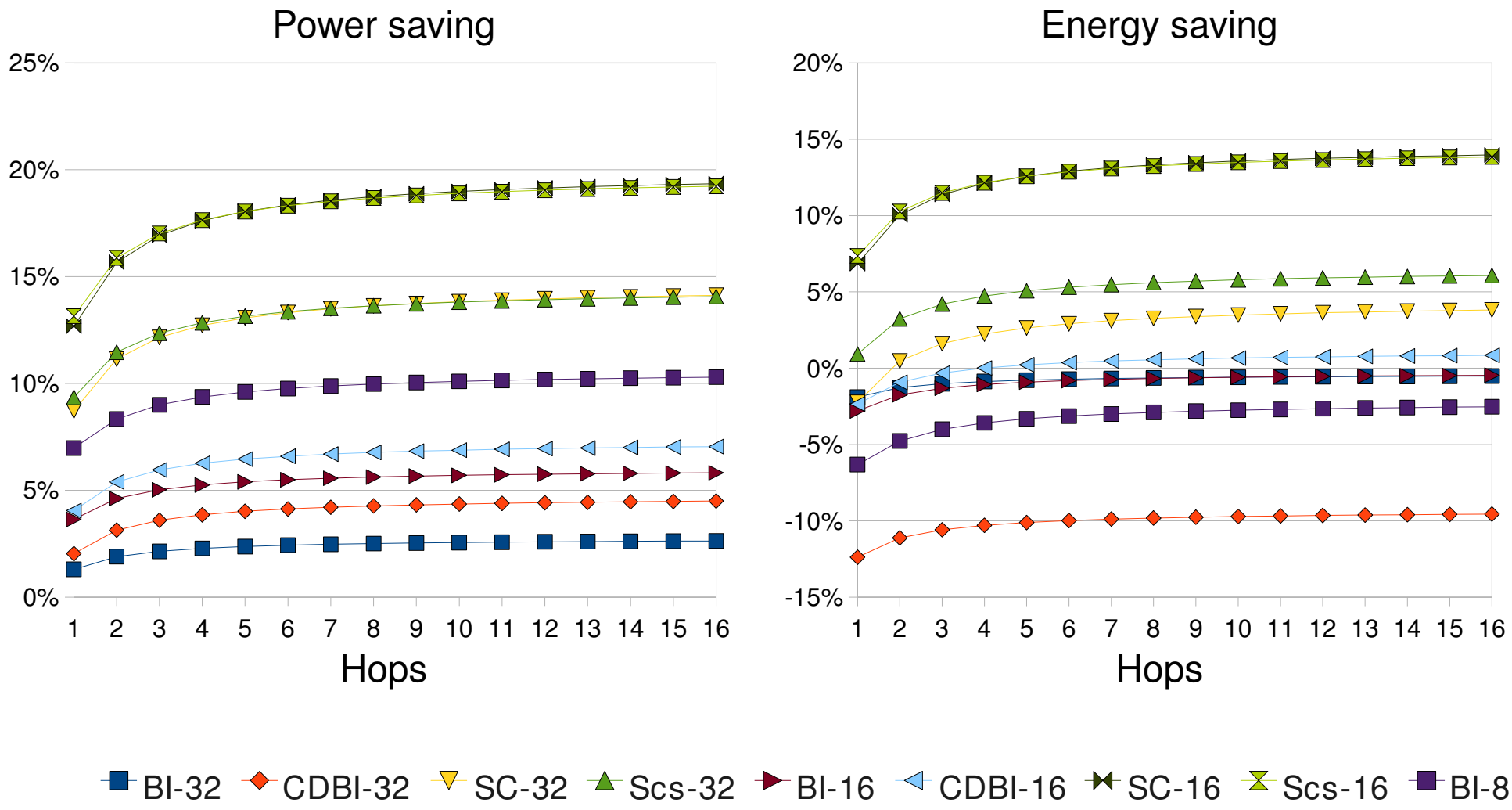
Overhead


Area
Delay
Power
12%
10%
8%
6%
4%
2%
0%
Percent overhead
BI8
BI16
BI32
CDBI8
CDBI16
CDBI32
SC8
SC16
SC32

Power and Energy Saving



Saving *vs.* Path Length



Outline

- Application Specific Routing Algorithms ✓
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References (1/3)

- M. Palesi, R. Holsmark, S. Kumar, V. Catania. Application Specific Routing Algorithms for Networks on Chip. IEEE Transactions on Parallel and Distributed Systems, 20(3), pp. 316-330, March 2009.
- A. Mejia, M. Palesi, J. Flich, S. Kumar, P. Lopez, R. Holsmark and J. Duato. Region-Based Routing: A Mechanism to Support Efficient Routing Algorithms in NoCs IEEE Transactions on on Very Large Scale Integration Systems, 17(3), pp. 356-369, March 2009.
- G. Ascia, V. Catania, M. Palesi, D. Patti. Implementation and Analysis of a New Selection Strategy for Adaptive Routing in Networks-on-Chip. IEEE Transactions on Computers, 57(6), pp. 809-820, June 2008.
- R. Holsmark, M. Palesi, S. Kumar. Deadlock free Routing Algorithms for Irregular Mesh Topology NoC Systems with Rectangular Regions. Journal of Systems Architecture, 54/3-4 (2008) pp. 427-440.
- D. Bertozzi, S. Kumar, M. Palesi. Networks-on-Chip: Emerging Research Topics and Novel Ideas. VLSI Design, vol. 2007, Article ID 26454, doi:10.1155/2007/26454.
- G. Ascia, V. Catania, M. Palesi. A Multi-objective Genetic Approach to Mapping Problem on Network-on-Chip. Journal of Universal Computer Science, 12(4):370--394, 2006.
- G. Ascia, V. Catania, M. Palesi. Mapping Cores on Network-on-Chip. International Journal of Computational Intelligence Research (IJCIR), ISSN 0972-9836, 1(1-2):109--126, 2005.
- M. Palesi, F. Fazzino, G. Ascia, V. Catania. Data Encoding for Low-Power in Wormhole-Switched Networks-on-Chip. To appear in The 12th Euromicro Conference on Digital System Design (DSD), 27-29 Aug 2009, Patras, Greece.
- R. Tornero, V. Sterrantino, M. Palesi, J. M. Orduna. A Multi-objective Strategy for Concurrent Mapping and Routing in Networks on Chip. To appear in The 12th International Workshop on Nature Inspired Distributed Computing held in conjunction with The 23th IEEE/ACM International Parallel and Distributed Processing, May 25-28, 2009, Rome, Italy.
- R. Holsmark, M. Palesi, S. Kumar, A. Mejia. HiRA: A Methodology for Deadlock Free Routing in Hierarchical Networks on Chip. 3rd ACM/IEEE International Symposium on Networks on Chip. May 10-13, 2009, San Diego, CA

References (2/3)

- D. Frazzetta, G. Dimartino, M. Palesi, S. Kumar, V. Catania. Efficient Application Specific Routing Algorithms for NoC Systems utilizing Partially Faulty Links. 11th EUROMICRO Conference on Digital System Design, Architectures, Methods and Tools, pp. 18-25, Sep. 3-5, 2008, Parma, Italy.
- R. Tornero, J. M. Orduna, M. Palesi, J. Duato. A Communication-Aware Topological Mapping Technique for NoCs. International Conference on Parallel and Distributed Computing, pp. 910-919, August 26-29th, 2008, Las Palmas de Gran Canaria, Spain.
- M. Palesi, G. Longo, S. Signorino, S. Kumar, R. Holsmark, V. Catania. Design of Bandwidth Aware and Congestion Avoiding Efficient Routing Algorithms for Networks-on-Chip Platforms. IEEE International Symposium on Networks-on-Chip, pp. 97-106, 7th-11th April 2008, Newcastle University, UK.
- G. Longo, S. Signorino, M. Palesi, S. Kumar, R. Holsmark, V. Catania. Bandwidth Aware Routing Algorithms for Networks-on-Chip. 2nd Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip. Goteborg, Sweden, January 27, 2008.
- R. Tornero, J. M. Orduna, M. Palesi, J. Duato. A Communication-Aware Task Mapping Technique for NoCs. 2nd Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip. Goteborg, Sweden, January 27, 2008.
- M. Palesi, S. Kumar, R. Holsmark, V. Catania. Exploiting Communication Concurrency for Efficient Deadlock Free Routing in Reconfigurable NoC Platforms. IEEE International Parallel and Distributed Processing Symposium, pp. 1-8, Long Beach, CA, March 2007.
- G. Ascia, V. Catania, M. Palesi, D. Patti. Neighbors-on-Path: A New Selection Strategy for On-Chip Networks. Fourth IEEE Workshop on Embedded Systems for Real Time Multimedia, pp. 79-84. Seoul, Korea, October 26-27, 2006.
- M. Palesi, R. Holsmark, S. Kumar, V. Catania. A Methodology for Design of Application Specific Deadlock-free Routing Algorithms for NoC Systems. International Conference on Hardware-Software Codesign and System Synthesis, pp. 142-147. Seoul, Korea, October 22-25, 2006.
- R. Holsmark, M. Palesi, S. Kumar. Deadlock Free Routing Algorithms for Mesh Topology NoC Systems with Regions. DSD 2006, 9th EUROMICRO Conference on Digital System Design, Architectures, Methods and Tools, pp. 696-703. Croatia, Sept 2006.

References (3/3)

- M. Palesi, S. Kumar, R. Holsmark. A Method for Router Table Compression for Application Specific Routing in Mesh Topology NoC Architectures. SAMOS VI Workshop: Embedded Computer Systems: Architectures, Modeling, and Simulation, pp. 373-384. Samos, Greece, July 17-20, 2006.
- G. Ascia, V. Catania, M. Palesi, D. Patti. A New Selection Policy for Adaptive Routing in Network on Chip. International Conference on Electronics, Hardware, Wireless and Optical Communications. Madrid, Spain, February 15-17, 2006.
- G. Ascia, V. Catania, M. Palesi. An Evolutionary Approach to Network-on-Chip Mapping Problem. IEEE Congress on Evolutionary Computation. Edinburgh, UK, September 2nd-5th, 2005.
- G. Ascia, V. Catania, M. Palesi. Multi-objective Mapping for Mesh-based NoC Architectures. In Second IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, pages 182--187, Stockholm, Sweden, Sept. 8-10, 2004.