
VLSI Design Automation

Maurizio Palesi

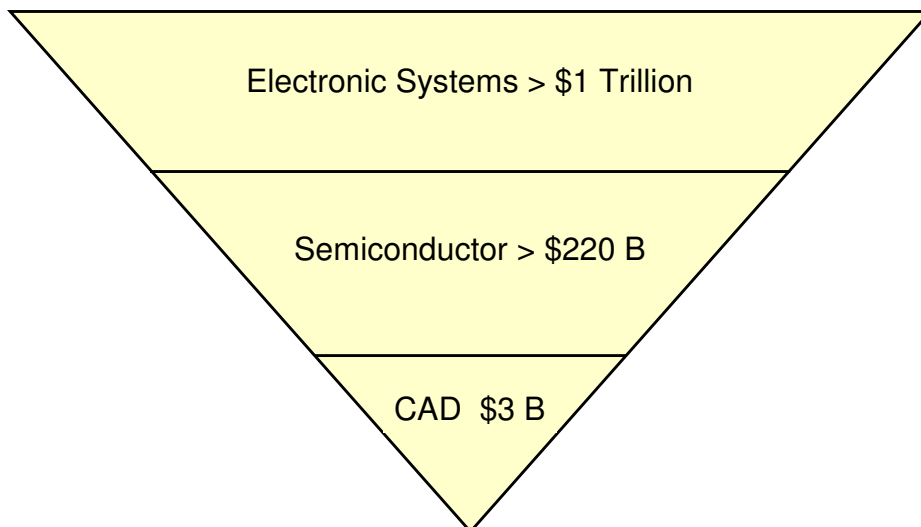
Outline

- Technology trends
- General Design flow

Outline

- **Technology trends** ←
- General Design flow

The Inverted Pyramid



IC Products

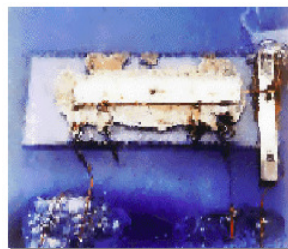
- Processors
 - CPU, DSP, Controllers
- Memory chips
 - RAM, ROM, EEPROM
- Analog
 - Mobile communication, audio/video processing
- Programmable
 - PLA, FPGA
- Embedded systems
 - Used in cars, factories
 - Network cards
- System-on-chip (SoC)



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Integrated Circuit Revolution

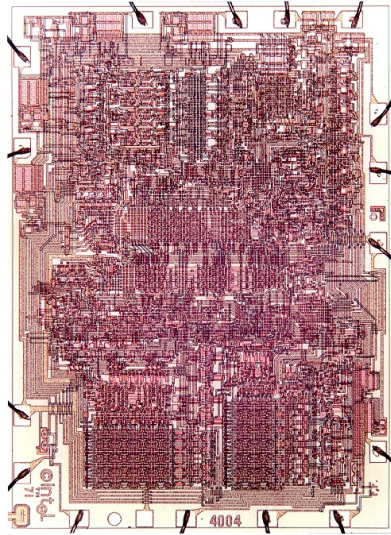


1958: First integrated circuit (germanium)
Built by Jack Kilby at Texas Instruments:
Contained *five* components: transistors, resistors,
and capacitors

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Integrated Circuit Revolution

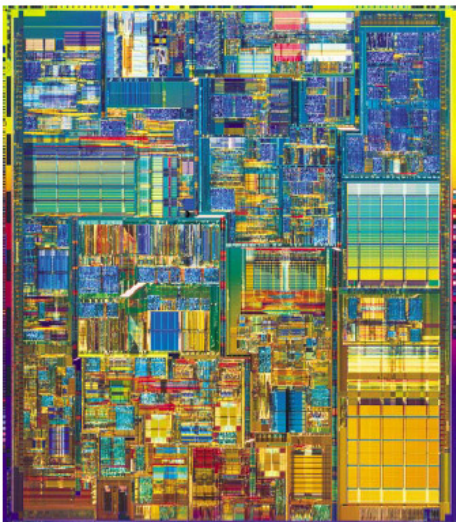


1972: Intel 4004 Microprocessor
Clock speed: 108 KHz
Transistors: 2,300
I/O pins: 16
Technology: 10 μ m

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Integrated Circuit Revolution

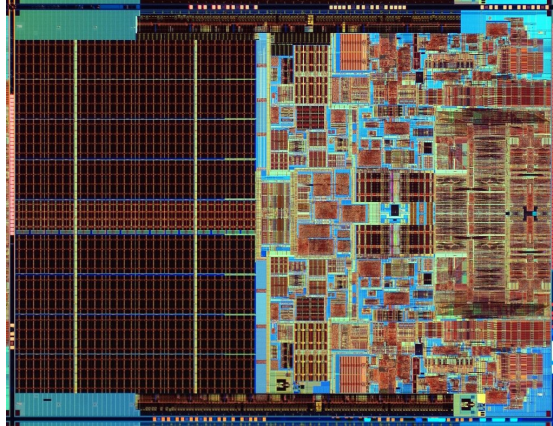


2000: Intel Pentium 4 Processor
Clock speed: 1.5 GHz
Transistors: 42 million
Technology: 0.18 μ m CMOS

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Integrated Circuit Revolution



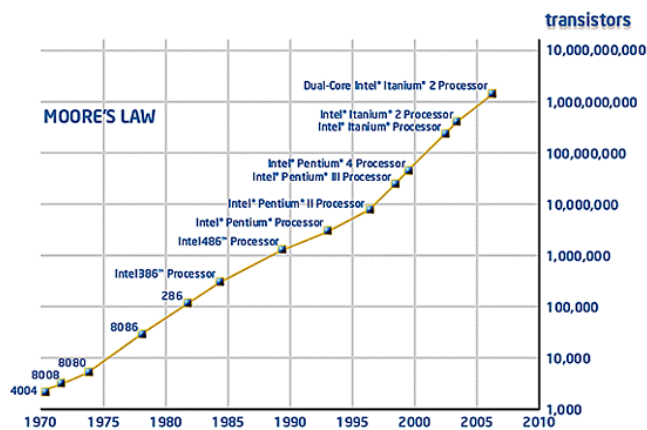
2006: Intel Core 2 Duo
Clock speed: 3.73 GHz
Transistors: 1 billion
Technology: 65nm CMOS

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Moore's Law

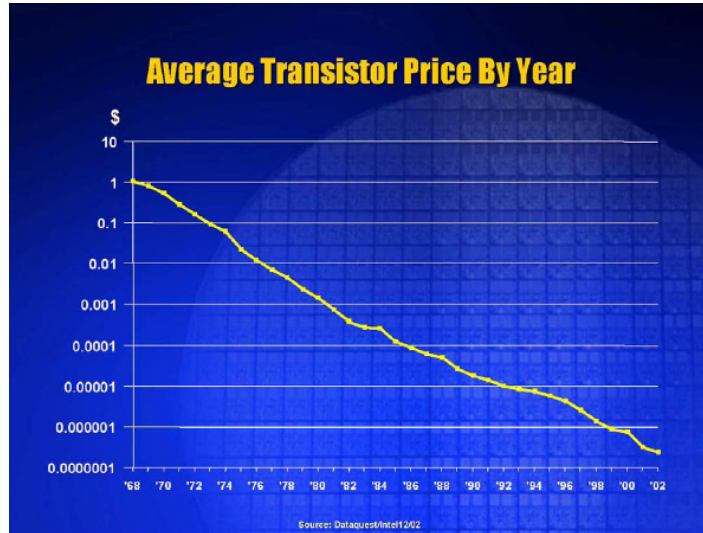
- *Gordon Moore* predicted in 1965 that the number of transistors that can be integrated on a die would **double every 18 months**.



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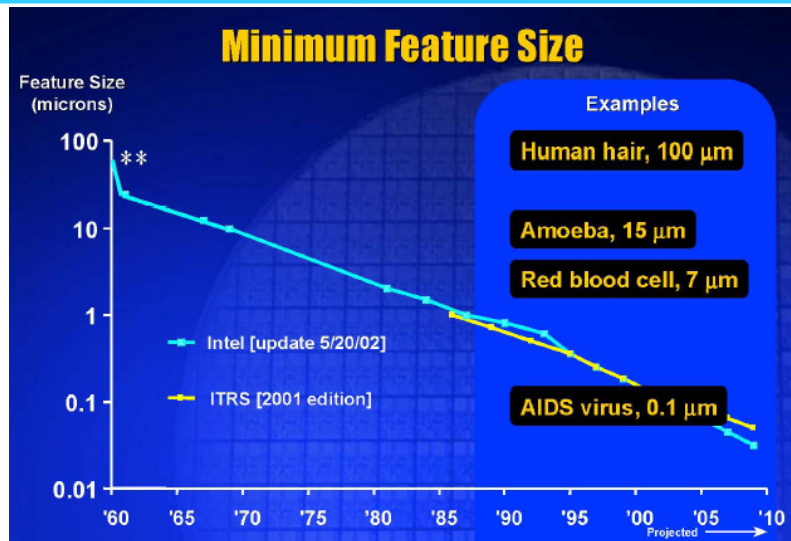
Semiconductor Growth



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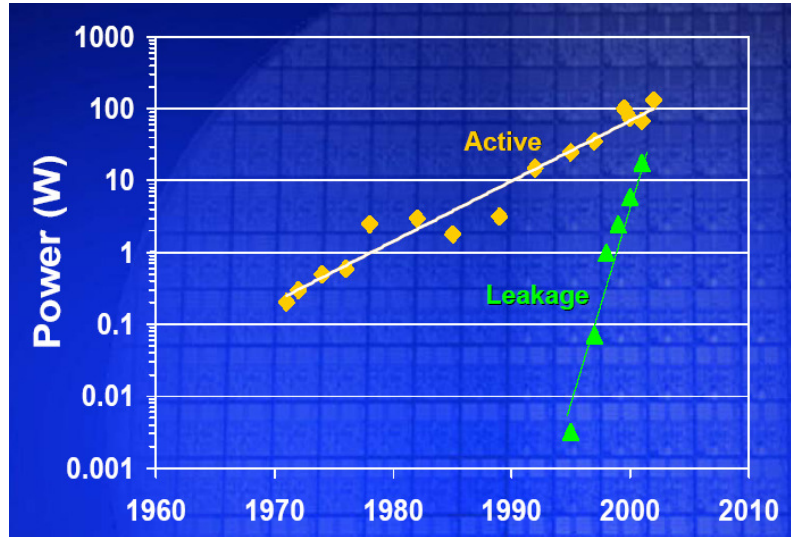
What Makes it Happen



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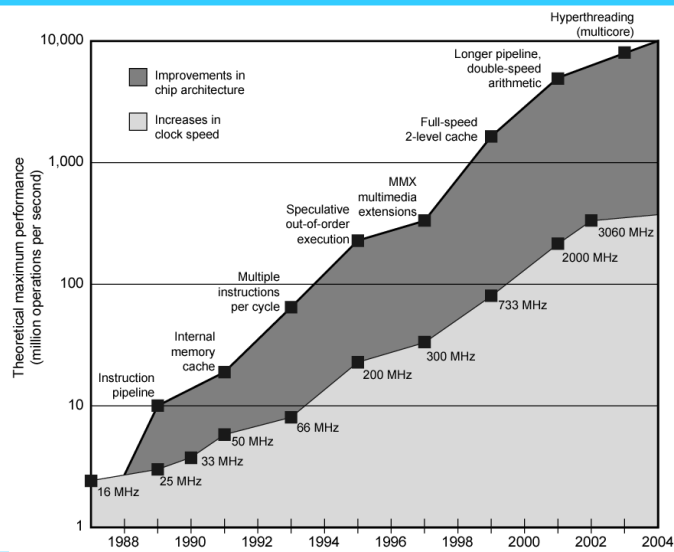
Processor Power (Watts)



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Intel Microprocessor Performance

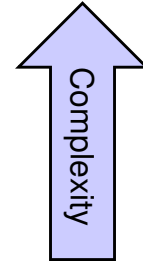


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Increasing Device and Context Complexity

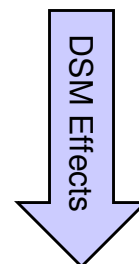
- Exponential increase in device complexity
 - Increasing with Moore's law (or faster)!
- More complex system contexts
 - System contexts in which devices are deployed (e.g. cellular radio) are increasing in complexity
- Require exponential increases in design productivity



We have exponentially more transistors!

Deep Submicron Effects

- Smaller geometries are causing a wide variety of effects that we have largely ignored in the past:
 - Cross-coupled capacitances
 - Signal integrity
 - Resistance
 - Inductance

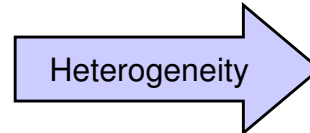


Design of each transistor is getting more difficult!

Heterogeneity on Chip

- Greater diversity of on-chip elements

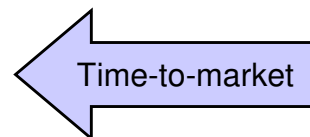
- Processors
- Software
- Memory
- Analog



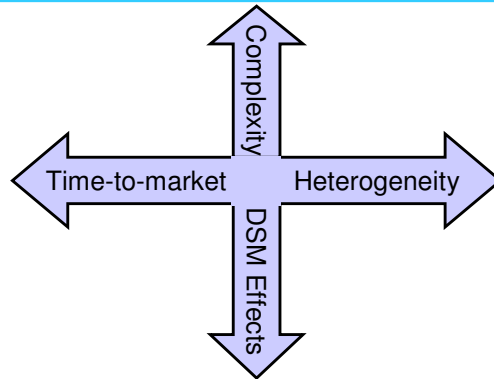
More transistors doing different things!

Stronger Market Pressures

- Decreasing design window
- Less tolerance for design revisions

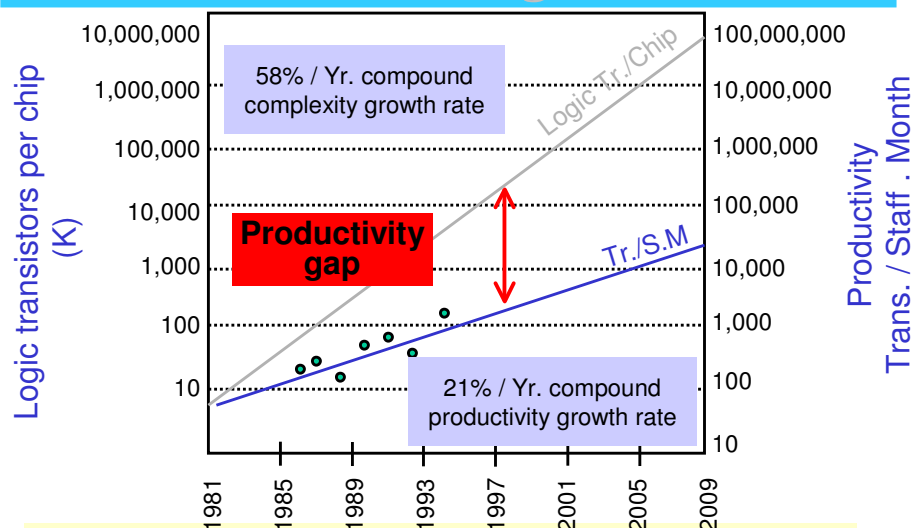


A Quadruple



Exponentially more complex, greater design risk, greater variety, and a smaller design window!

How Are We Doing?



Role of EDA: close the productivity gap

The Evolution of Design Methodology

- We are now entering the era of *block-based design*



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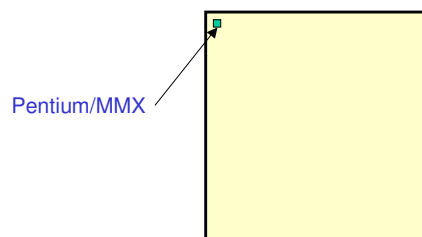
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Trends

- A inexpensive 200mm^2 die has 75M logic transistors, or 375M SRAM transistors
- A 1000mm^2 die would have 400M logic transistors

Core	Trans. Count
486DX4	0.7 million
Pentium/MMX	2.8 million
MPEG-2 encoder	1.5 million
MPEG-2 decoder	0.5 million
8051 microcontroller	0.05 million

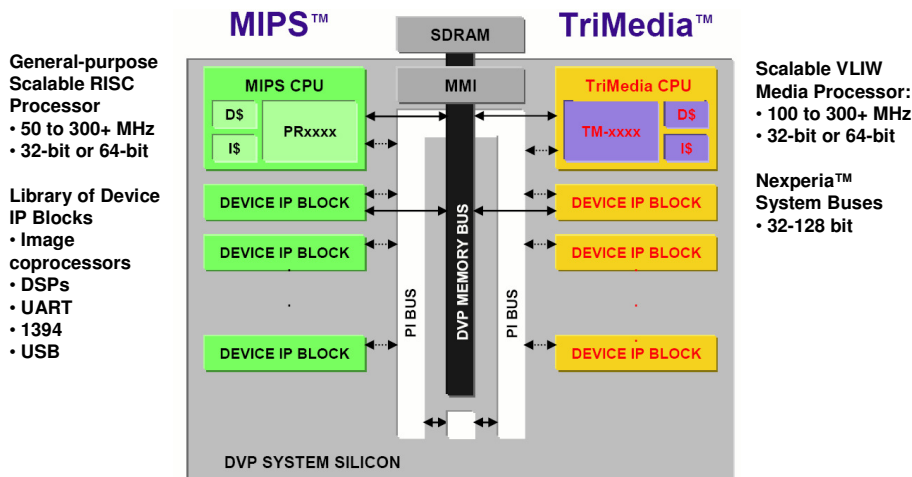
- Up to 7500 8051 microcontrollers on a single chip!
- 150 – 750 cores on a single chip



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The Evolution of SoC Platforms



General-purpose Scalable RISC Processor
 • 50 to 300+ MHz
 • 32-bit or 64-bit

Library of Device IP Blocks
 • Image coprocessors
 • DSPs
 • UART
 • 1394
 • USB

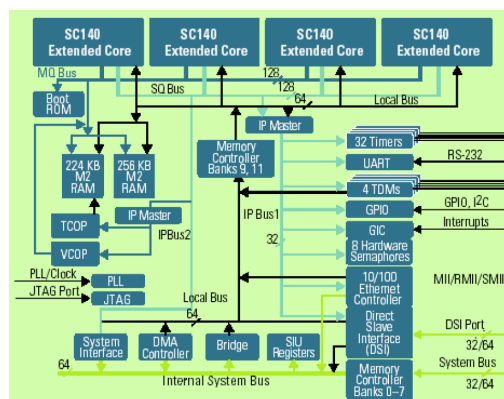
Scalable VLIW Media Processor:
 • 100 to 300+ MHz
 • 32-bit or 64-bit

Nexperia™ System Buses
 • 32-128 bit

2 Cores: Philips' Nexperia PNX8850 SoC platform for High-end digital video (2001)

Running Forward...

- Four 350/400 MHz StarCore SC140 DSP extended cores
- 16 ALUs: 5600/6400 MMACS
- 1436 KB of internal SRAM & multi-level memory hierarchy
- Internal DMA controller supports 16 TDM unidirectional channels,
- Two internal coprocessors (TCOP and VCOP) to provide special-purpose processing capability in parallel with the core processors



6 Cores: Motorola's MSC8126 SoC platform for 3G base stations (late 2003)

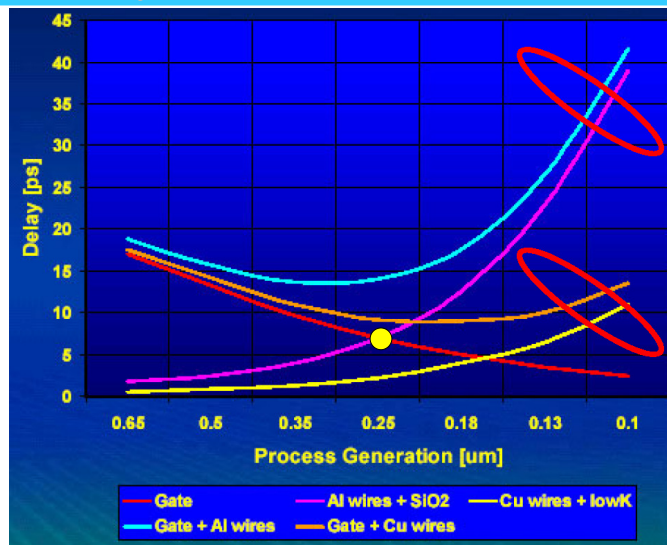
What's Happening in SoCs?

- Technology: no slow-down in sight!
 - Faster and smaller transistors: 90 → 65 → 45 nm
 - ... but slower wires, lower voltage, more noise!
 - ✓ 80% or more of the delay of critical paths will be due to interconnects
- Design complexity: from 2 to 10 to 100 cores!
 - Design reuse is essential
 - ...but differentiation/innovation is key for winning on the market!
- Performance and power: GOPS for MWs!
 - Performance requirements keep going up
 - ...but power budgets don't!

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The Deep Submicron Effects

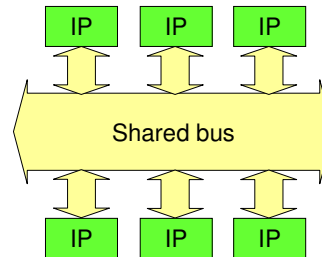


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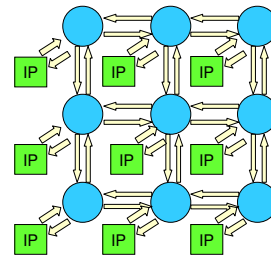
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Communication Architectures

- Shared bus
 - Low area
 - Poor scalability
 - High energy consumption



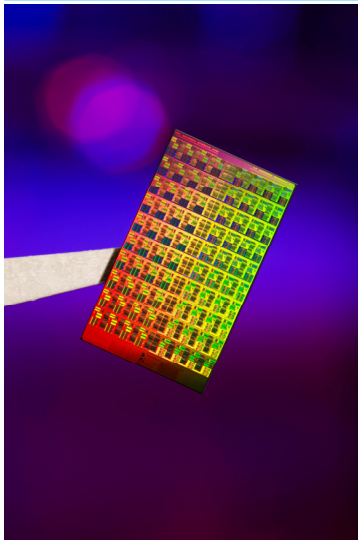
- Network-on-Chip
 - Scalability and modularity
 - Low energy consumption
 - Increase of design complexity



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Intel's Teraflops

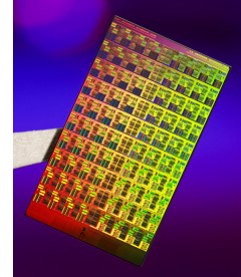


- 100 Million transistors
- 80 cores, 160 FP engines
- Teraflops perf. @ 62 Watts
- On-die mesh network
- Power aware design

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Terascale vs. ASCI RED

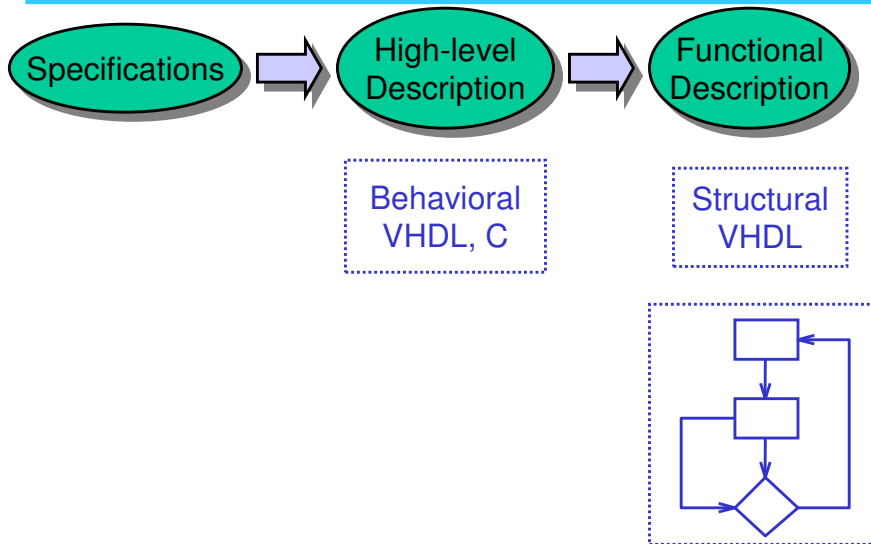


- **ASCI Red** the first computer to reach a Teraflops of processing (1996)
 - 10,000 Pentium @ 200 MHz
 - 500kW of power (+500kW to keep the room cool)
- **Terascale** the first on-chip solution reaching Teraflop of processing (2006)
 - 80 core chip (VLIW based)
 - 3.16-5.7 GHz
 - 62W-256W

Outline

- Technology trends
- **General Design flow** ←

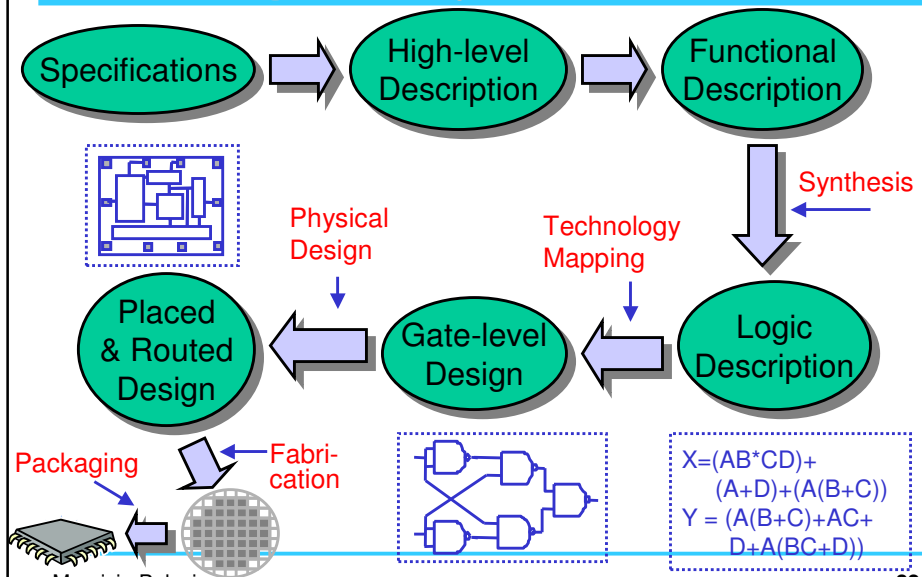
IC Design Steps



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IC Design Steps

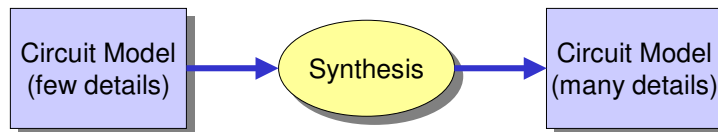


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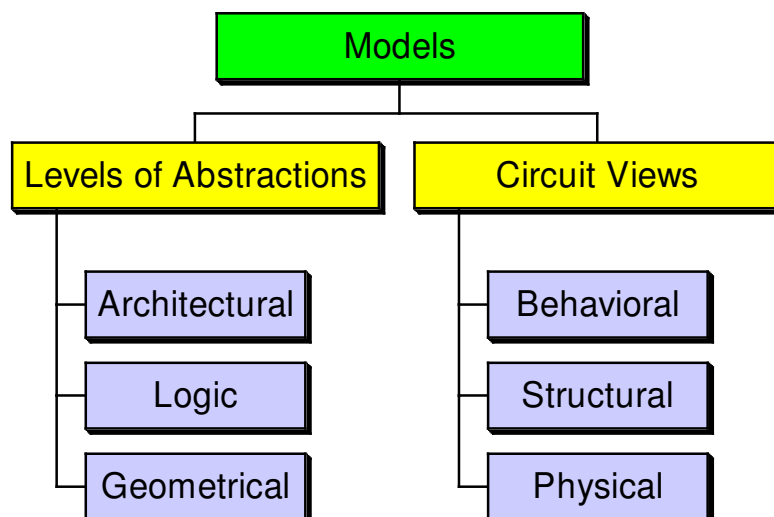
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Circuit Models

- A *model of a circuit* is an *abstraction*
 - A representation that shows relevant features without associated details



Model Classification



Levels of Abstraction

■ Architectural

→ A circuit performs a set of operation, such as *data computation* or *transfer*

✓ HDL models, Flow diagrams, ...

■ Logic

→ A circuit evaluate a set of *logic functions*

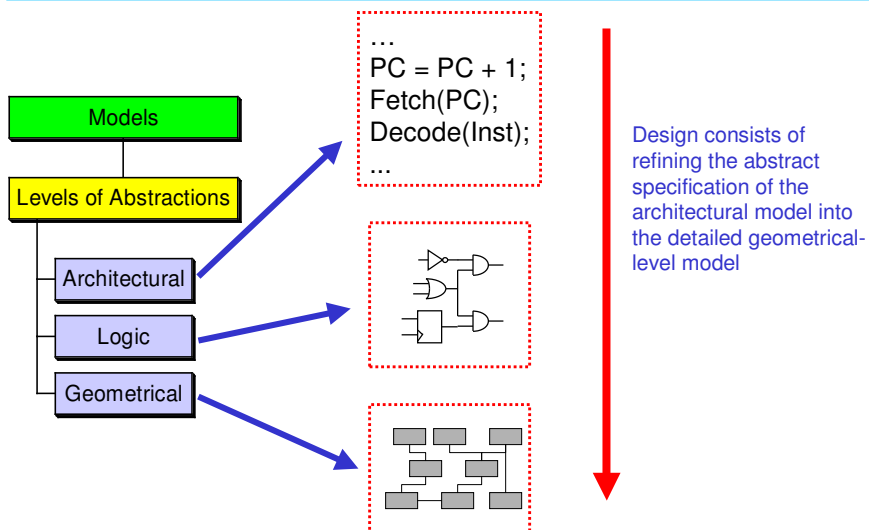
✓ FSMs, Schematics, ...

■ Geometrical

→ A circuit is a set of *geometrical entities*

✓ Floor plans, layouts, ...

Levels of Abstraction



Views of a Model

■ Behavioral

→ Describe the function of a circuit *regardless* of its implementation

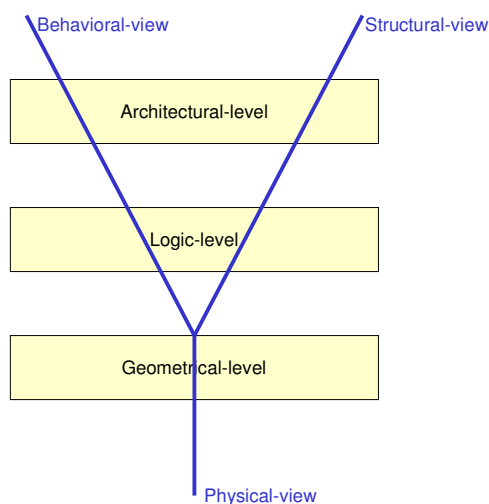
■ Structural

→ Describe a model as an *interconnection* of components

■ Physical

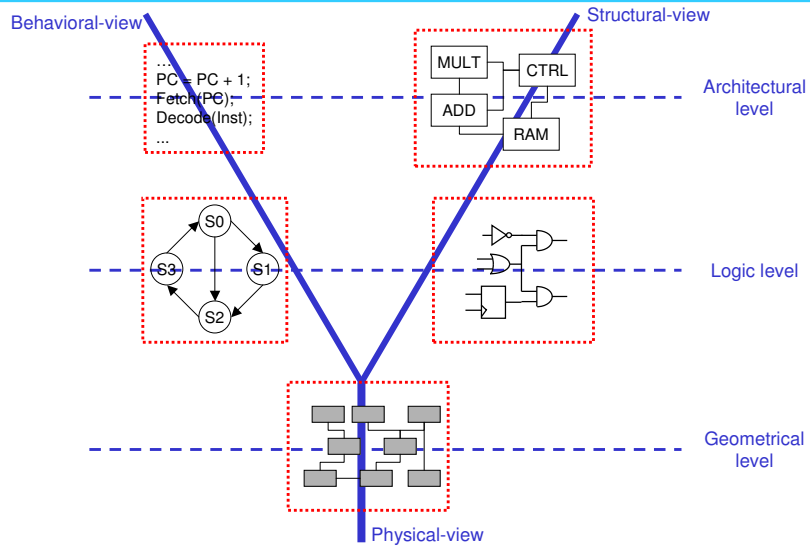
→ Relate to the *physical object* (e.g., transistors) of a design

The Y-chart



Gajski and Kuhn's Y-chart
(Silicon Compilers, Addison-Wesley, 1987)

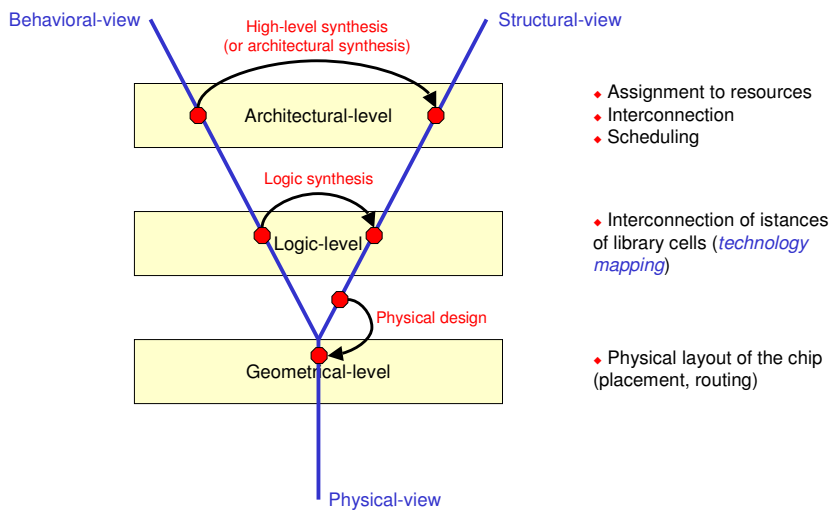
The Y-chart



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Synthesis

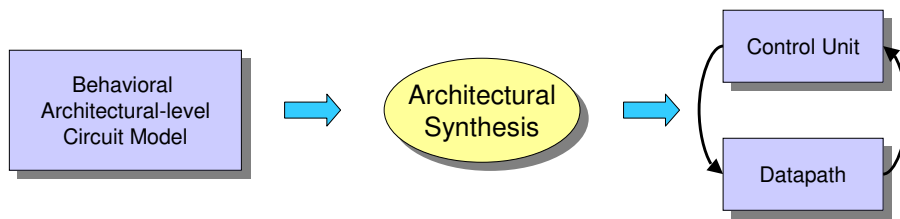


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Architectural Synthesis

- *Identify the resources* that can implement the operations
- *Scheduling* the execution time of the operation
- *Binding* them to the resources



Architectural Synthesis (Example)

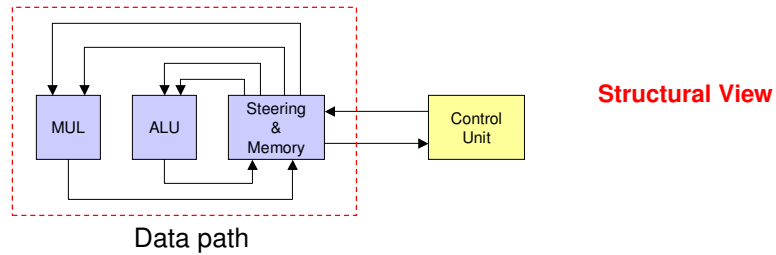
- Solve numerically (by means of the *forward Euler method*) the differential equation $y'+3xy'+3y=0$ in the interval $[0,a]$ with step-size dx and initial values $x(0)=x; y(0)=y; y'(0)=u$.

```
diffeq {
  read (x, y, u, dx, a);
  repeat {
    x1 = x + dx;
    u1 = u - (3*x*u*dx) - (3*y*dx);
    y1 = y + u*dx;
    c = x1 < a;
    x = x1; u = u1; y = y1;
  }
  until (c);
  write (y);
}
```

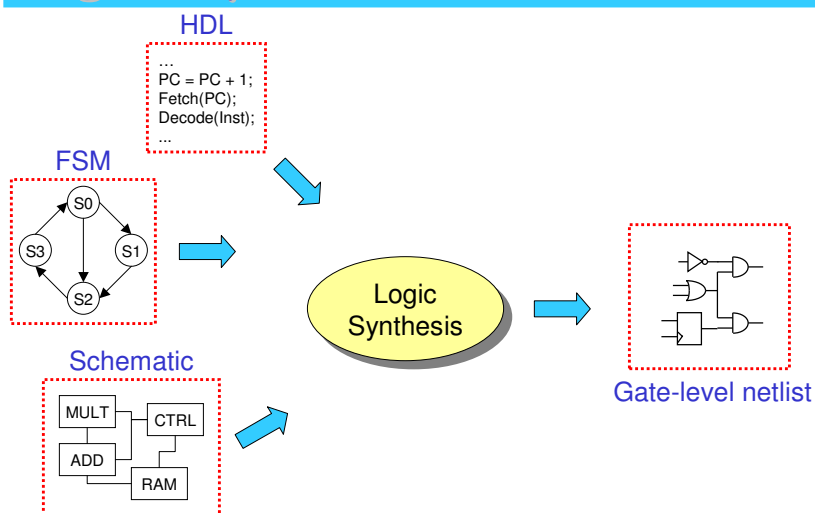
Behavioral View

Architectural Synthesis (Example)

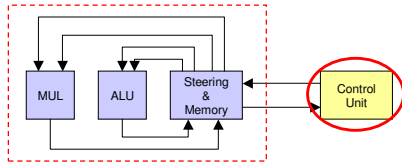
- Let us assume that the data path of the circuit contains two resources:
 - 1 multiplier
 - 1 ALU (add, sub, comparison)



Logic Synthesis



Logic Synthesis (Example)

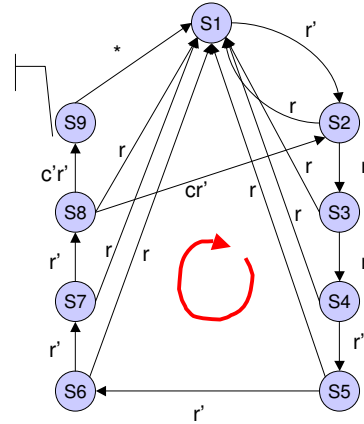


```

diffeq {
  read (x, y, u, dx, a);
  repeat {
    x1 = x + dx;
    u1 = u - (3*x*u*dx) - (3*y*dx);
    y1 = y + u*dx;
    c = x1 < a;
    x = x1; u = u1; y = y1;
  }
  until (c);
  write (y);
}
    
```

Writing the data

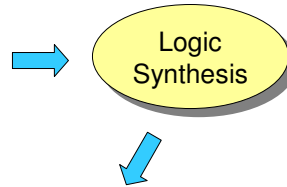
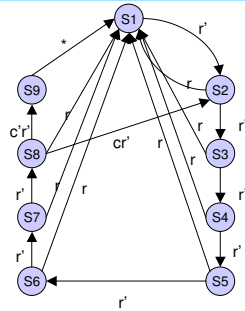
Reset state
(reading the data)



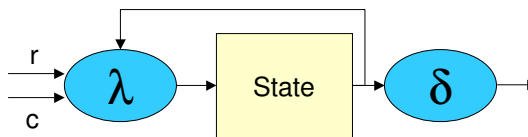
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Logic Synthesis (Example)



From steering
& memory module



To steering
& memory module

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Optimization

Quality measures

→ Performance

- ✓ Combinational logic circuits
 - Propagation delay through the critical path [sec]
- ✓ Synchronous sequential circuits
 - Cycle time [sec]
 - Latency [clock cycles]
 - Execution time = Latency * Cycle time
 - Throughput (for pipeline organization)

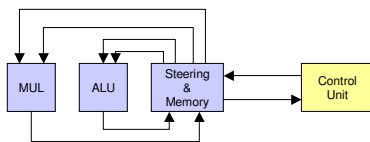
→ Area

- ✓ Logic gates, registers, wiring

→ Power

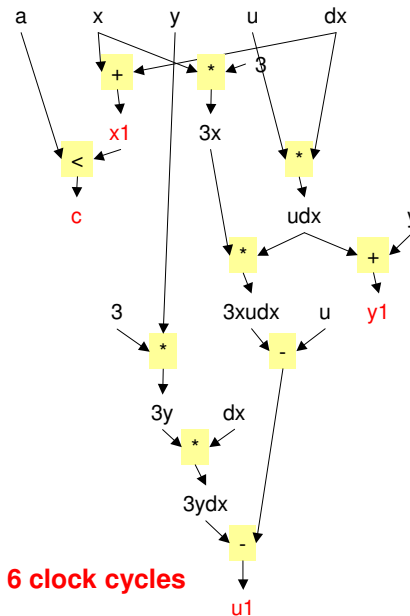
- ✓ Energy
 - Battery life, system weight, ...
- ✓ Power
 - Packaging, reliability, cost, ...

Optimization

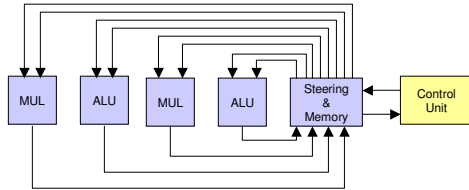


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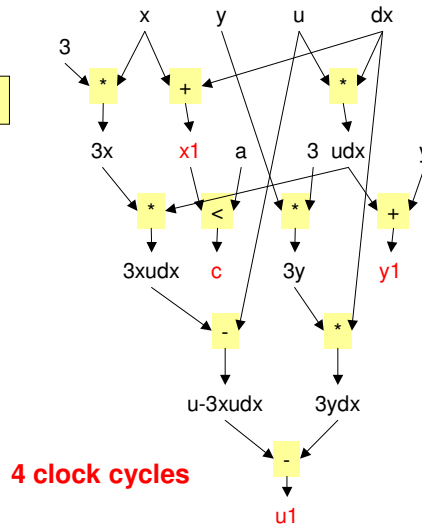


Optimization



```

diffeq {
  read (x, y, u, dx, a);
  repeat {
    x1 = x + dx;
    u1 = u - (3*x*u*dx) - (3*y*dx);
    y1 = y + u*dx;
    c = x1 < a;
    x = x1; u = u1; y = y1;
  }
  until (c);
  write (y);
}
    
```



Design Space

- Parameters
 - # of ALU (max 2), # of Multiplier (max 2)
- Design space
 - System A = 1 alu, 1 multiplier
 - System B = 1 alu, 2 multiplier
 - System C = 2 alu, 1 multiplier
 - System D = 2 alu, 2 multiplier
- Let us assume
 - Multiplier = 5 units of area
 - ALU = 1 unit of area
 - Control Unit + Steering logic = 1 unit of area

