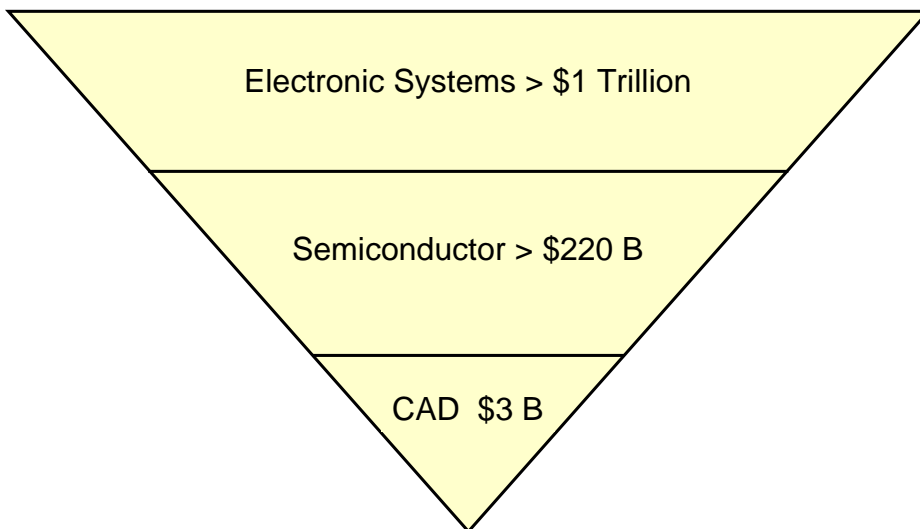

VLSI Design Automation

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The Inverted Pyramid



IC Products

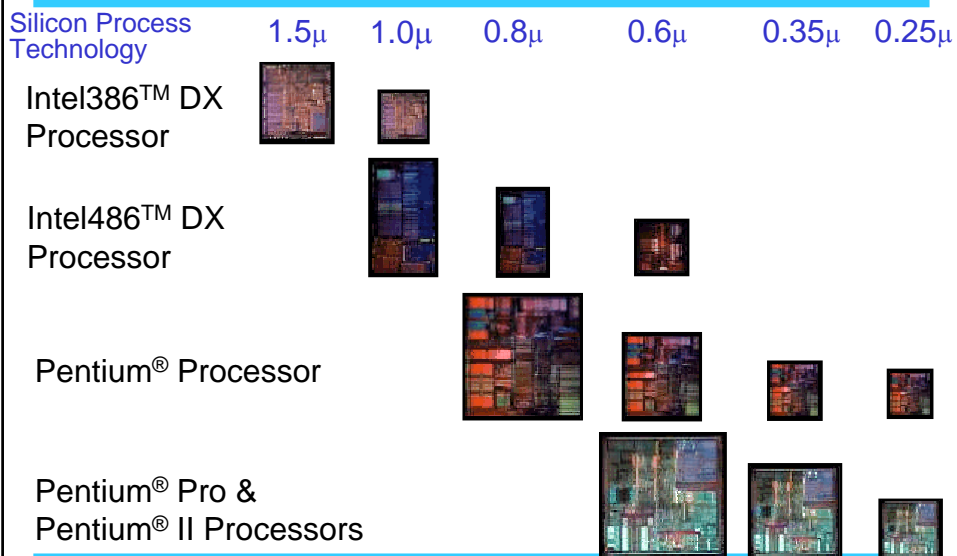
- Processors
 - CPU, DSP, Controllers
- Memory chips
 - RAM, ROM, EEPROM
- Analog
 - Mobile communication, audio/video processing
- Programmable
 - PLA, FPGA
- Embedded systems
 - Used in cars, factories
 - Network cards
- System-on-chip (SoC)



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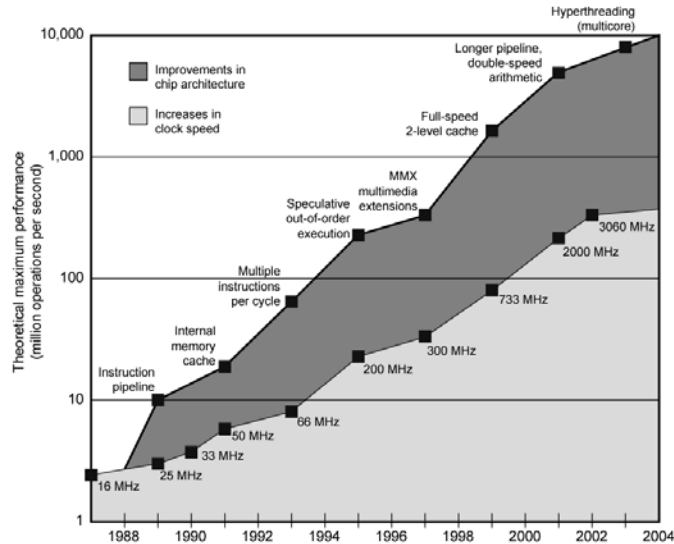
Example: Intel Processor Sizes



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Intel Microprocessor Performance

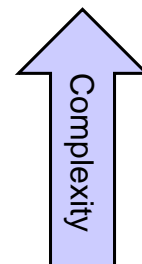


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Increasing Device and Context Complexity

- Exponential increase in device complexity
 - Increasing with Moore's law (or faster)!
- More complex system contexts
 - System contexts in which devices are deployed (e.g. cellular radio) are increasing in complexity
- Require exponential increases in design productivity



We have exponentially more transistors!

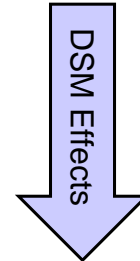
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Deep Submicron Effects

- Smaller geometries are causing a wide variety of effects that we have largely ignored in the past:

- Cross-coupled capacitances
- Signal integrity
- Resistance
- Inductance

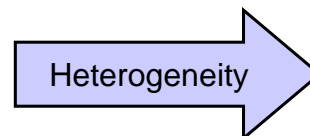


Design of each transistor is getting more difficult!

Heterogeneity on Chip

- Greater diversity of on-chip elements

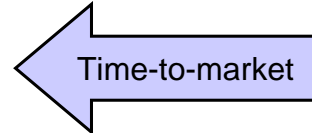
- Processors
- Software
- Memory
- Analog



More transistors doing different things!

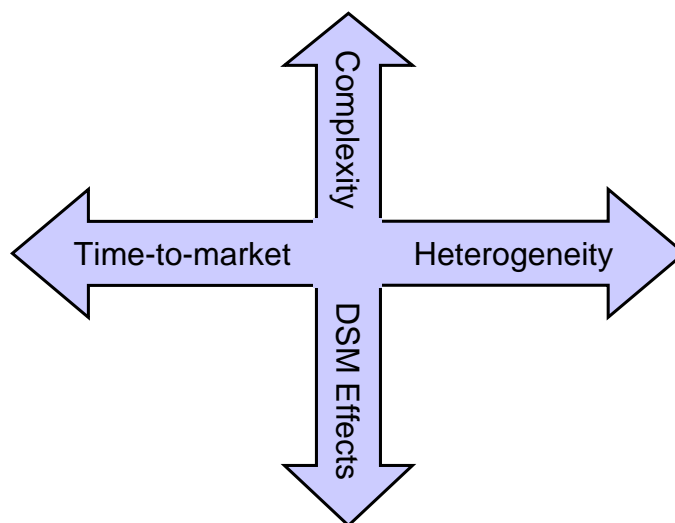
Stronger Market Pressures

- Decreasing design window
- Less tolerance for design revisions

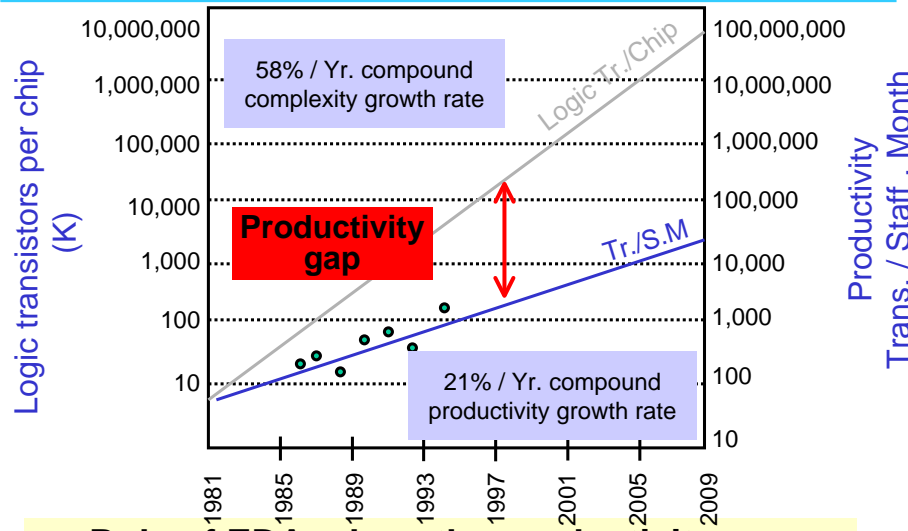


Exponentially more complex, greater design risk, greater variety, and a smaller design window!

A Quadruple



How Are We Doing?



Role of EDA: close the productivity gap

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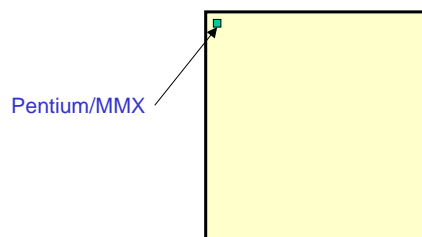
11

Trends

- By 2006, an inexpensive **200mm²** die would have **75M** logic transistors
- A **1000mm²** die would have **400M** logic transistors

Core	Trans. Count
486DX4	0.7 million
Pentium/MMX	2.8 million
MPEG-2 encoder	1.5 million
MPEG-2 decoder	0.5 million
8051 microcontroller	0.05 million

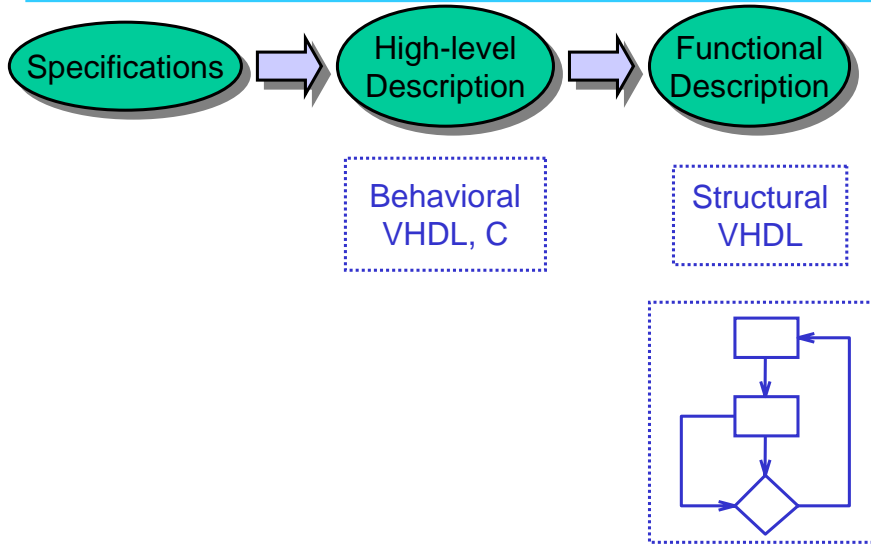
- **Up to 7500** 8051 microcontrollers on a single chip!
- **150 – 750** cores on a single chip



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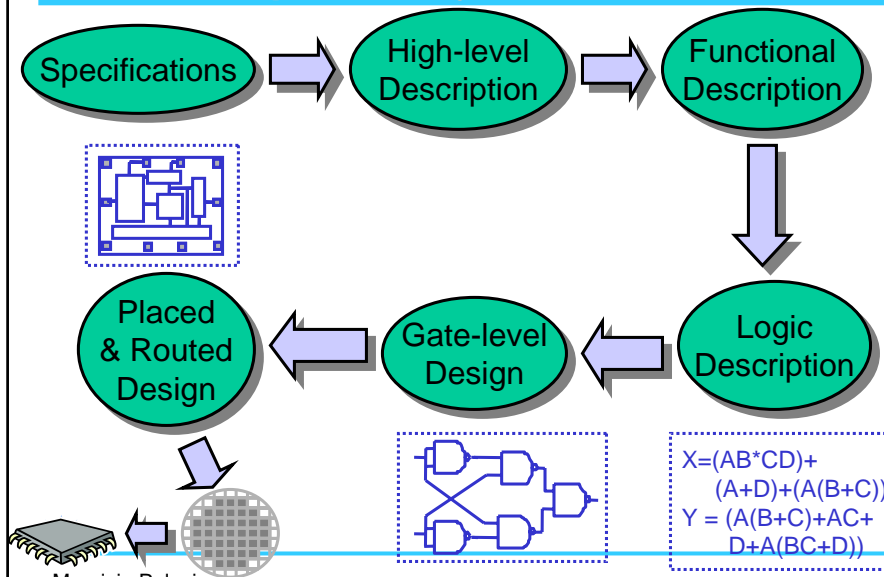
IC Design Steps



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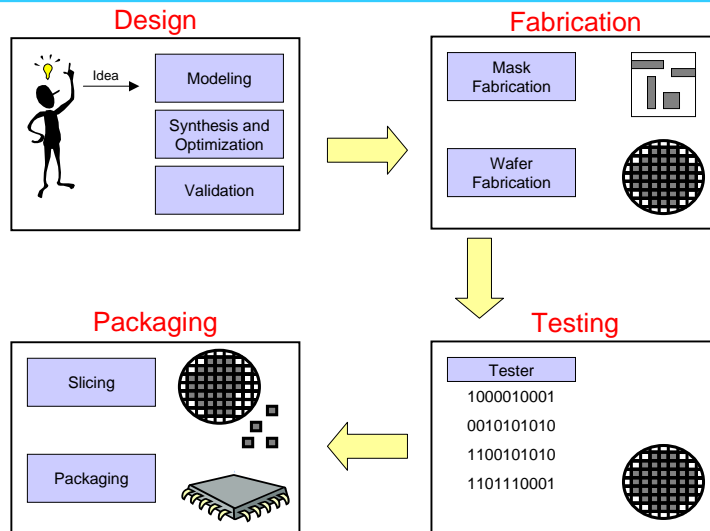
IC Design Steps



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Design of Microelectronic Circuits

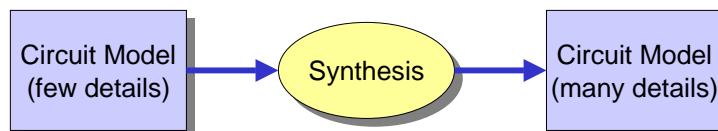


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Circuit Models

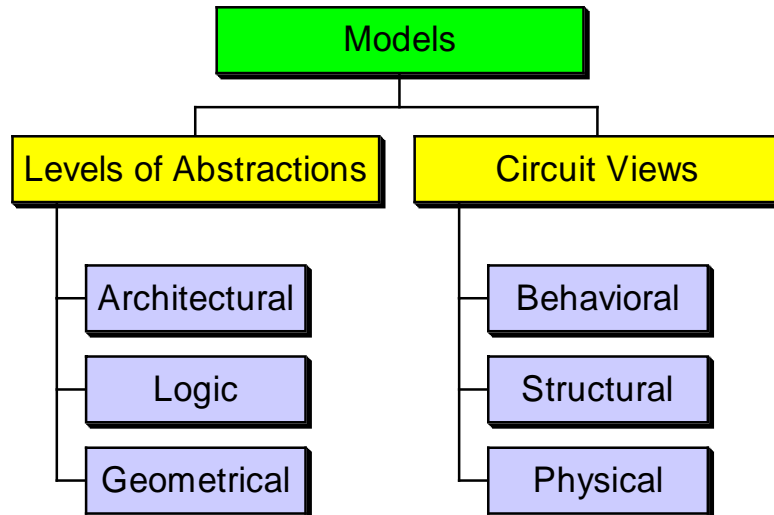
- A *model of a circuit* is an *abstraction*
 - ➔ A representation that shows relevant features without associated details



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Model Classification



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Levels of Abstraction

■ Architectural

→ A circuit performs a set of operation, such as *data computation* or *transfer*

✓ HDL models, Flow diagrams, ...

■ Logic

→ A circuit evaluate a set of *logic functions*

✓ FSMs, Schematics, ...

■ Geometrical

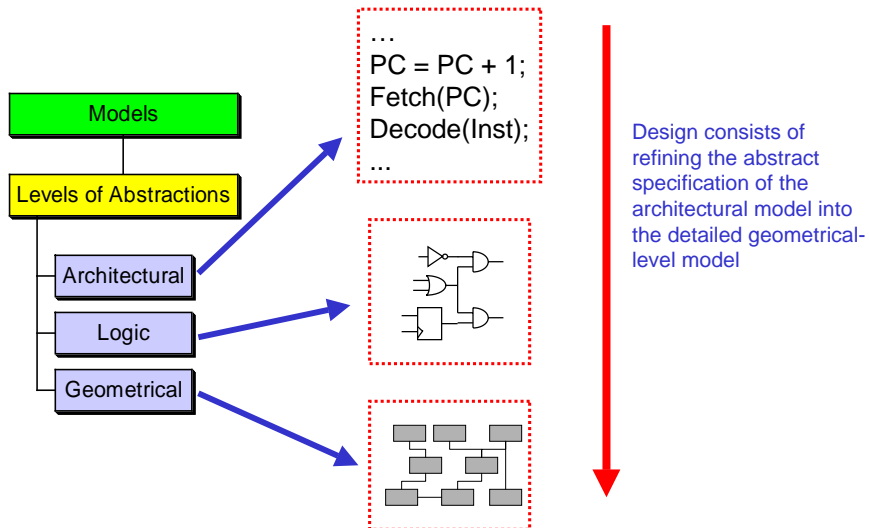
→ A circuit is a set of *geometrical entities*

✓ Floor plans, layouts, ...

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Levels of Abstraction



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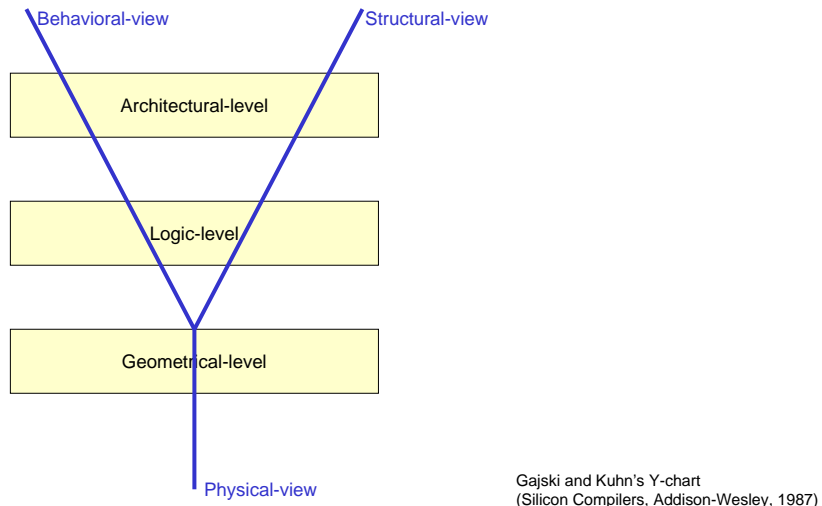
Views of a Model

- Behavioral
 - Describe the function of a circuit *regardless* of its implementation
- Structural
 - Describe a model as an *interconnection* of components
- Physical
 - Relate to the *physical object* (e.g., transistors) of a design

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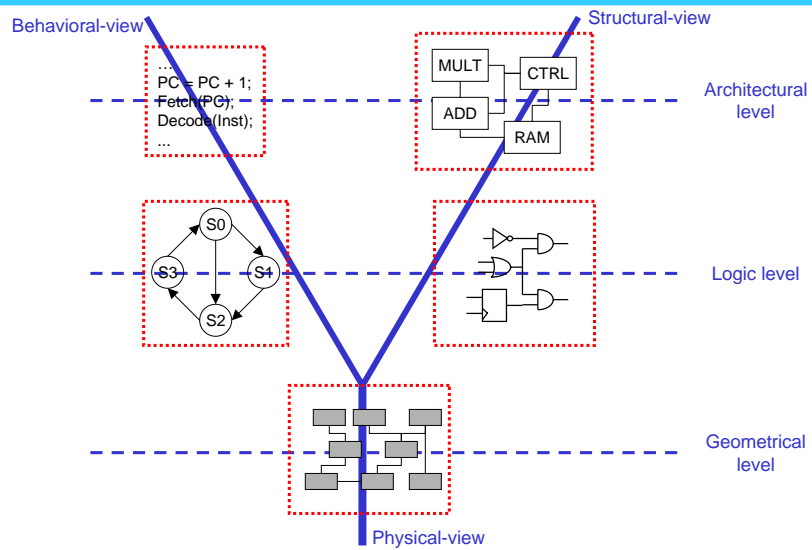
The Y-chart



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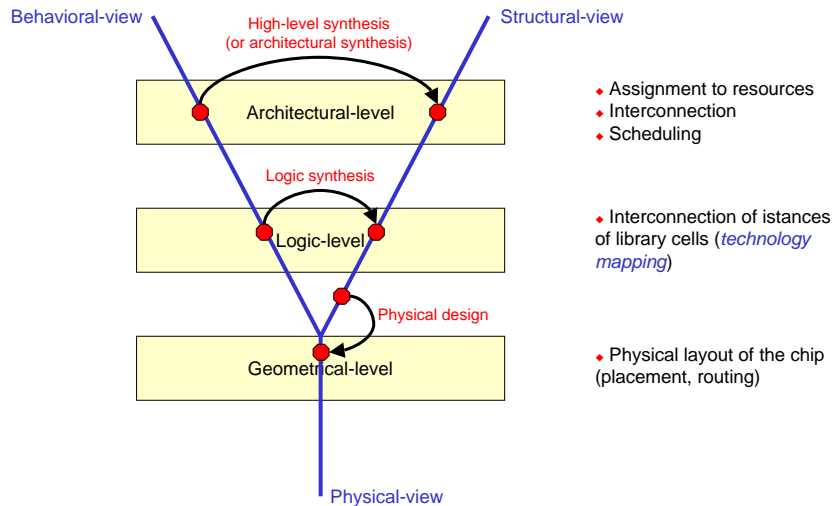
The Y-chart



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Synthesis

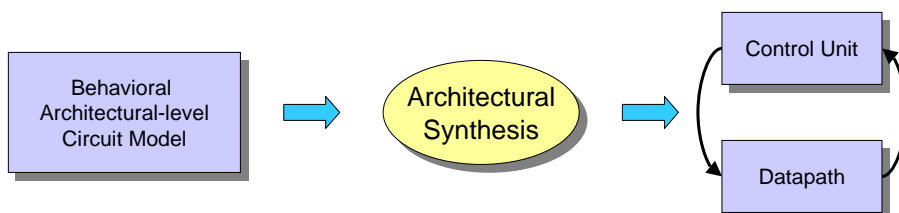


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Architectural Synthesis

- **Identify the resources** that can implement the operations
- **Scheduling** the execution time of the operation
- **Binding** them to the resources



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Architectural Synthesis (Example)

- Solve numerically (by means of the *forward Euler method*) the differential equation $y''+3xy'+3y=0$ in the interval $[0,a]$ with step-size dx and initial values $x(0)=x$, $y(0)=y$, $y'(0)=u$.

```
diffEq {  
  read (x, y, u, dx, a);  
  repeat {  
    x1 = x + dx;  
    u1 = u - (3*x*u*dx) - (3*y*dx);  
    y1 = y + u*dx;  
    c = x1 < a;  
    x = x1; u = u1; y = y1;  
  }  
  until(c);  
  write(y);  
}
```

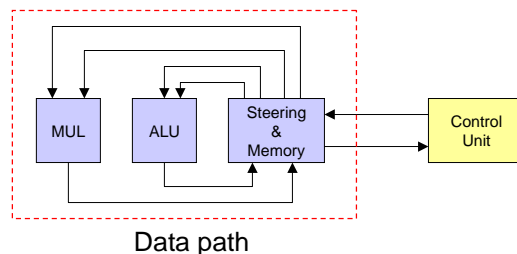
Behavioral View

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Architectural Synthesis (Example)

- Let us assume that the data path of the circuit contains two resources:
 - 1 multiplier
 - 1 ALU (add, sub, comparison)

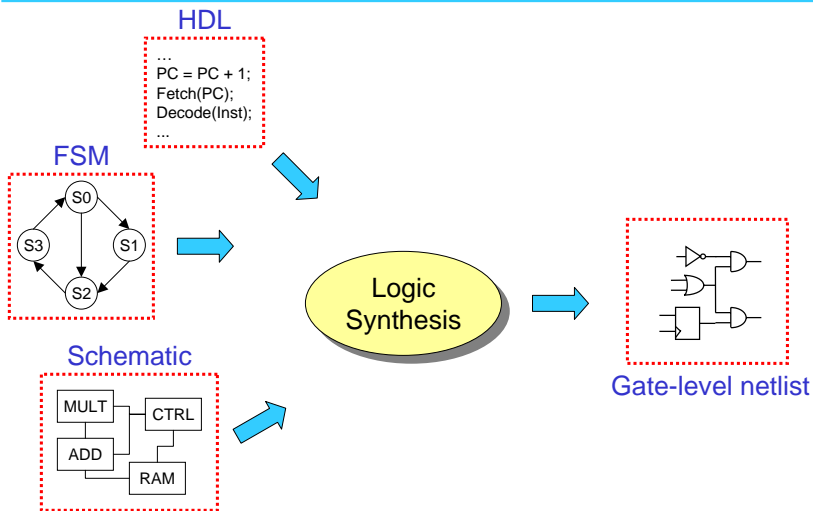


Structural View

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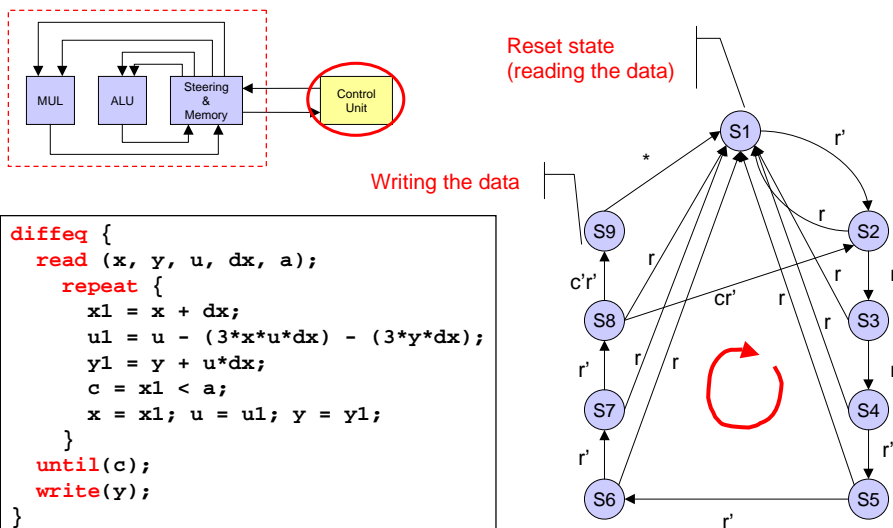
Logic Synthesis



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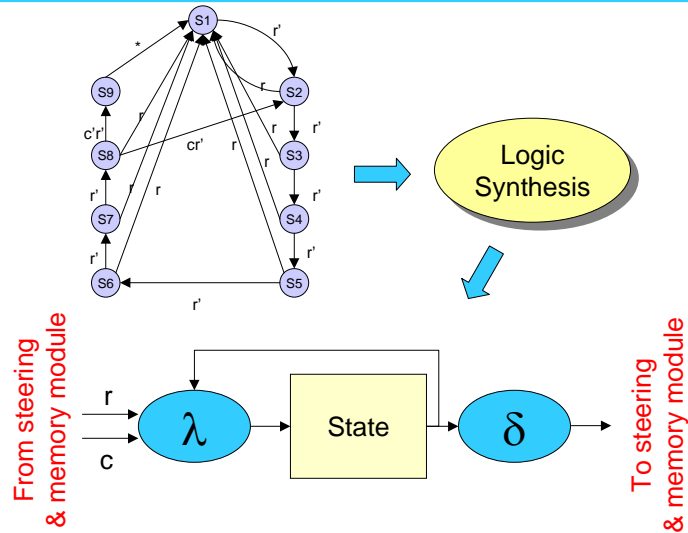
Logic Synthesis (Example)



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Logic Synthesis (Example)



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Optimization

■ Quality measures

→ Performance

- ✓ Combinational logic circuits
 - *Propagation delay* through the critical path [sec]
- ✓ Synchronous sequential circuits
 - *Cycle time* [sec]
 - *Latency* [clock cycles]
 - *Execution time* = Latency * Cycle time
 - *Throughput* (for *pipeline* organization)

→ Area

- ✓ Logic gates, registers, wiring

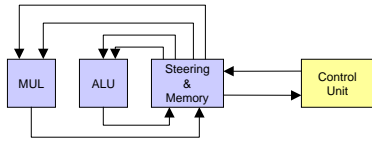
→ Power

- ✓ Energy
 - Battery life, system weight, ...
- ✓ Power
 - Packaging, reliability, cost, ...

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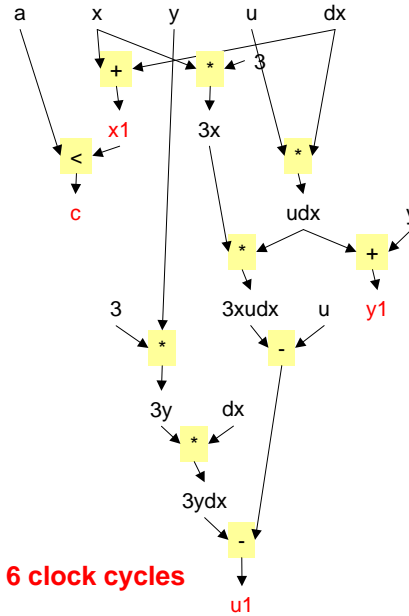
30

Optimization



```

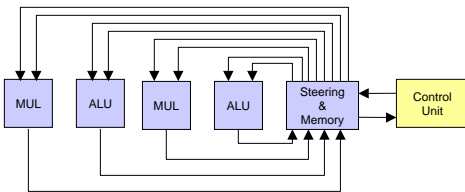
diffeq {
  read (x, y, u, dx, a);
  repeat {
    x1 = x + dx;
    u1 = u - (3*x*u*dx) - (3*y*dx);
    y1 = y + u*dx;
    c = x1 < a;
    x = x1; u = u1; y = y1;
  }
  until(c);
  write(y);
}
    
```



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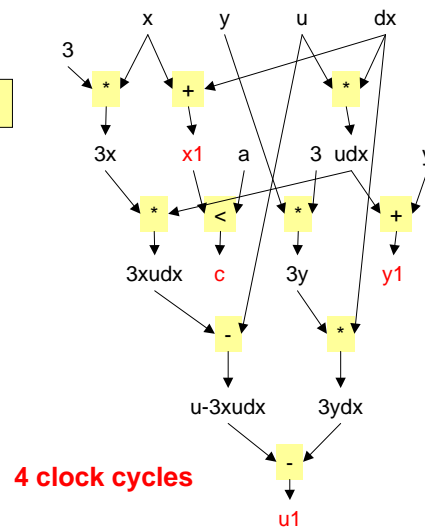
31

Optimization



```

diffeq {
  read (x, y, u, dx, a);
  repeat {
    x1 = x + dx;
    u1 = u - (3*x*u*dx) - (3*y*dx);
    y1 = y + u*dx;
    c = x1 < a;
    x = x1; u = u1; y = y1;
  }
  until(c);
  write(y);
}
    
```

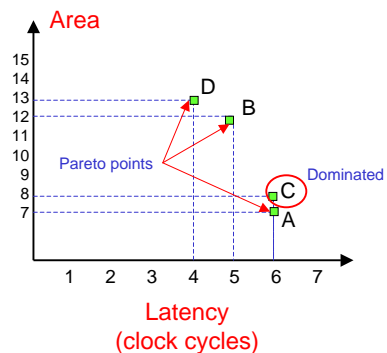


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Design Space

- Parameters
 - # of ALU (max 2), # of Multiplier (max 2)
- Design space
 - System A = 1 alu, 1 multiplier
 - System B = 1 alu, 2 multiplier
 - System C = 2 alu, 1 multiplier
 - System D = 2 alu, 2 multiplier
- Let us assume
 - Multiplier = 5 units of area
 - ALU = 1 unit of area
 - Control Unit + Steering logic = 1 unit of area



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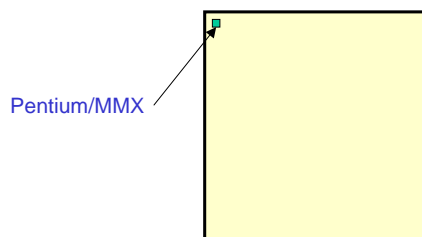
33

Trends

- By 2006, an inexpensive 200mm^2 die would have 75M logic transistors, or 375M SRAM transistors
- A 1000mm^2 die would have 400M logic transistors

Core	Trans. Count
486DX4	0.7 million
Pentium/MMX	2.8 million
MPEG-2 encoder	1.5 million
MPEG-2 decoder	0.5 million
8051 microcontroller	0.05 million

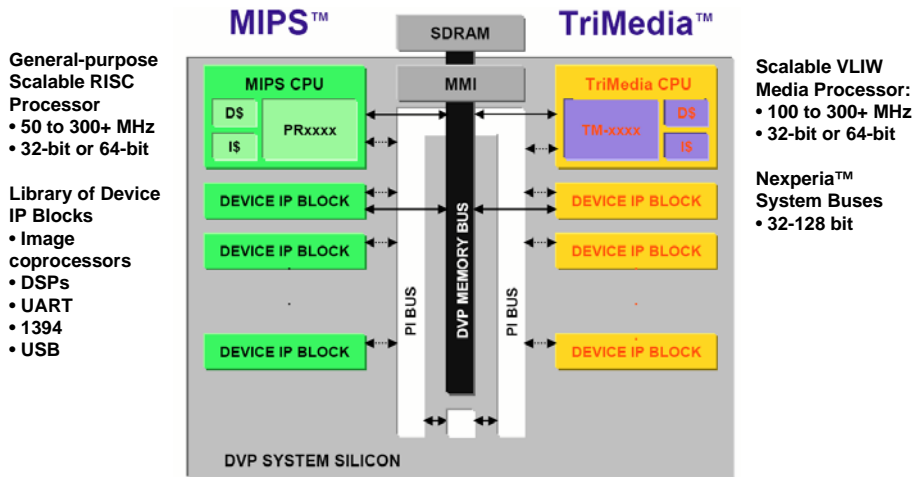
- Up to 7500 8051 microcontrollers on a single chip!
- 150 – 750 cores on a single chip



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The Evolution of SoC Platforms



General-purpose Scalable RISC Processor
 • 50 to 300+ MHz
 • 32-bit or 64-bit

Library of Device IP Blocks
 • Image coprocessors
 • DSPs
 • UART
 • 1394
 • USB

Scalable VLIW Media Processor:
 • 100 to 300+ MHz
 • 32-bit or 64-bit

Nexperia™ System Buses
 • 32-128 bit

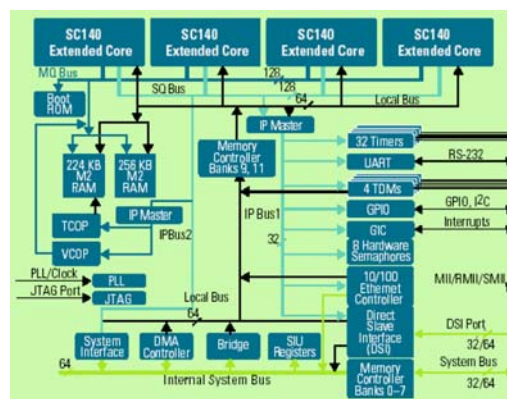
2 Cores: Philips' Nexperia PNX8850 SoC platform for High-end digital video (2001)

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Running Forward...

- Four 350/400 MHz StarCore SC140 DSP extended cores
- 16 ALUs: 5600/6400 MMACS
- 1436 KB of internal SRAM & multi-level memory hierarchy
- Internal DMA controller supports 16 TDM unidirectional channels,
- Two internal coprocessors (TCOP and VCOP) to provide special-purpose processing capability in parallel with the core processors



6 Cores: Motorola's MSC8126 SoC platform for 3G base stations (late 2003)

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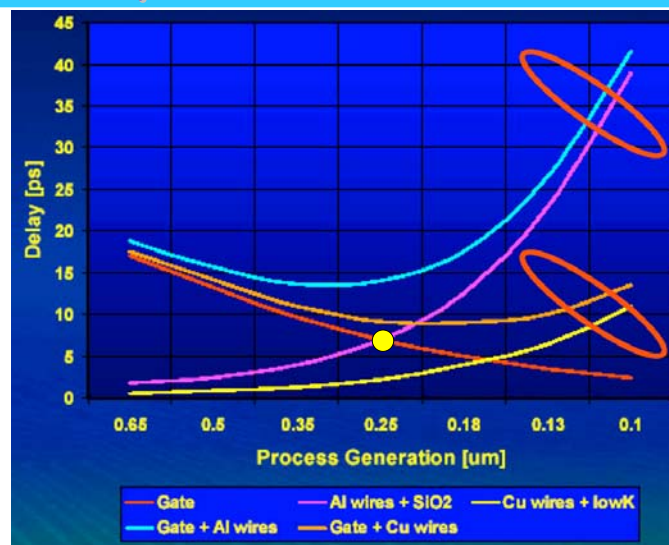
What's Happening in SoCs?

- Technology: no slow-down in sight!
 - Faster and smaller transistors: 90 → 65 → 45 nm
 - ... but slower wires, lower voltage, more noise!
 - ✓ 80% or more of the delay of critical paths will be due to interconnects
- Design complexity: from 2 to 10 to 100 cores!
 - Design reuse is essential
 - ...but differentiation/innovation is key for winning on the market!
- Performance and power: GOPS for MWs!
 - Performance requirements keep going up
 - ...but power budgets don't!

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The Deep Submicron Effects

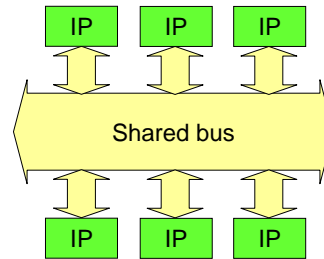


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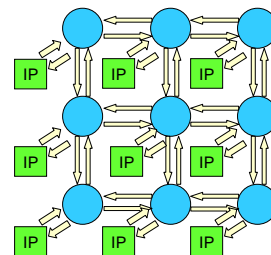
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Communication Architectures

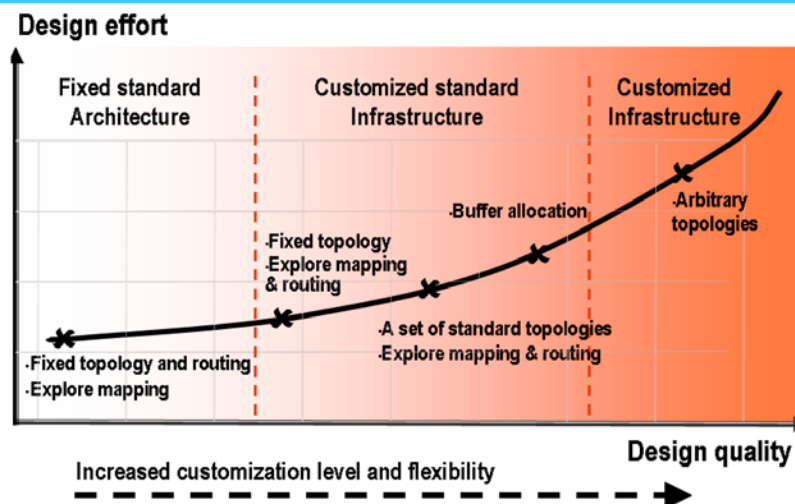
- Shared bus
 - ➔ Low area
 - ➔ Poor scalability
 - ➔ High energy consumption



- Network-on-Chip
 - ➔ Scalability and modularity
 - ➔ Low energy consumption
 - ➔ Increase of design complexity



Design Space Exploration for NoC



Ogras et al., ASAP'05