

---

# VLSI Design Automation

# Outline

---

- Technology trends
- VLSI Design flow (an overview)

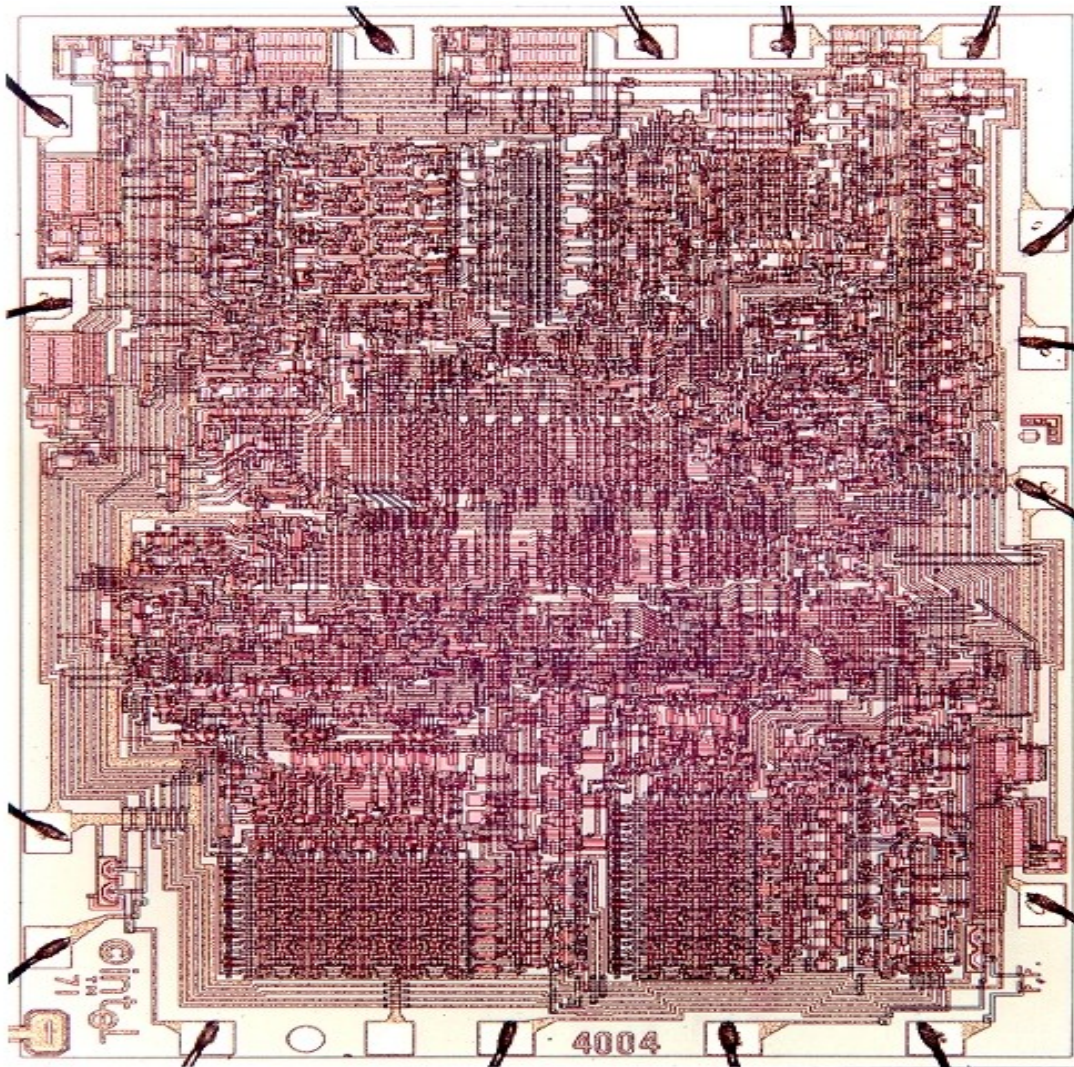
# IC Products

- Processors
  - CPU, DSP, Controllers
- Memory chips
  - RAM, ROM, EEPROM
- Analog
  - Mobile communication, audio/video processing
- Programmable
  - PLA, FPGA
- Embedded systems
  - Used in cars, factories
  - Network cards
- System-on-chip (SoC)



# Integrated Circuit Revolution

---



## 1972: Intel 4004 Microprocessor

Clock speed: 108 KHz

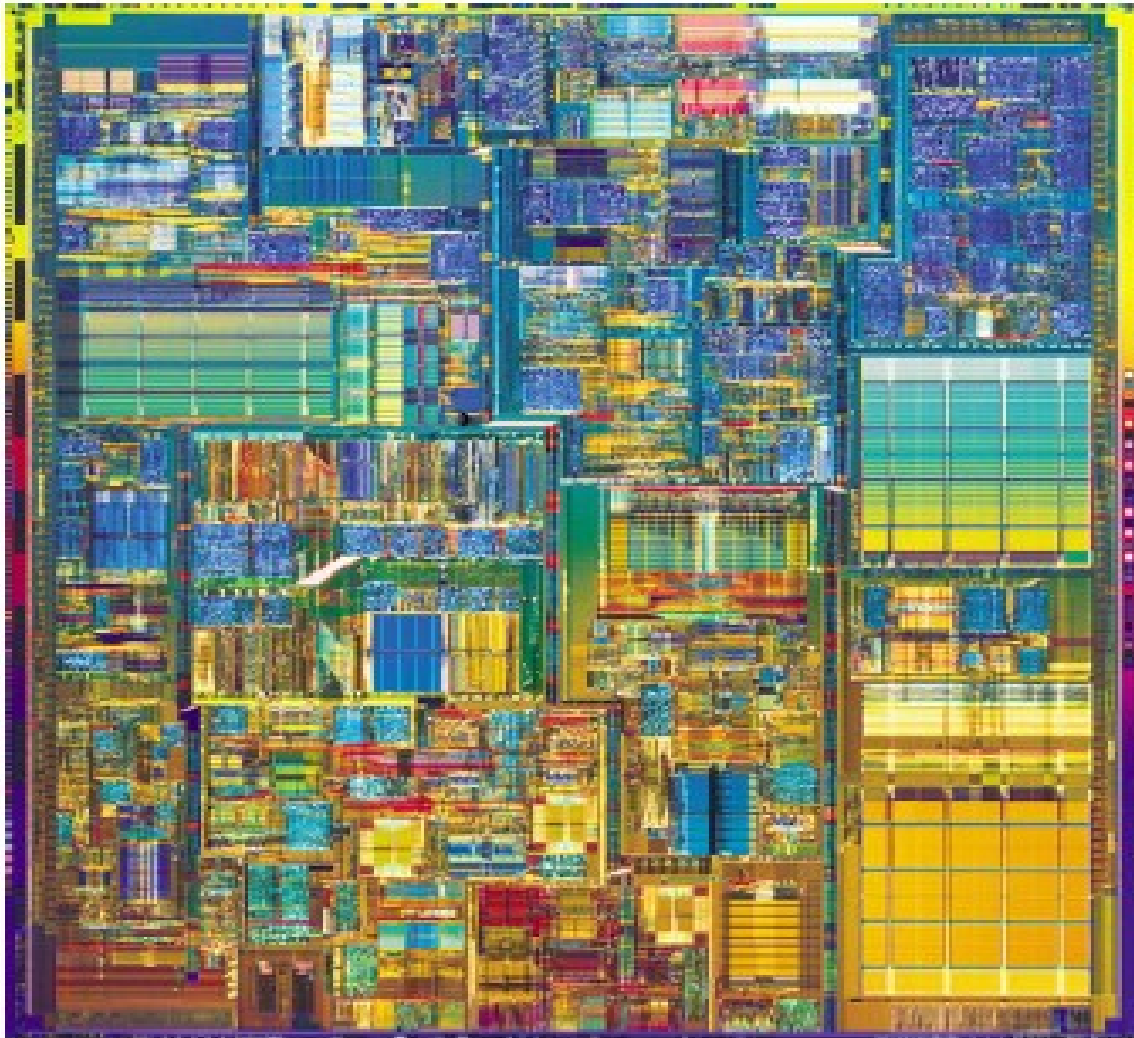
# Transistors: 2,300

# I/O pins: 16

Technology: 10 $\mu$ m

# Integrated Circuit Revolution

---



**2000: Intel Pentium 4 Processor**

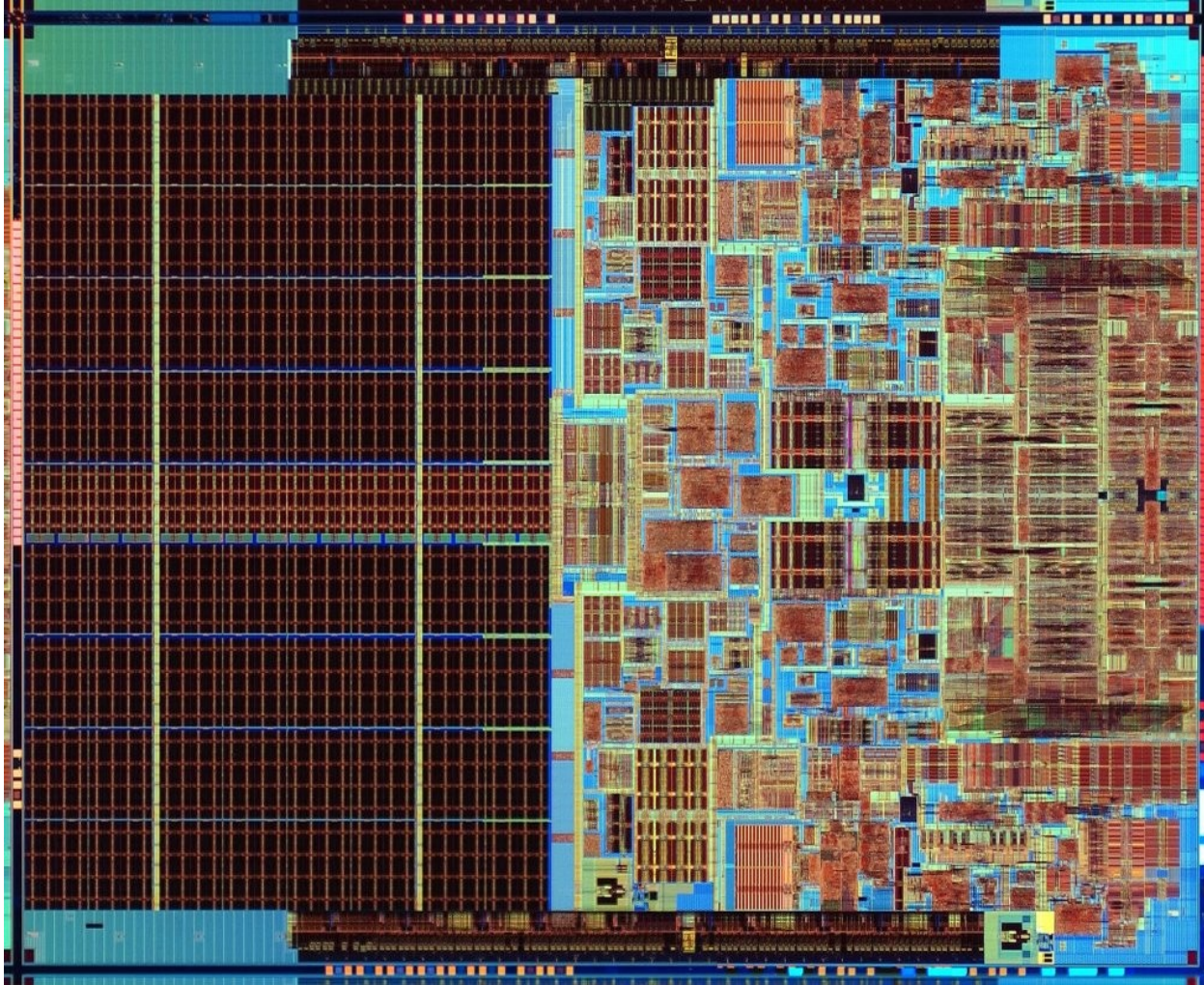
Clock speed: 1.5 GHz

# Transistors: 42 million

Technology: 0.18 $\mu$ m CMOS

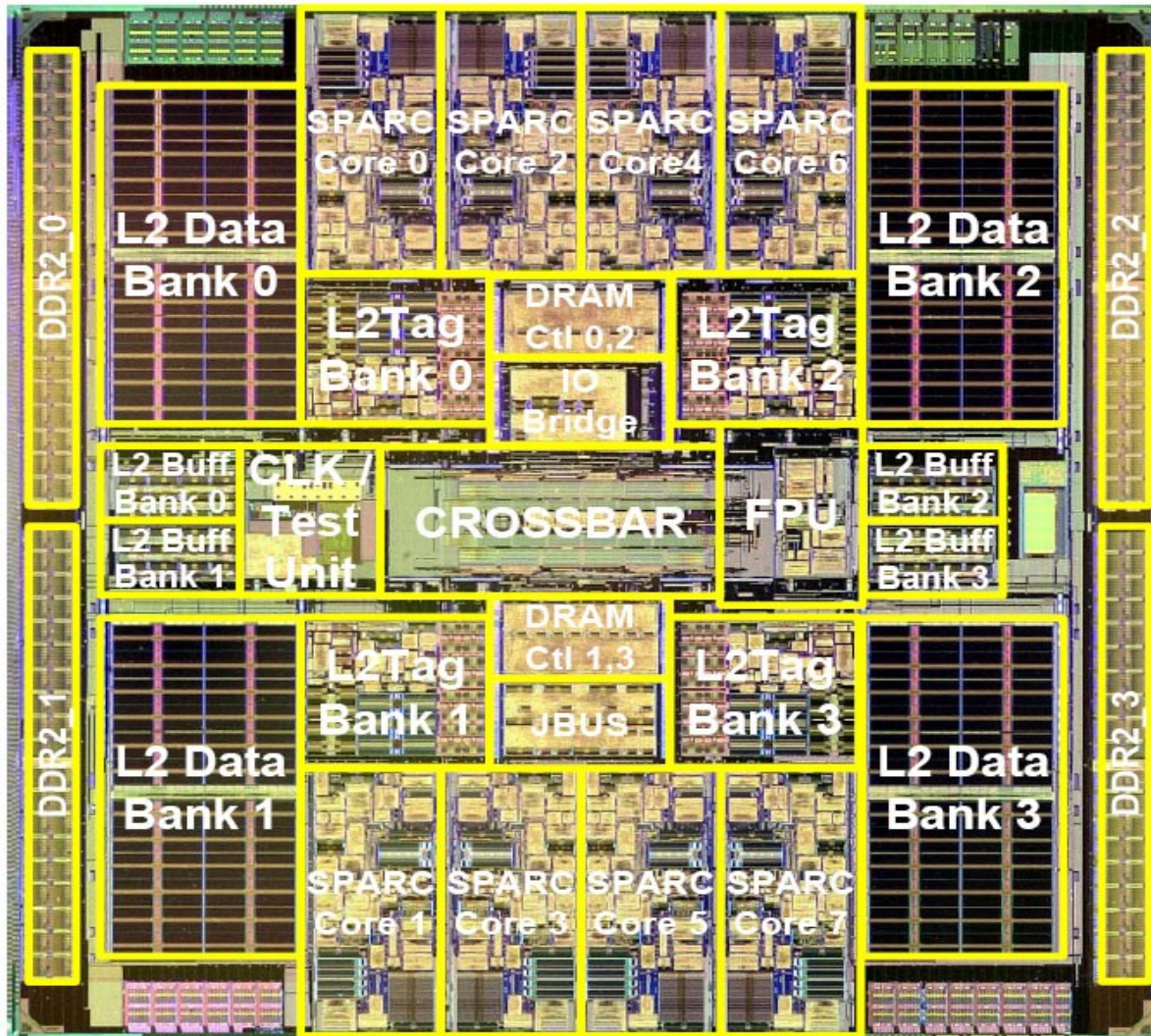
# Integrated Circuit Revolution

---



**2006: Intel Core 2 Duo**  
Clock speed: 3.73 GHz  
# Transistors: 1 billion  
Technology: 65nm CMOS

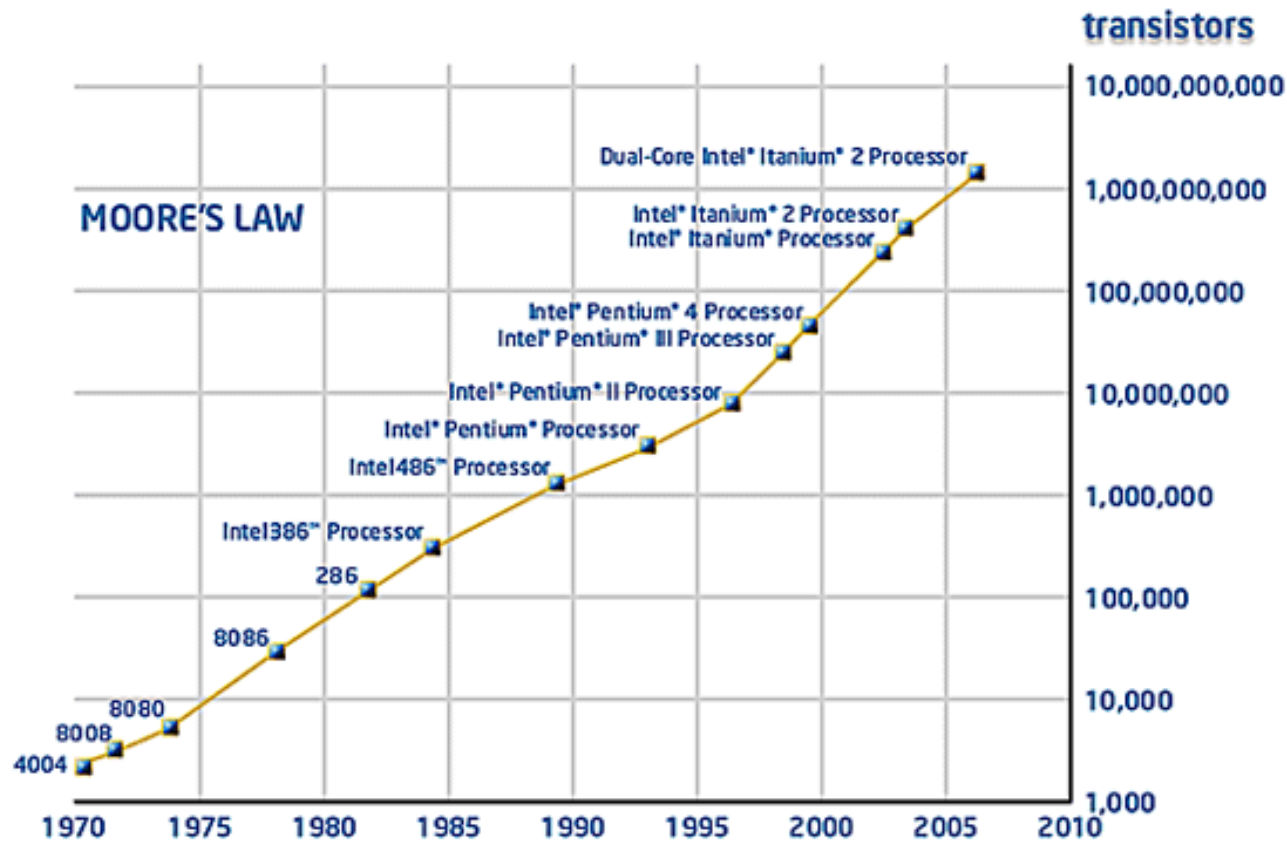
# Integrated Circuit Revolution



**2005: Sun UltraSparc T1**  
8 cores, 4 threads per core  
Clock speed: 1.2 GHz  
# Transistors: 300 million  
Technology: 90nm CMOS

# Moore's Law

- *Gordon Moore* predicted in 1965 that the number of transistors that can be integrated on a die would **double every 18 months**.

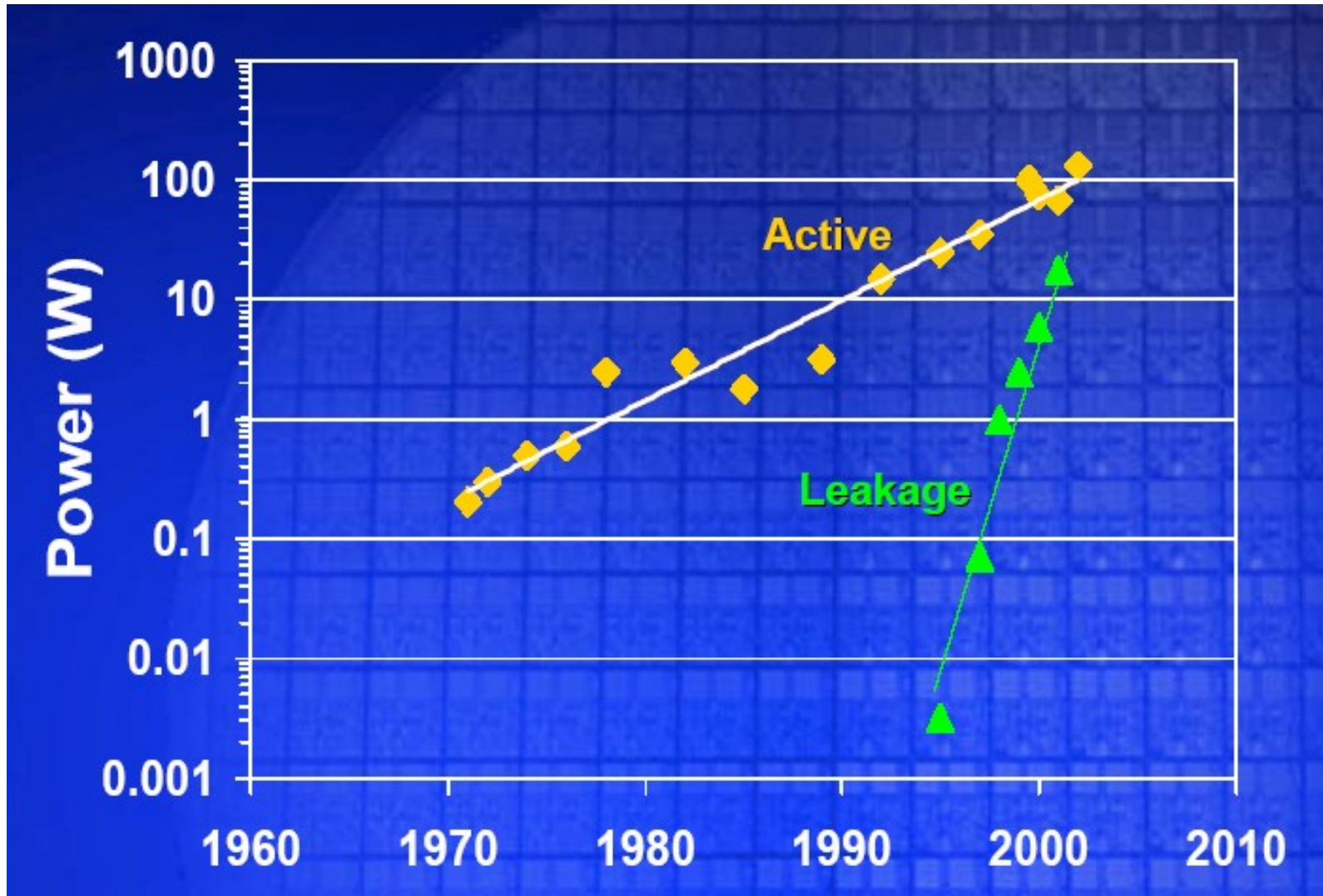




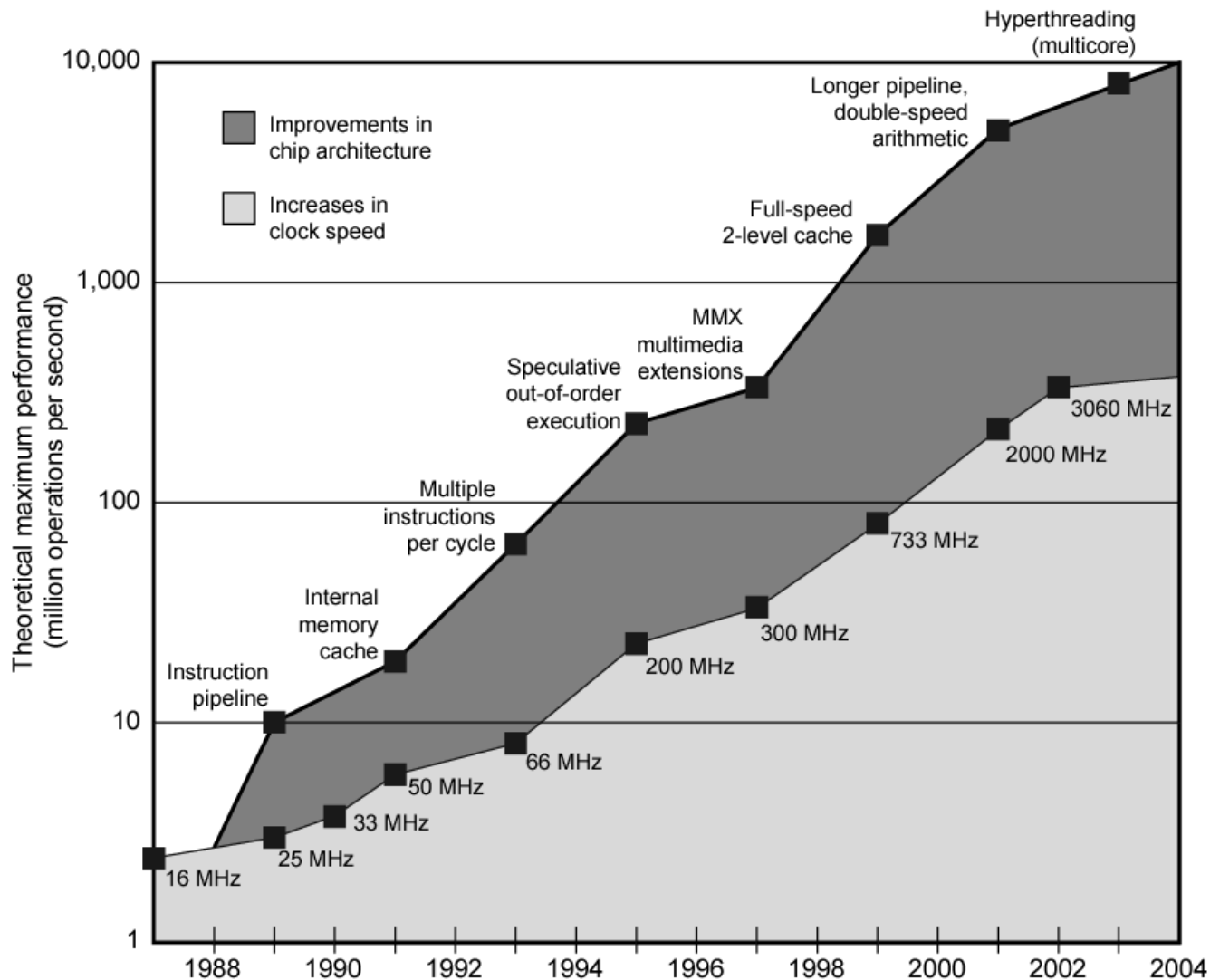
# Semiconductor Growth



# Processor Power (Watts)



# Intel Microprocessor Performance



# Device Complexity

---

- Exponential increase in device complexity
  - Increasing with Moore's law (or faster)!
- Require exponential increases in design productivity

We have exponentially more transistors!

# Heterogeneity on Chip

---

- Greater diversity of on-chip elements
  - Processors
  - Software
  - Memory
  - Analog

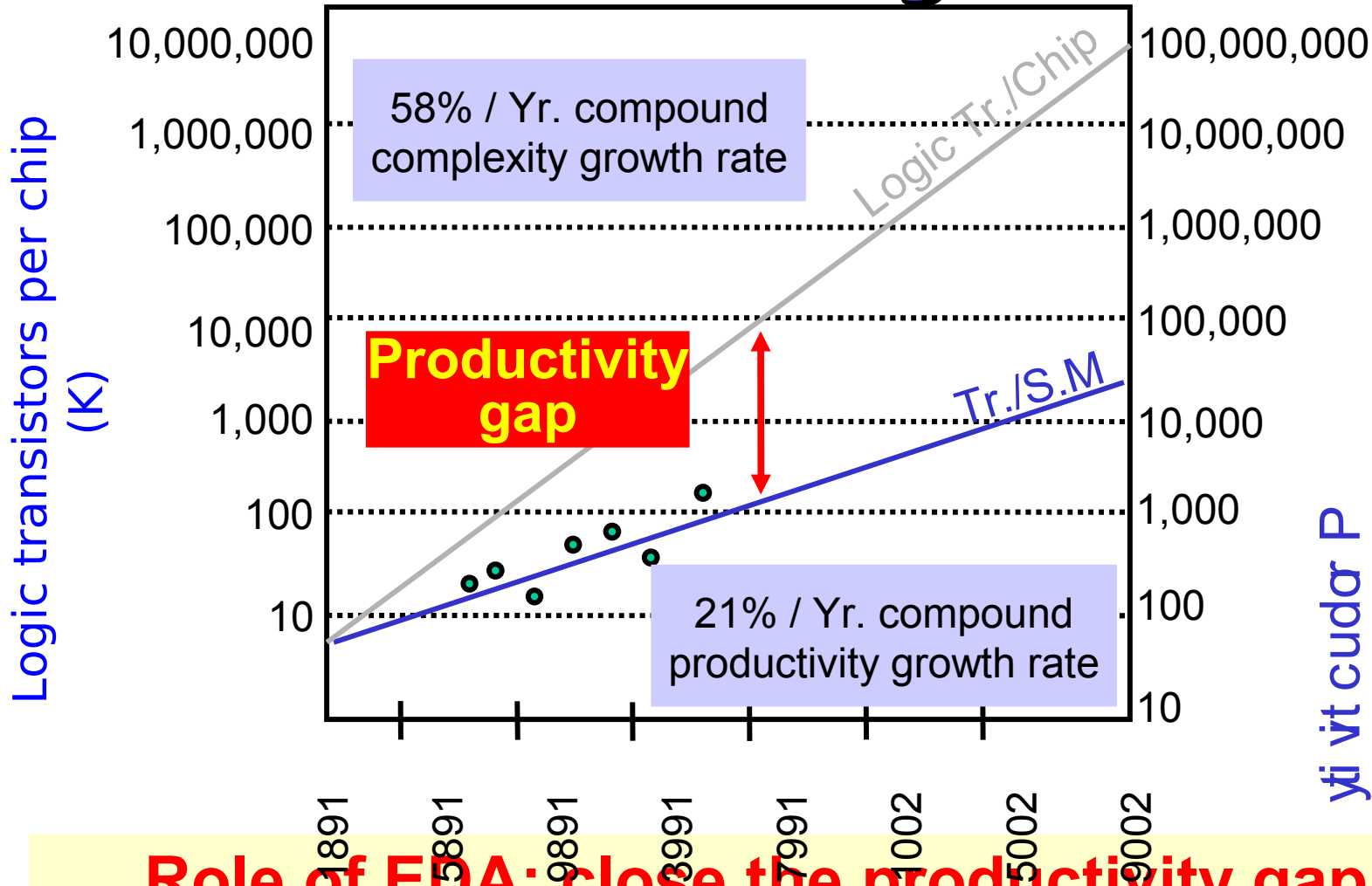
More transistors doing different things!

# Stronger Market Pressures

---

- Time-to-market
  - Decreasing design window
  - Less tolerance for design revisions

# How Are We Doing?



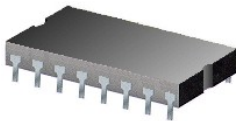
**Role of EDA: close the productivity gap**

# Evolution of Design Methodology

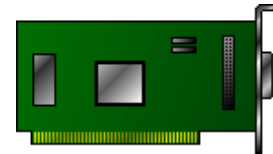
---

- We are now entering the era of *block-based design*

ASIC/ASSP  
Design

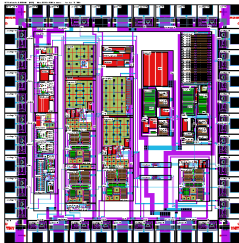


Yesterday  
Bus Standards,  
Predictable, Preverified

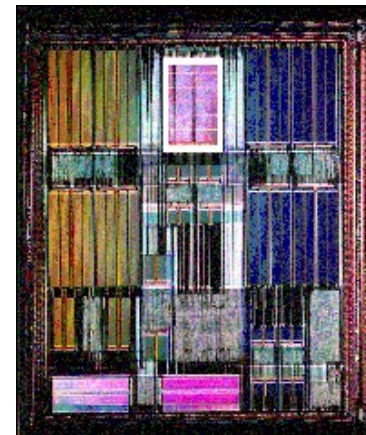


System-Board  
Integration

IP/Block  
Authoring



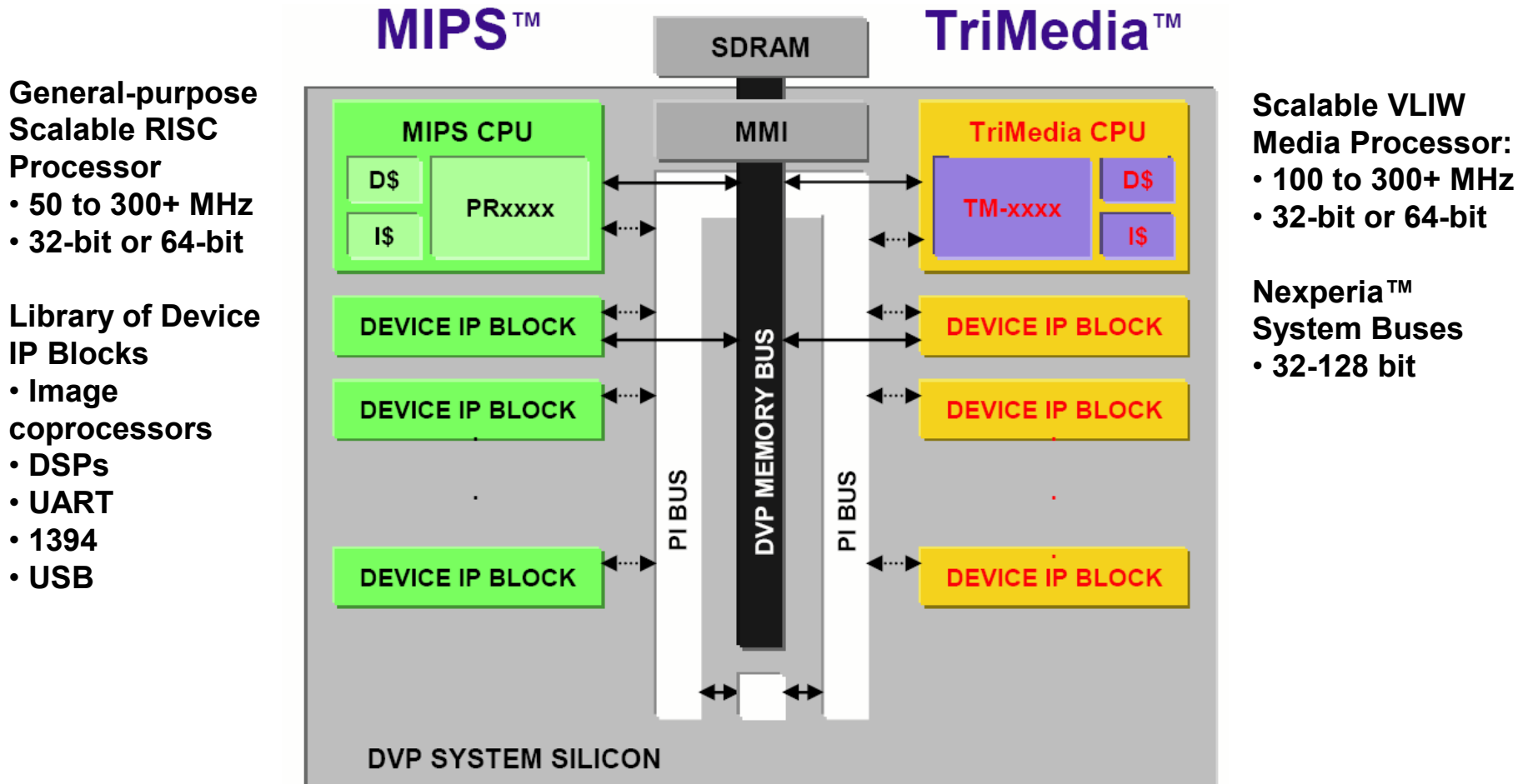
Today  
VSI Compatible Standards,  
Predictable, Preverified



System-Chip  
Integration



# Evolution of SoC Platforms



**2 Cores:** Philips' Nexperia PNX8850 SoC platform for High-end digital video (2001)

# What's Happening in SoCs?

---

## ■ Technology: no slow-down in sight!

Faster and smaller transistors: 90 → 65 → 45 → 32 nm

→ ... but slower wires, lower voltage, more noise!

✓ 80% or more of the delay of critical paths will be due to interconnects

## ■ Design complexity: from 2 to 10 to 100 cores!

→ Design reuse is essential

→ ...but differentiation/innovation is key for winning on the market!

## ■ Performance and power:

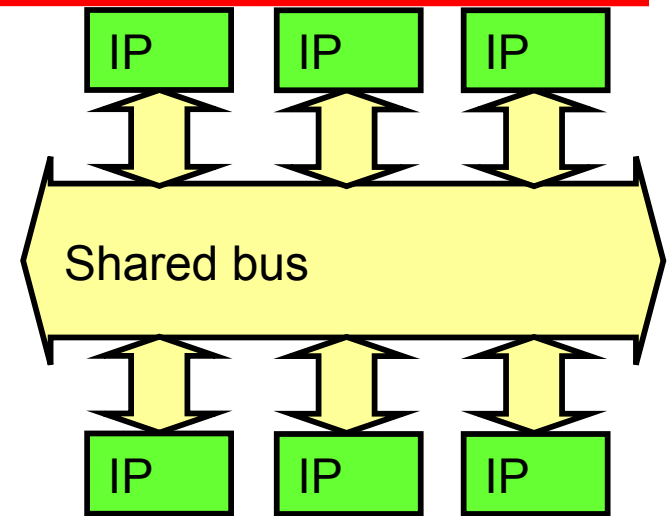
→ Performance requirements keep going up

→ ...but power budgets don't!

# Communication Architectures

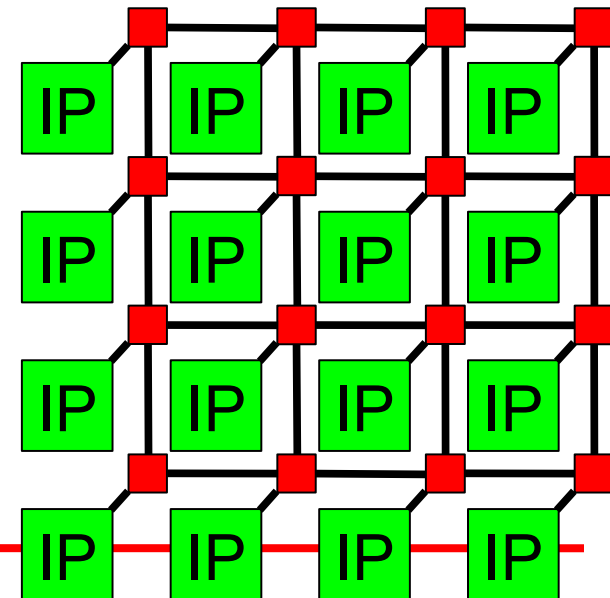
## ■ Shared bus

- Low area
- Poor scalability
- High energy consumption



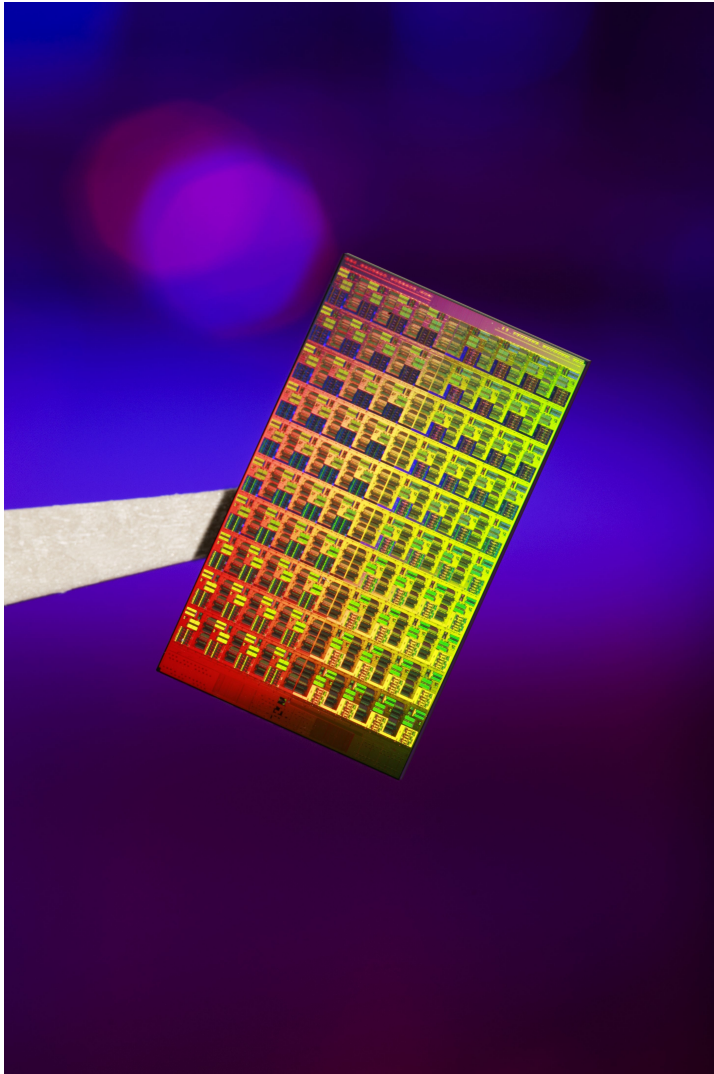
## ■ Network-on-Chip

- Scalability and modularity
- Low energy consumption
- Increase of design complexity



# Intel's Teraflops

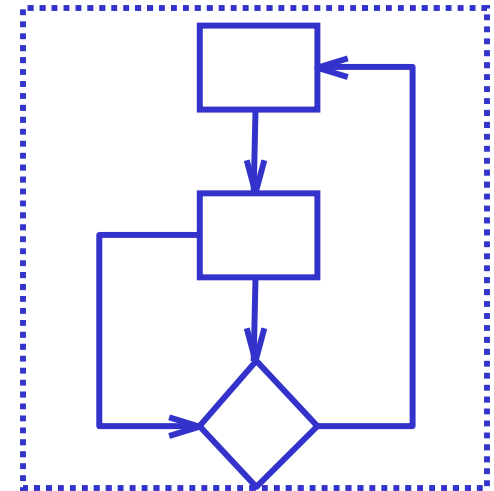
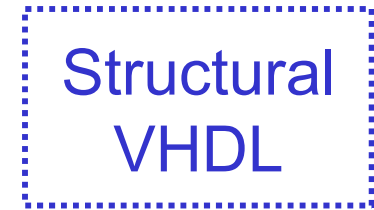
---



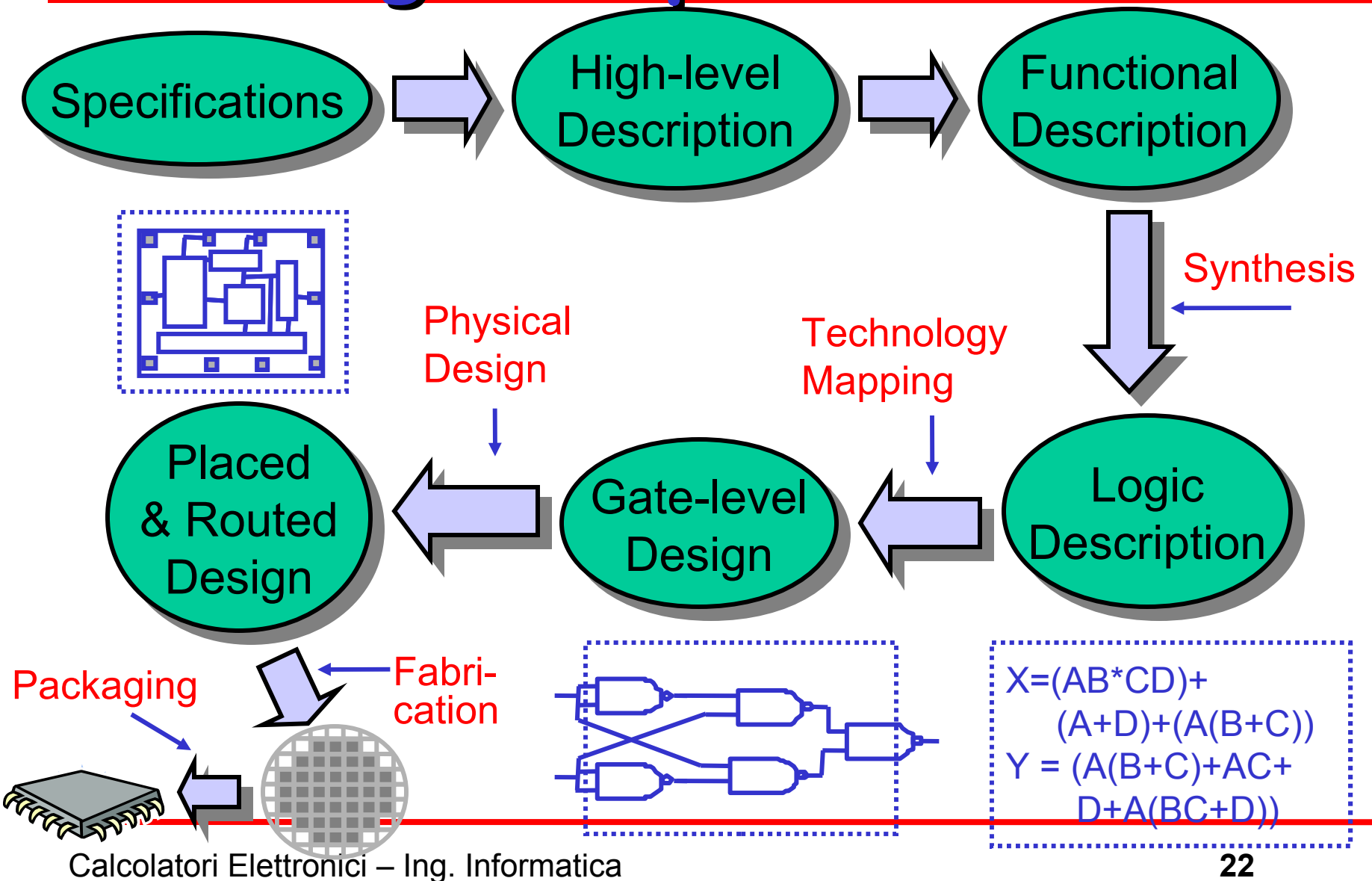
- 100 Million transistors
- 80 cores, 160 FP engines
- Teraflops perf. @ 62 Watts
- On-die mesh network
- Power aware design

# IC Design Steps

---



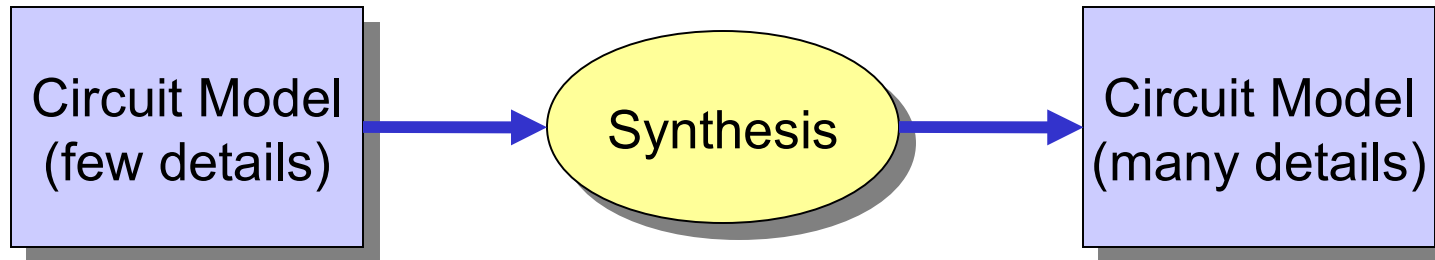
# IC Design Steps



# Circuit Models

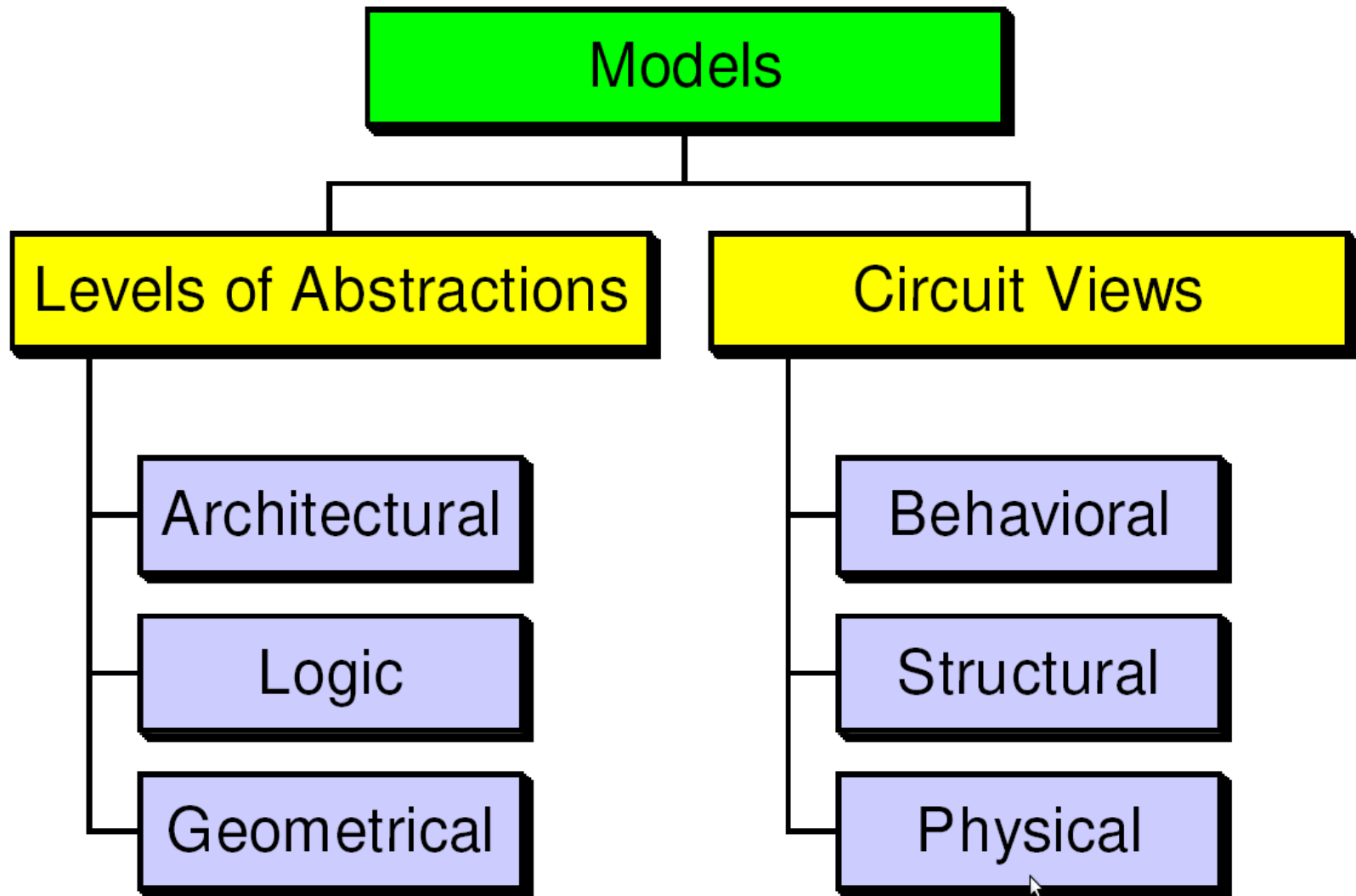
---

- A *model of a circuit* is an *abstraction*
  - A representation that shows relevant features without associated details



# Model Classification

---





# Levels of Abstraction

---

## ■ Architectural

- A circuit performs a set of operation, such as *data computation* or *transfer*
  - ✓ HDL models, Flow diagrams, ...

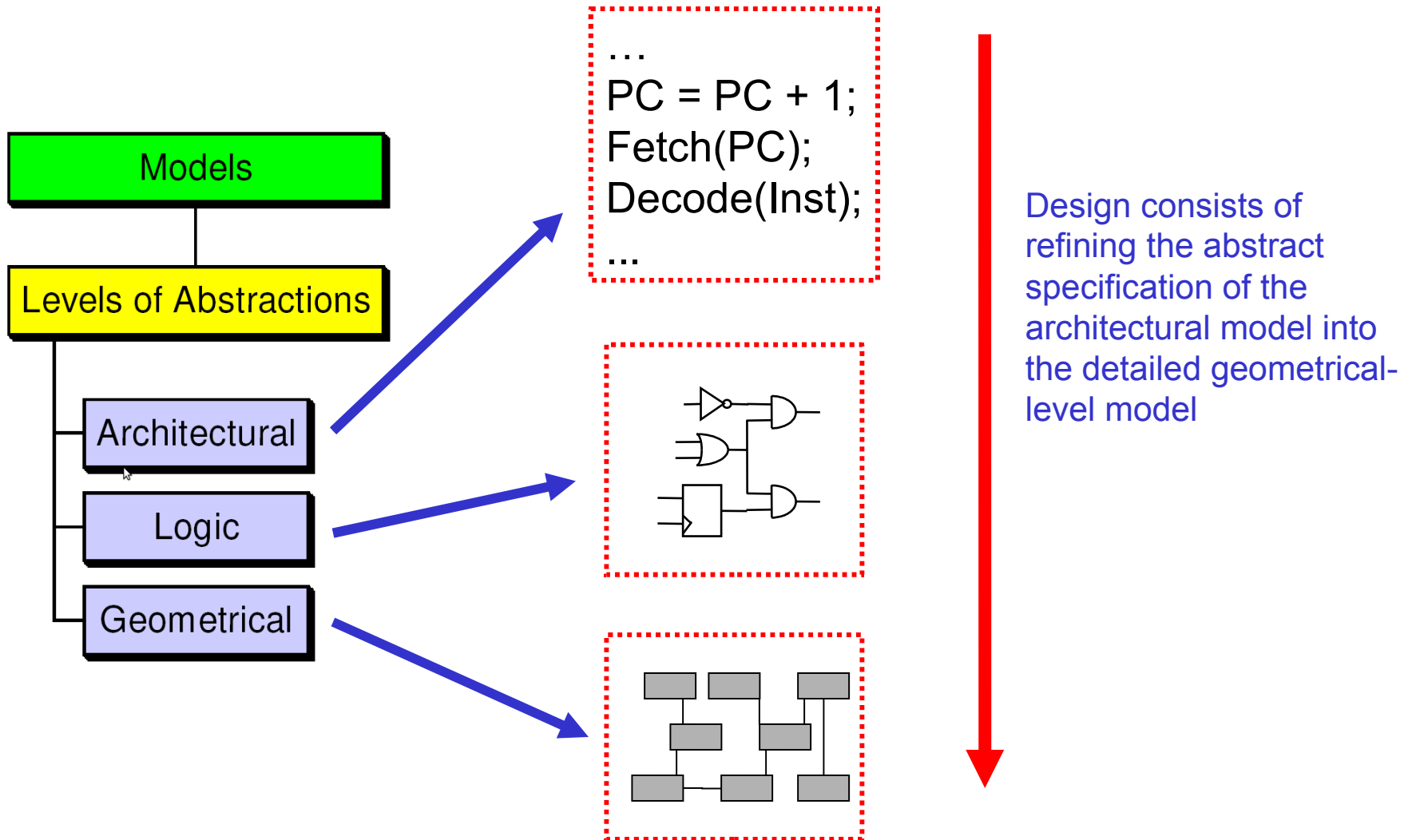
## ■ Logic

- A circuit evaluate a set of *logic functions*
  - ✓ FSMs, Schematics, ...

## ■ Geometrical

- A circuit is a set of *geometrical entities*
  - ✓ Floor plans, layouts, ...

# Levels of Abstraction



# Views of a Model

---

## ■ Behavioral

→ Describe the function of a circuit *regardless* of its implementation

## ■ Structural

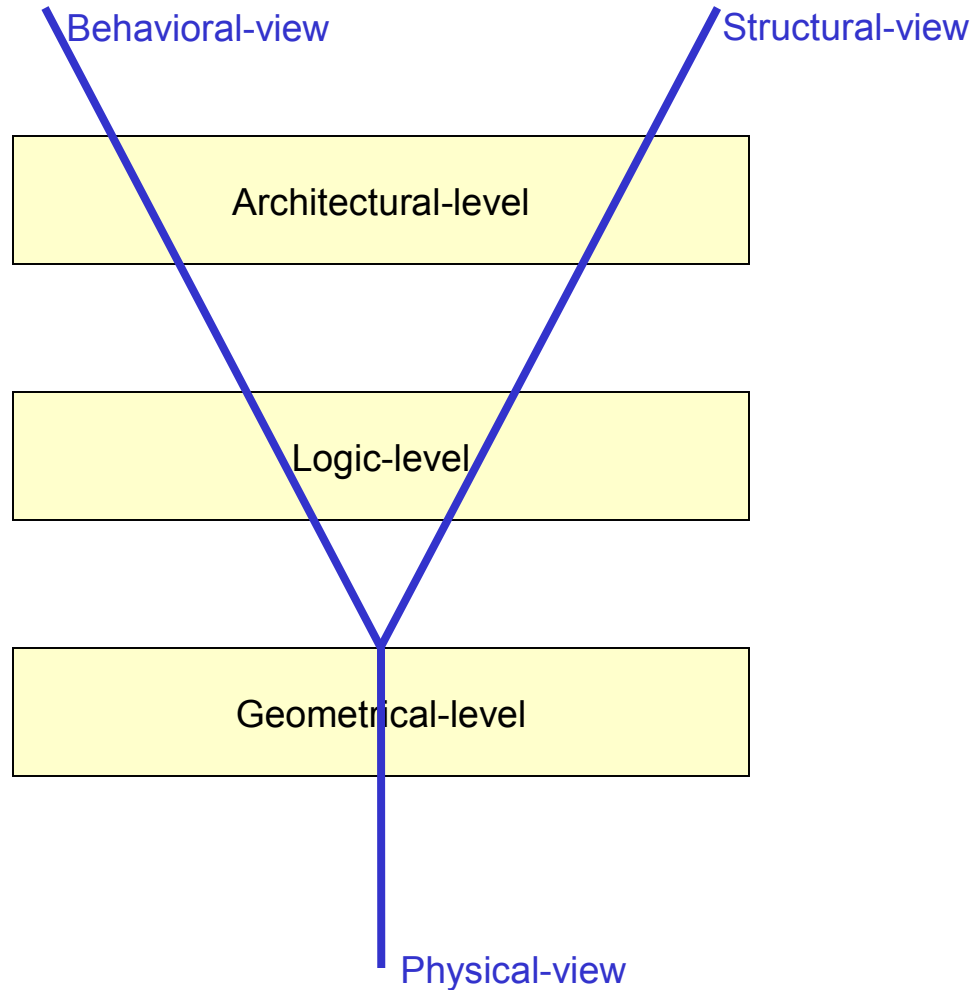
→ Describe a model as an *interconnection* of components

## ■ Physical

→ Relate to the *physical object* (e.g., transistors) of a design

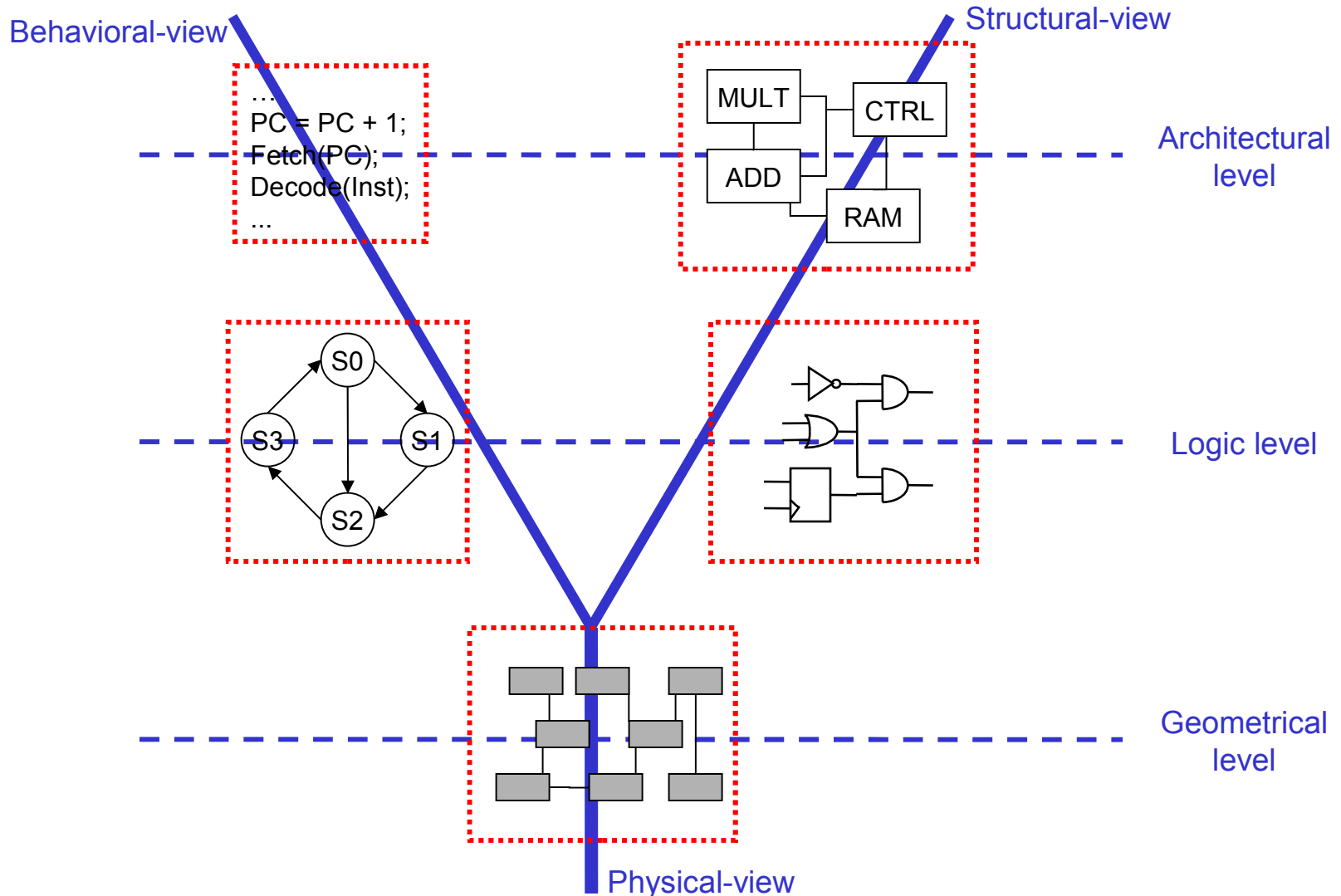
# The Y-chart

---



Gajski and Kuhn's Y-chart  
(Silicon Compilers, Addison-Wesley, 1987)

# The Y-chart



# Synthesis

---

